

Serial EEPROM Series Standard EEPROM

Plug & Play EEPROM

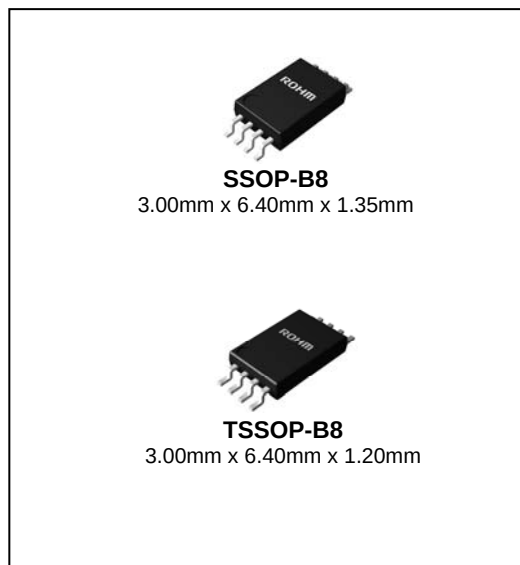
BR34L02-W

General Description

BR34L02-W is 256 × 8 bit Electrically Erasable PROM (Based on Serial Presence Detect)

Features

- 256 × 8 bit architecture serial EEPROM
- Wide operating voltage range: 1.7V-5.5V
- Two-wire serial interface
- High reliability connection using Au pads and Au wires
- Self-Timed Erase and Write Cycle
- Page Write Function (16byte)
- Write Protect Mode
 - Write Protect 1 (Onetime Rom) : 00h-7Fh
 - Write Protect 2 (Hardwire WP PIN) : 00h-FFh
- Low Power consumption
 - Write (at 5V) :1.2mA (typ.)
 - Read (at 5V) :0.2mA(typ.)
 - Standby (at 5V) :0.1μA(typ.)
- DATA security
 - Write protect feature (WP pin)
 - Inhibit to WRITE at low Vcc
- High reliability fine pattern CMOS technology
- Rewriting possible up to 1,000,000 times
- Data retention: 40 years
- Noise reduction Filtered inputs in SCL / SDA
- Initial data FFh at all addresses

Packages W(Typ.) × D(Typ.) × H(Max.)

BR34L02-W

Capacity	Bit format	Type	Power Source Voltage	SSOP-B8	TSSOP-B8
2Kbit	256 x 8	BR34L02-W	1.7V to 5.5V	●	●

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit	Remarks
Supply Voltage	Vcc	-0.3 to +6.5	V	
Power Dissipation	Pd	300 (SSOP-B8)	mW	Reduce by 3.0mW/°C over 25°C
		330 (TSSOP-B8)		Reduce by 3.3mW/°C over 25°C
Storage Temperature	Tstg	-65 to +125	°C	
Operating Temperature	Topr	-40 to +85	°C	
Terminal Voltage	-	-0.3 to Vcc+0.3	V	

●Memory Cell Characteristics(Ta=25°C, Vcc=1.7V to 5.5V)

Parameter	Specification			Unit
	Min.	Typ.	Max.	
Write / Erase Cycle ^{*1}	1,000,000	-	-	Times
Data Retention ^{*1}	40	-	-	Years

*1: Not 100% TESTED

●Recommended Operating Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc	1.7 to 5.5	V
Input Voltage	VIN	0 to Vcc	V

●Electrical Characteristics

DC(Unless otherwise specified Ta=-40°C to +85°C, Vcc=1.7V to 5.5V)

Parameter	Symbol	Specification			Unit	Test Condition
		Min.	Typ.	Max.		
"H" Input Voltage 1	VIH1	0.7 Vcc	-	-	V	2.5V ≤ Vcc ≤ 5.5V
"L" Input Voltage 1	VIL1	-	-	0.3 Vcc	V	2.5V ≤ Vcc ≤ 5.5V
"H" Input Voltage 2	VIH2	0.8 Vcc	-	-	V	1.7V ≤ Vcc < 2.5V
"L" Input Voltage 2	VIL2	-	-	0.2 Vcc	V	1.7V ≤ Vcc < 2.5V
"L" Output Voltage 1	VOL1	-	-	0.4	V	IOL=3.0mA, 2.5V ≤ Vcc ≤ 5.5V(SDA)
"L" Output Voltage 2	VOL2	-	-	0.2	V	IOL=0.7mA, 1.7V ≤ Vcc < 2.5V(SDA)
Input Leakage Current 1	ILI1	-1	-	1	μA	VIN=0V to Vcc(A0,A1,A2,SCL)
Input Leakage Current 2	ILI2	-1	-	15	μA	VIN=0V to Vcc(WP)
Output Leakage Current	ILO	-1	-	1	μA	VOUT=0V to Vcc(SDA)
Operating Current	ICC1	-	-	2.0	mA	Vcc=5.5V, fSCL=400kHz, tWR=5ms Byte Write Page Write Write Protect
	ICC2	-	-	0.5	mA	Vcc=5.5V, fSCL=400kHz Random Read Current Read Sequential Read
Standby Current	ISB	-	-	2.0	μA	Vcc=5.5V, SDA,SCL= Vcc A0,A1,A2=GND, WP=GND

AC(Unless otherwise specified Ta=-40°C to +85°C, Vcc =1.7V to 5.5V)

Parameter	Symbol	FAST-MODE 2.5V ≤ Vcc ≤ 5.5V			STANDARD-MODE 1.7V ≤ Vcc ≤ 5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	fSCL	-	-	400	-	-	100	kHz
Data Clock High Period	tHIGH	0.6	-	-	4.0	-	-	μs
Data Clock Low Period	tLOW	1.2	-	-	4.7	-	-	μs
SDA and SCL Rise Time ^{*1}	tR	-	-	0.3	-	-	1.0	μs
SDA and SCL Fall Time ^{*1}	tF	-	-	0.3	-	-	0.3	μs
Start Condition Hold Time	tHD:STA	0.6	-	-	4.0	-	-	μs
Start Condition Setup Time	tSU:STA	0.6	-	-	4.7	-	-	μs
Input Data Hold Time	tHD:DAT	0	-	-	0	-	-	ns
Input Data Setup Time	tSU:DAT	50	-	-	50	-	-	ns
Output Data Delay Time	tPD	0.1	-	0.9	0.2	-	3.5	μs
Output Data Hold Time	tDH	0.1	-	-	0.2	-	-	μs
Stop Condition Setup Time	tSU:STO	0.6	-	-	4.7	-	-	μs
Bus Free Time	tBUF	1.2	-	-	4.7	-	-	μs
Write Cycle Time	tWR	-	-	5	-	-	5	ms
Noise Spike Width (SDA and SCL)	tI	-	-	0.1	-	-	0.1	μs
WP Hold Time	tHD : WP	0	-	-	0	-	-	ns
WP Setup Time	tSU : WP	0.1	-	-	0.1	-	-	μs
WP High Period	tHIGH : WP	1.0	-	-	1.0	-	-	μs

*1 : Not 100% TESTED

■Fast / Standard Modes

Fast mode and Standard mode differ only in operation frequency. Operations performed at 100kHz are considered in "Standard-mode", while those conducted at 400kHz are in "Fast-mode".

Please note that these clock frequencies are maximum values. At lower power supply voltage it is difficult to operate at high speeds. The EEPROM can operate at 400kHz, between 2.5V and 5.5V, and at 100kHz from 1.7V-5.5V.

●Synchronous Data Timing

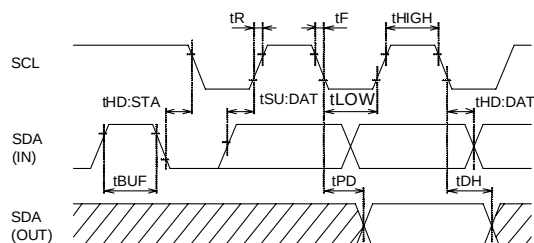


Figure 1-(a). Synchronous Data Timing

○SDA data is latched into the chip at the rising edge of SCL clock.

○Output data toggles at the falling edge of SCL clock.

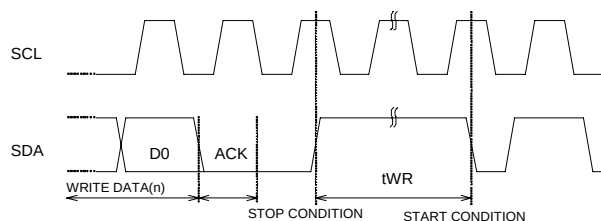


Figure 1-(c). Write Cycle Timing

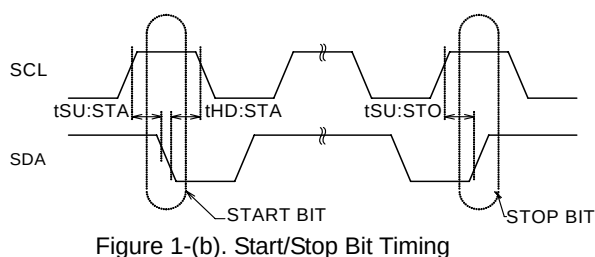


Figure 1-(b). Start/Stop Bit Timing

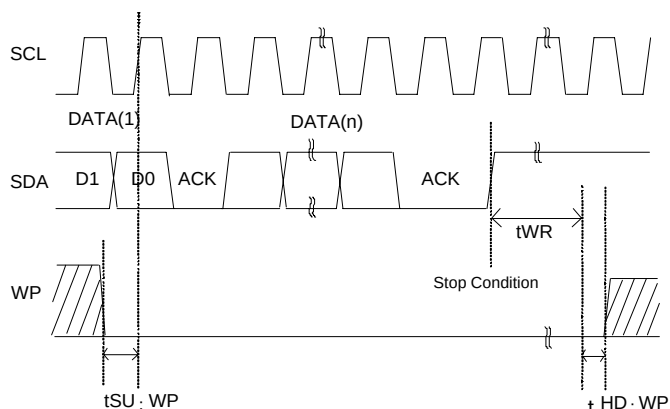


Figure 1-(d). WP Timing Of The Write Operation

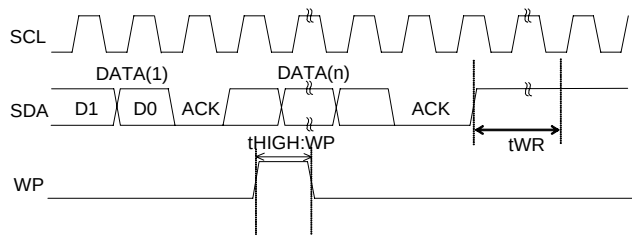
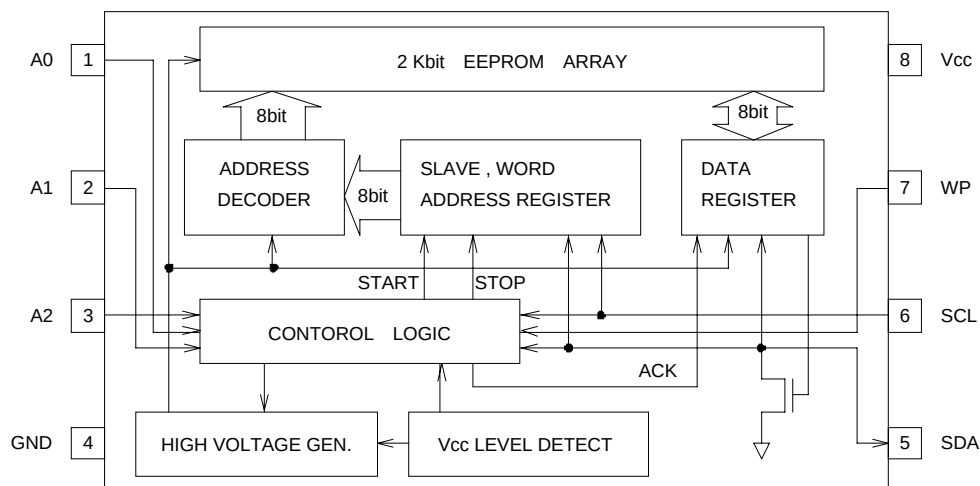


Figure 1-(e). WP Timing of The Write Cancel Operation

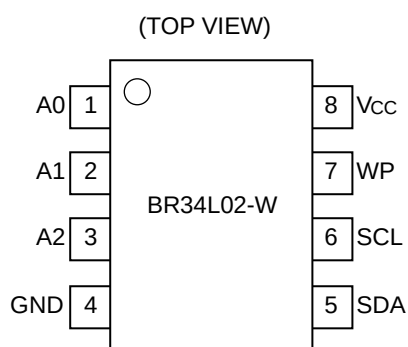
○For WRITE operation, WP must be "Low" from the rising edge of the clock (which takes in D0 of first byte) until the end of tWR. (See Figure 1-(d)) During this period, WRITE operation can be canceled by setting WP "High". (See Figure 1-(e))

○When WP is set to "High" during tWR, WRITE operation is immediately ceased, making the data unreliable. It must then be re-written.

●Block Diagram



● Pin Configuration



●Pin Descriptions

Pin Name	Input/Output	Functions
Vcc	-	Power Supply
GND	-	Ground 0V
A0,A1,A2	IN	Slave Address Set.
SCL	IN	Serial Clock Input
SDA	IN / OUT	Slave and Word Address, Serial Data Input, Serial Data Output ^{*1}
WP	IN	Write Protect Input ^{*2}

*1 Open drain output requires a pull-up resistor.

*2 WP Pin has a Pull-Down resistor. Please leave unconnected or connect to GND when not in use.

● Typical Performance Curves

The following characteristic data are typ. value.

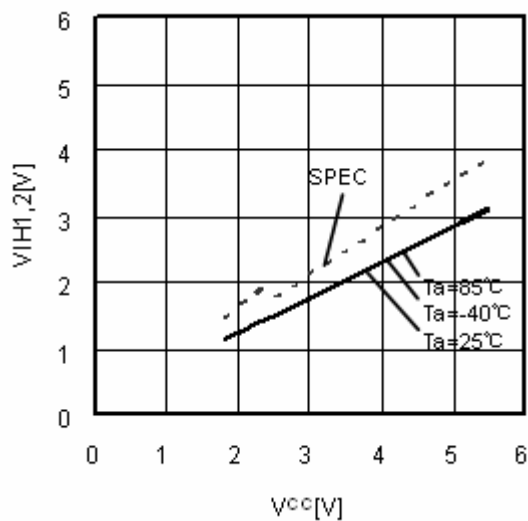


Figure 2. "H" Input Voltage $V_{IH1,2}$
(A0,A1,A2,SCL,SDA,WP)

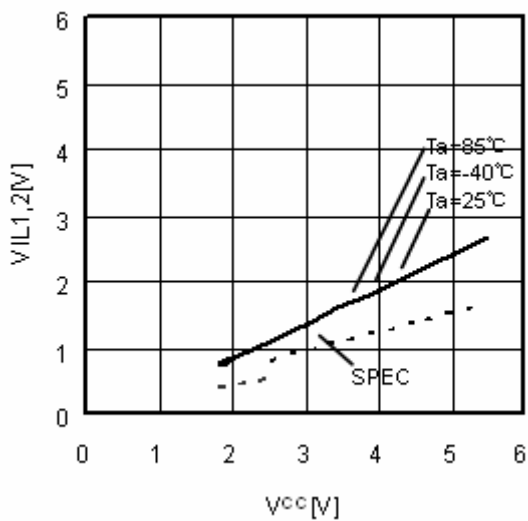


Figure 3. "L" Input Voltage $V_{IL1,2}$
(A0,A1,A2,SCL,SDA,WP)

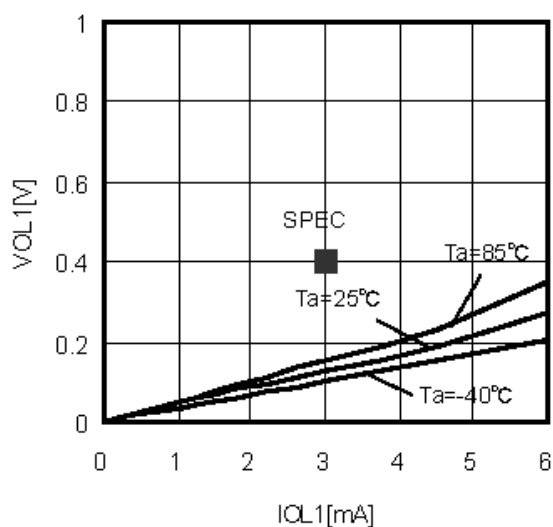


Figure 4. "L" Output Voltage
 $V_{OL1-IOL1}$ ($V_{CC}=2.5V$)

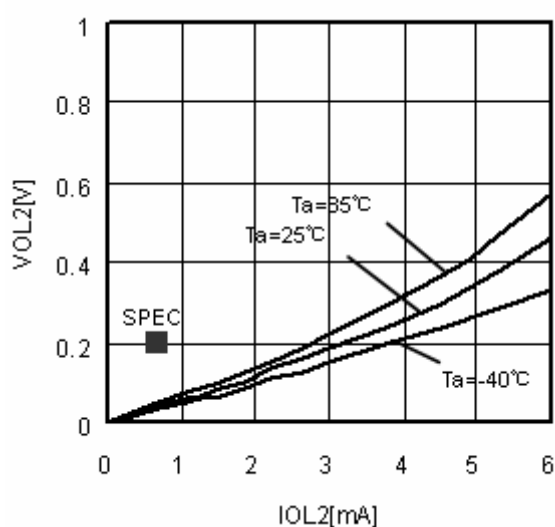


Figure 5. "L" Output Voltage
 $V_{OL2-IOL2}$ ($V_{CC}=1.7V$)

● Typical Performance Curves - Continued

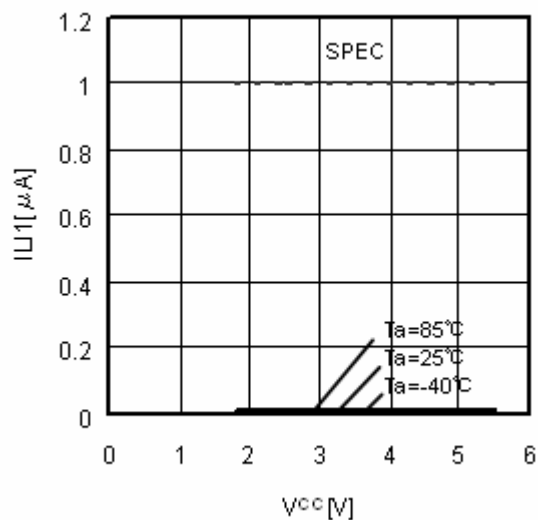


Figure 6. Input Leakage Current
ILI1 (A0,A1,A2,SCL,SDA)

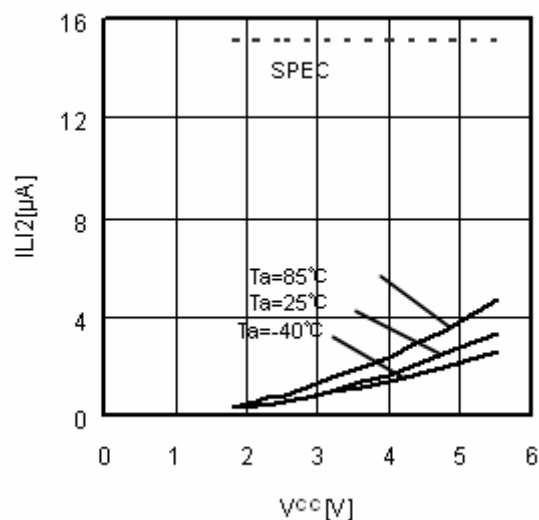


Figure 7. Input Leakage Current
ILI2 (WP)

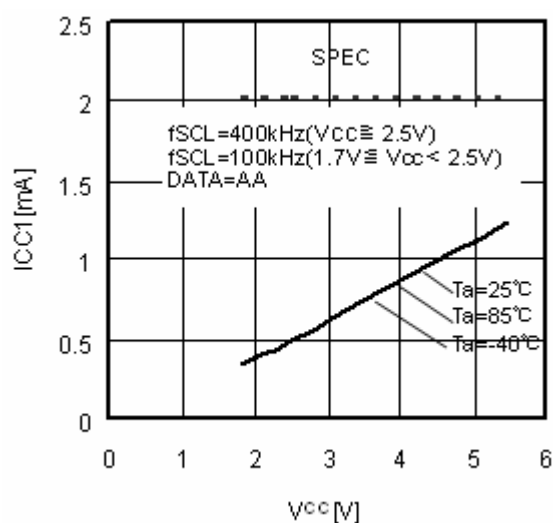


Figure 8. Write Operating Current
ICC1 (fSCL=100kHz,400kHz)

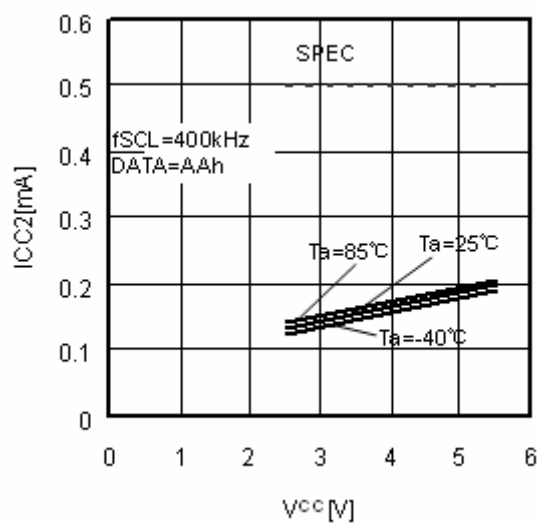
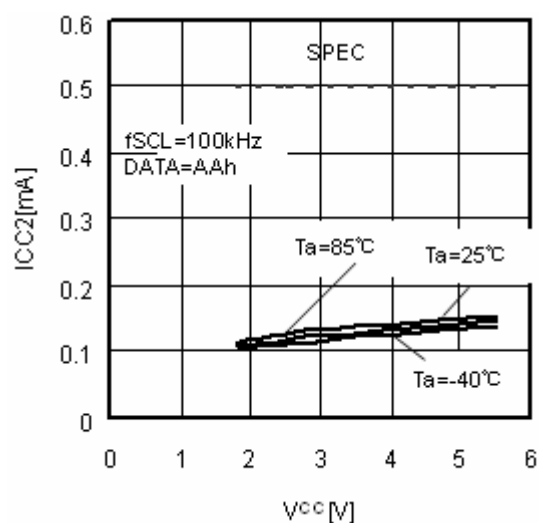
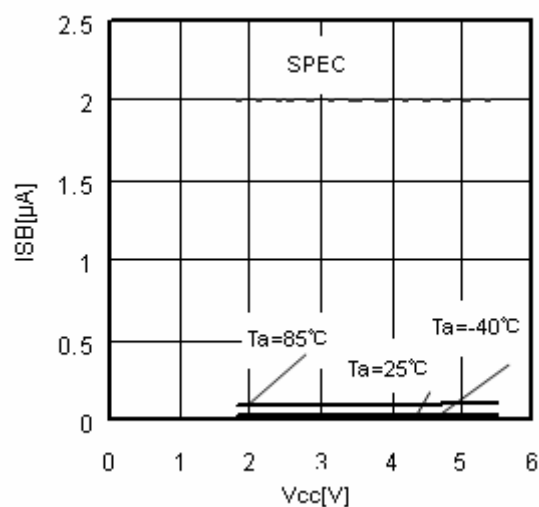
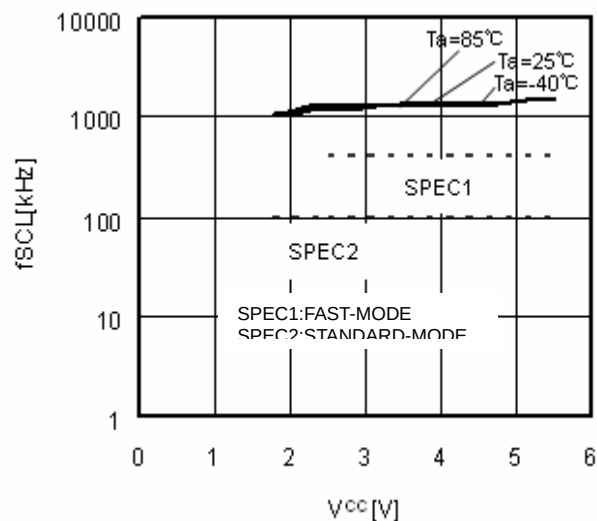
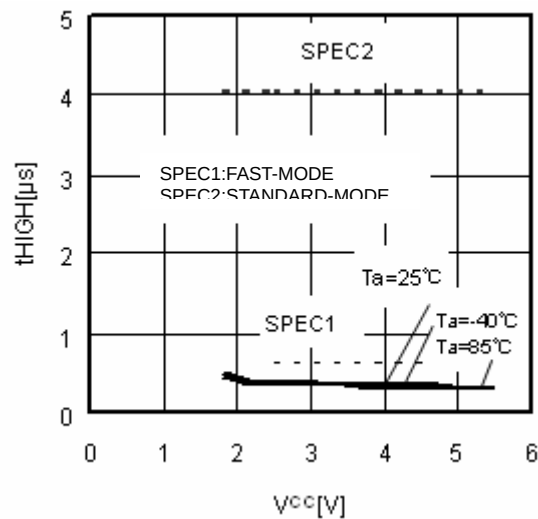


Figure 9. Read Operating Current
ICC2 (fSCL=400kHz)

● Typical Performance Curves - Continued

Figure 10. Read Operating Current $ICC2$ ($f_{SCL}=100\text{kHz}$)Figure 11. Standby Current ISB Figure 12. Clock Frequency f_{SCL} Figure 13. Data Clock High Period t_{HIGH}

● Typical Performance Curves - Continued

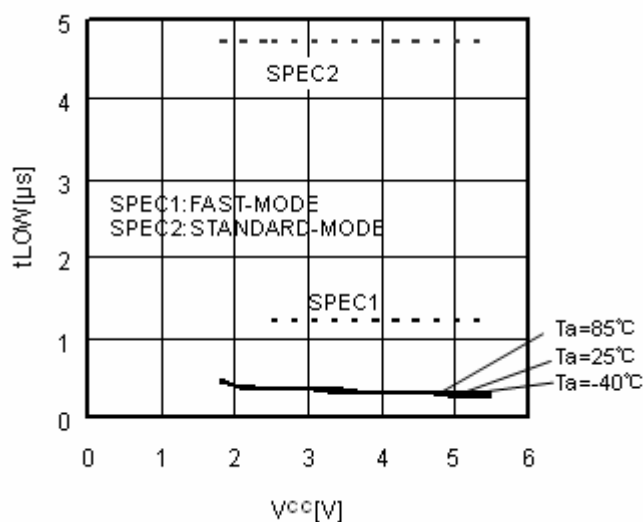


Figure 14. Data Clock Low Period
 t_{LOW}

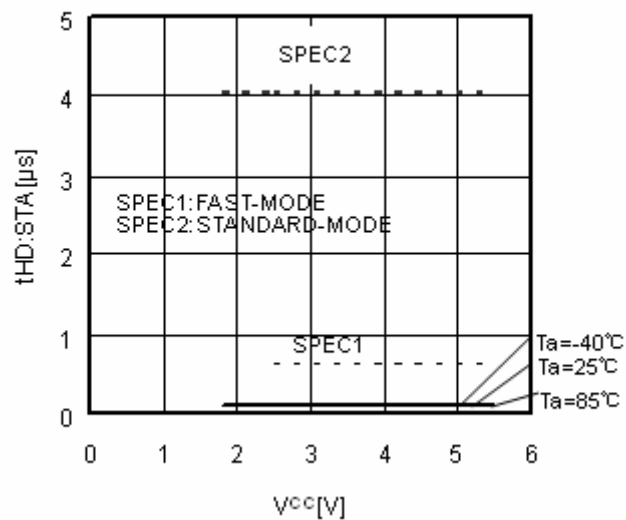


Figure 15. Start Condition Hold Time
 $t_{HD:STA}$

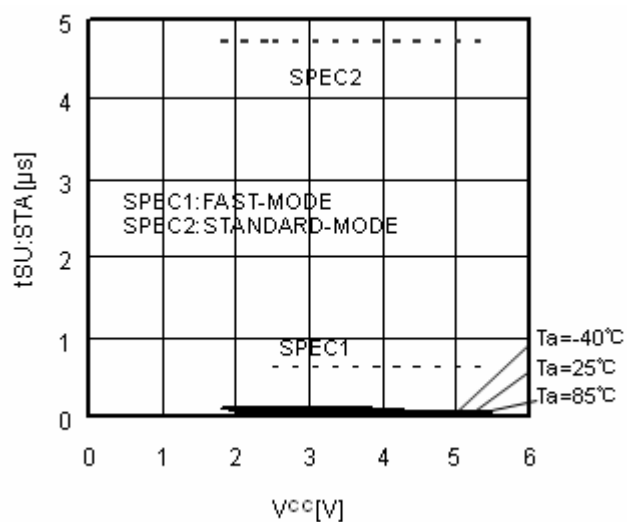


Figure 16. Start Condition Setup Time
 $t_{SU:STA}$

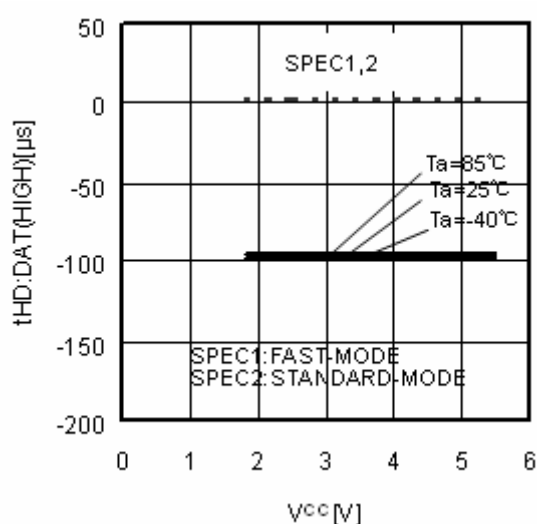


Figure 17. Input Data Hold Time
 $t_{HD:DAT (High)}$

● Typical Performance Curves - Continued

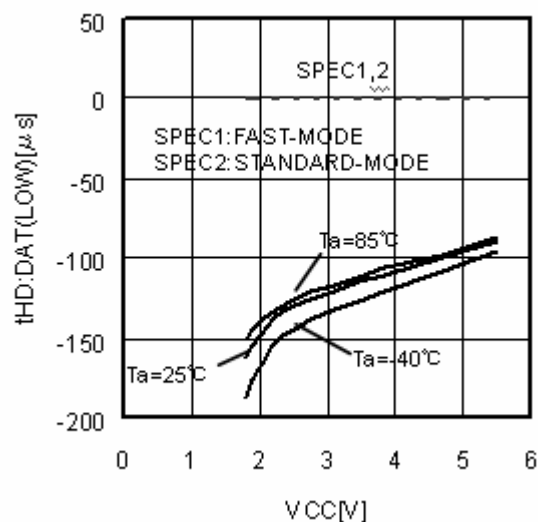


Figure 18. Input Data Hold Time
 $t_{HD:DAT(LOW)}$

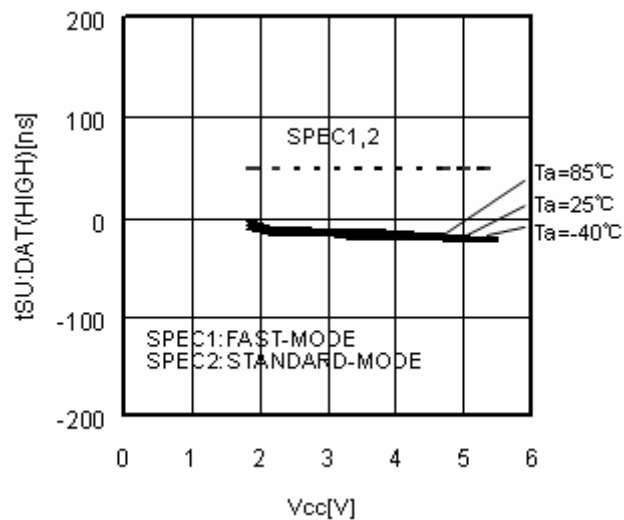


Figure 19. Input Data Setup Time
 $t_{SU:DAT(HIGH)}$

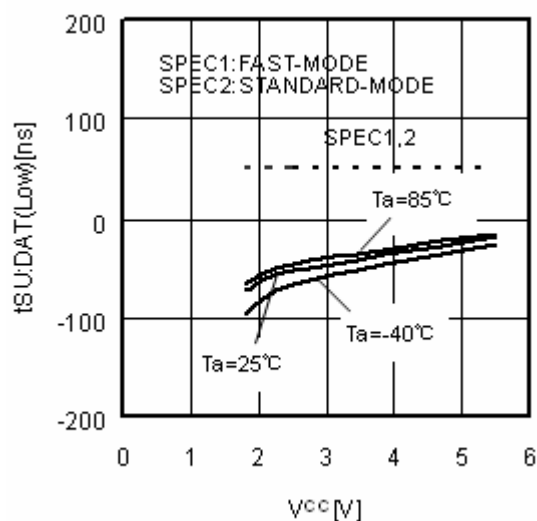


Figure 20. Input Data Setup Time
 $t_{SU:DAT(LOW)}$

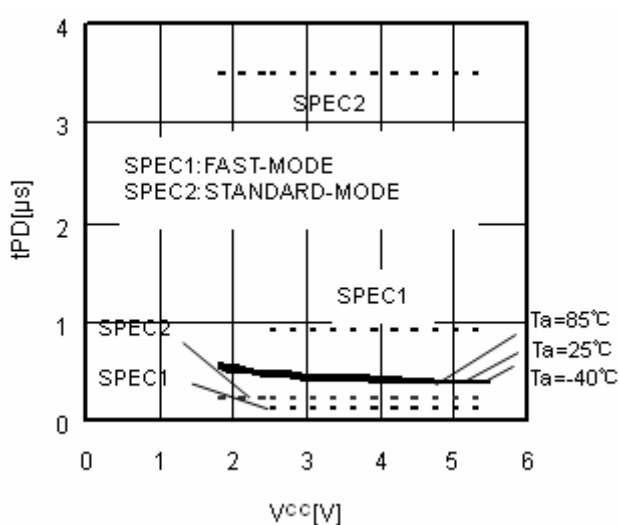
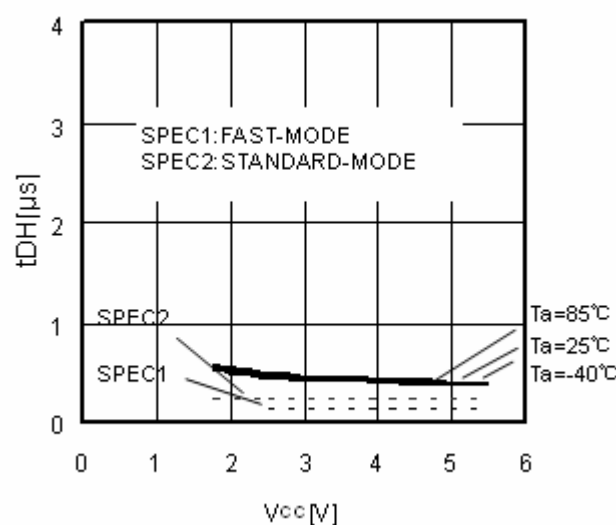
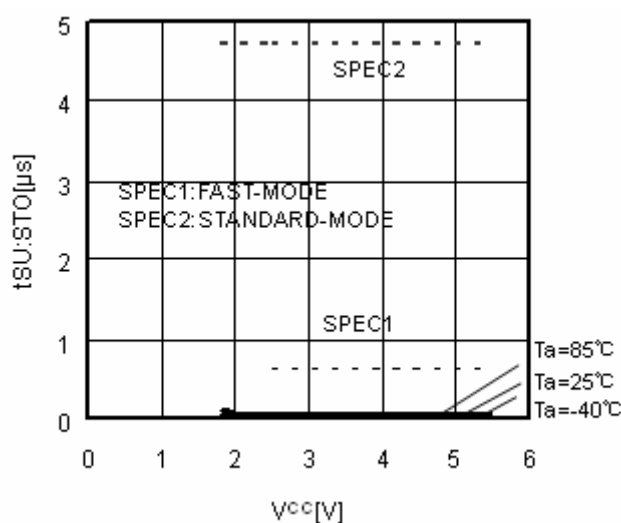
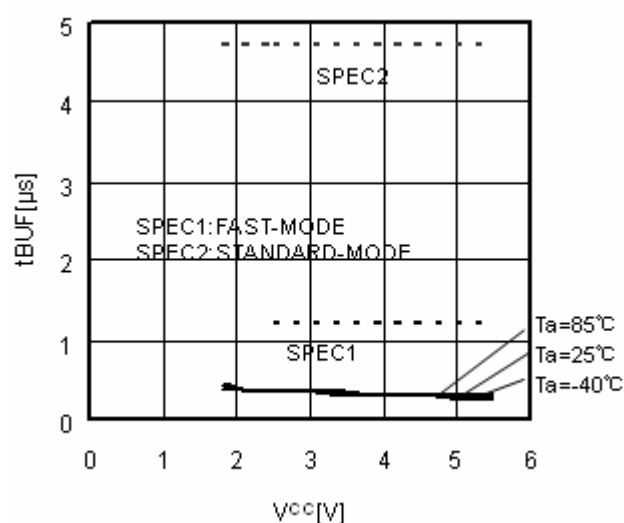
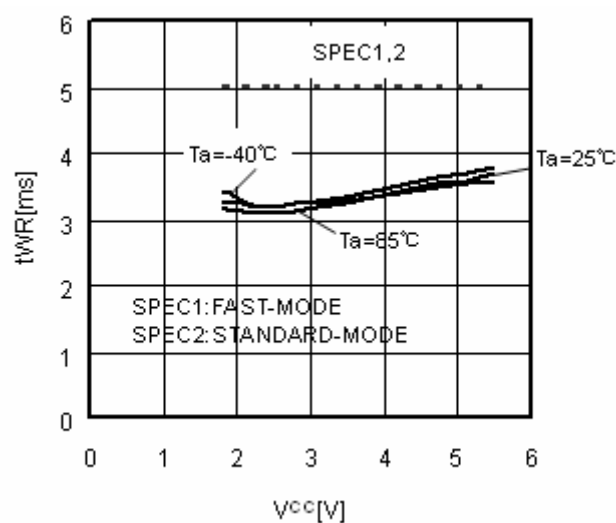


Figure 21. Output Data Delay Time
 t_{PD}

● Typical Performance Curves - Continued

Figure 22. Output Data Hold Time t_{DH} Figure 23. Stop Condition Setup Time $t_{SU:STO}$ Figure 24. Bus Free Time t_{BUF} Figure 25. Write Cycle Time t_{WR}

● Typical Performance Curves - Continued

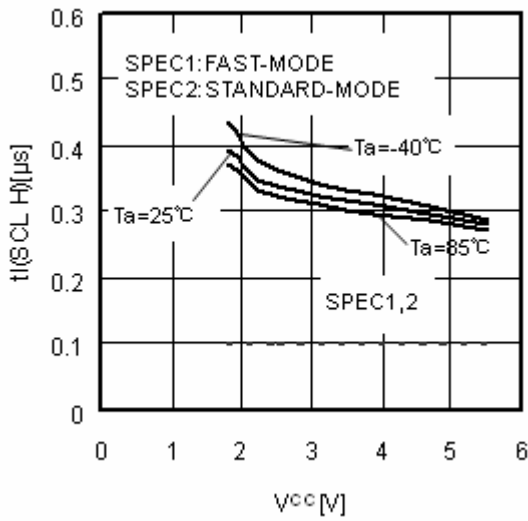


Figure 26. Noise Spike Width
 $t_I(\text{SCL H})$

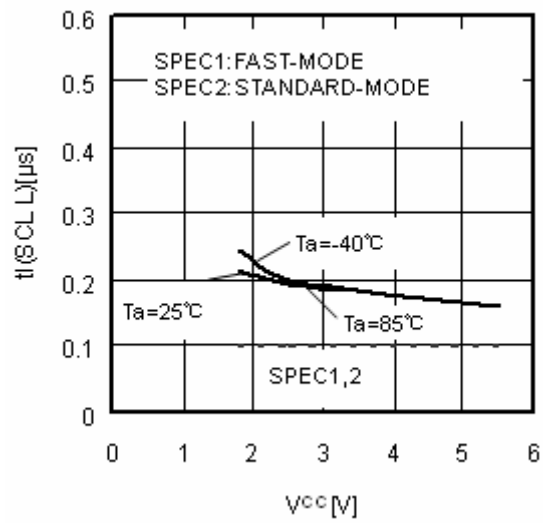


Figure 27. Noise Spike Width
 $t_I(\text{SCL L})$

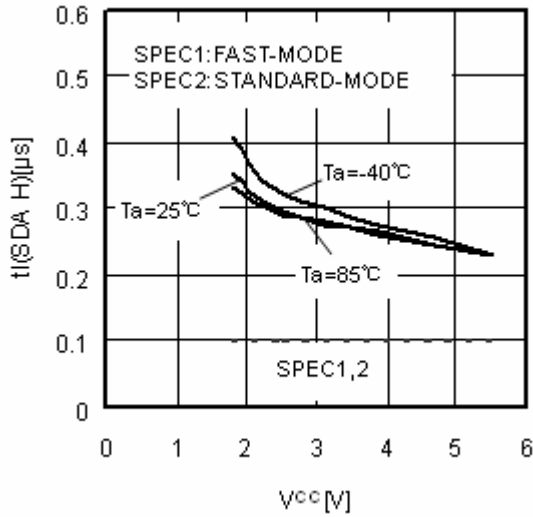


Figure 28. Noise Spike Width
 $t_I(\text{SDA H})$

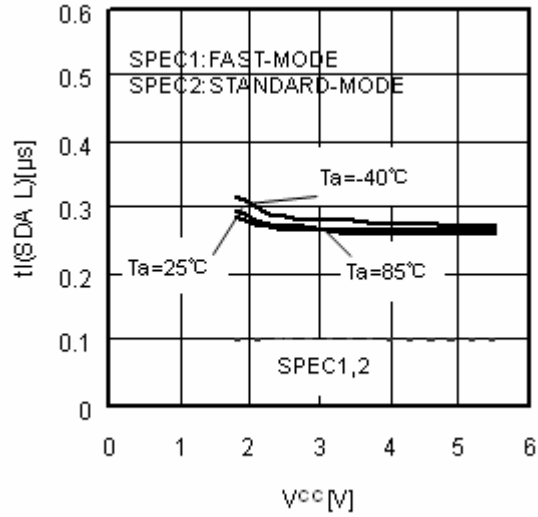


Figure 29. Noise Spike Width
 $t_I(\text{SDA L})$

●Typical Performance Curves - Continued

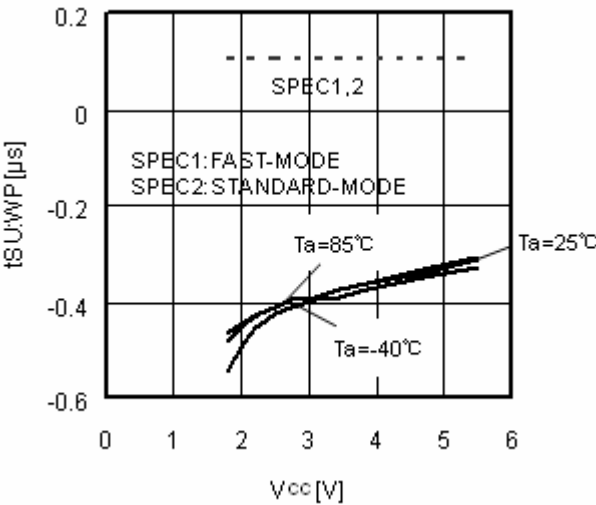


Figure 30. WP Setup Time
 $t_{SU:WP}$

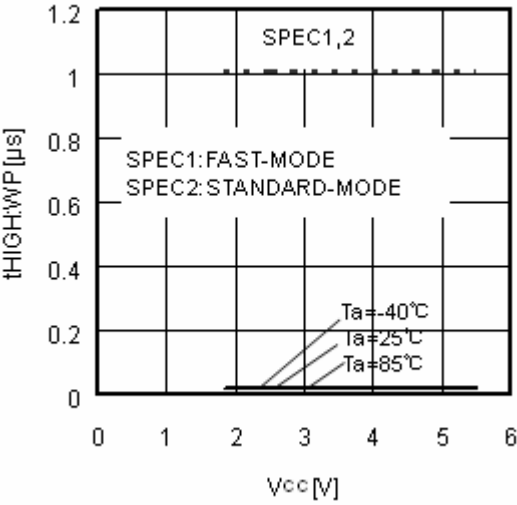


Figure 31. WP High Period
 $t_{High:WP}$

●Data transfer on the I²C BUS

○Data transfer on the I²C BUS

The BUS is considered to be busy after the START condition and free a certain time after the STOP condition.

Every SDA byte must be 8-bits long and requires an ACKNOWLEDGE signal after each byte. The devices have Master and Slave configurations. The Master device initiates and ends data transfer on the BUS and generates the clock signals in order to permit transfer.

The EEPROM in a slave configuration is controlled by a unique address. Devices transmitting data are referred to as the Transmitter. The devices receiving the data are called Receiver.

○START Condition (Recognition of the START bit)

- All commands are proceeded by the start condition, which is a High to Low transition of SDA when SCL is High.
- The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. (See Figure 1-(b) START/STOP Bit Timing)

○STOP Condition (Recognition of STOP bit)

- All communications must be terminated by a stop condition, which is a Low to High transition of SDA when SCL is High. (See Figure 1-(b) START/STOP Bit Timing)

○Acknowledge

- Acknowledge is a software used to indicate successful data transfers. The Transmitter device will release the BUS after transmitting eight bits. When inputting the slave address during write or read operation, the Transmitter is the μ -COM. When outputting the data during read operation, the Transmitter is the EEPROM.
- During the ninth clock cycle the Receiver will pull the SDA line Low to verify that the eight bits of data have been received. (When inputting the slave address during write or read operation, EEPROM is the receiver. When outputting the data during read operation the receiver is the μ -COM.)
- The device will respond with an Acknowledge after recognition of a START condition and its slave address (8bit).
- In WRITE mode, the device will respond with an Acknowledge after the receipt of each subsequent 8-bit word (word address and write data).
- In READ mode, the device will transmit eight bits of data, release the SDA line, and monitor the line for an Acknowledge.
- If an Acknowledge is detected and no STOP condition is generated by the Master, the device will continue to transmit the data. If an Acknowledge is not detected, the device will terminate further data transmissions and await a STOP condition before returning to standby mode.

○Device Addressing

- Following a START condition, the Master outputs the Slave address to be accessed. The most significant four bits of the slave address are the "device type identifier." For this EEPROM it is "1010." (For WP register access this code is "0110".)
- The next three bits identify the specified device on the BUS (device address). The device address is defined by the state of the A0,A1 and A2 input pins. This IC works only when the device address input from the SDA pin corresponds to the status of the A0,A1 and A2 input pins. Using this address scheme allows up to eight devices to be connected to the BUS. The last bit of the stream (R/W...READ/WRITE) determines the operation to be performed.

R/W=0 WRITE (including word address input of Random Read)
R/W=1 READ

Device Type	Device Address			Read Write Mode	Access Area
1010	A2	A1	A0	R/W	Access to Memory
0110	A2	A1	A0	R/W	Access to Write Protect Register

○Write Protect command

The Write Protect command cancels any write commands that access addresses 00 to 7Fh.

The Write Protect Register can be written to once (One time Rom).

Once this command is executed, the data is protected forever.

○Write Protect Pin (WP)

When the WP pin set to Vcc (H level), write protect is set for 256 words (all addresses). WP pin set to GND (L level) enables writing of 256 words (all addresses).

If permanent protection is implemented by the Write Protect command, writing is prohibited in the the lower half area (addresses 00 to 7Fh) regardless of the WP pin status.

The WP pin has a pulldown resistor. Please leave unconnected or connect to GND when not in use.

●Command

OWrite Cycle

During WRITE CYCLE operation data is written in the EEPROM. The Byte Write Cycle is used to write only one byte. In the case of writing continuous data consisting of more than one byte, Page Write is used. The maximum bytes that can be written at one time are 16 bytes.

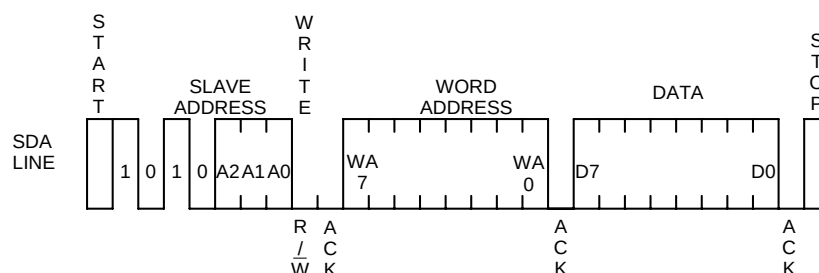


Figure 32. Byte Write Cycle Timing

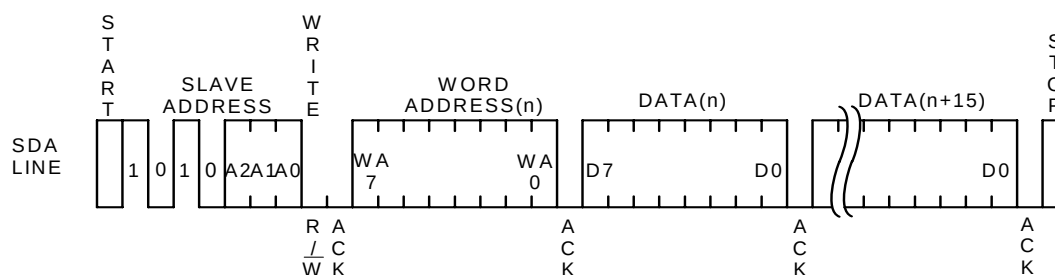


Figure 33. Page Write Cycle Timing

- With this command the data is programmed into the indicated word address.
- When the Master generates a STOP condition, the device begins the internal write cycle to the nonvolatile memory array. This device is capable of sixteen-byte Page Write operations. Once programming is started no commands are accepted for t_{WR} (5ms max.). If the Master transmits more than sixteen words prior to generating the STOP condition, the address counter will “roll over” and the previously transmitted data will be overwritten. When two or more byte of data are input, the four low order address bits are internally incremented by one after the receipt of each word, while the four higher order bits of the address (WA7 to WA4) remain constant.

ORead Cycle

During Read Cycle operation data is read from the EEPROM. The Read Cycle is composed of Random Read Cycle and Current Read Cycle. The Random Read Cycle reads the data in the indicated address.

The Current Read Cycle reads the data in the internally indicated address and verifies the data immediately after the Write Operation. The Sequential Read operation can be performed with both Current Read and Random Read. With the Sequential Read Cycle it is possible to continuously read the next data.

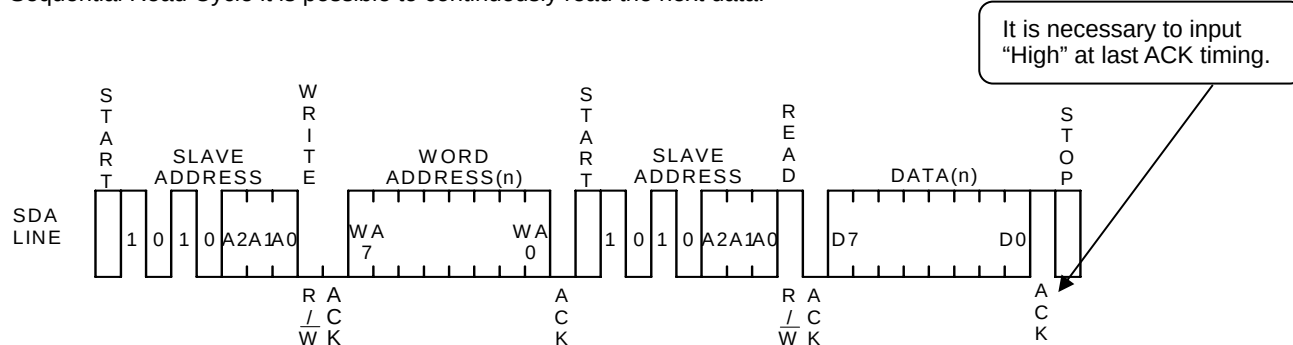


Figure 34. Random Read Cycle Timing

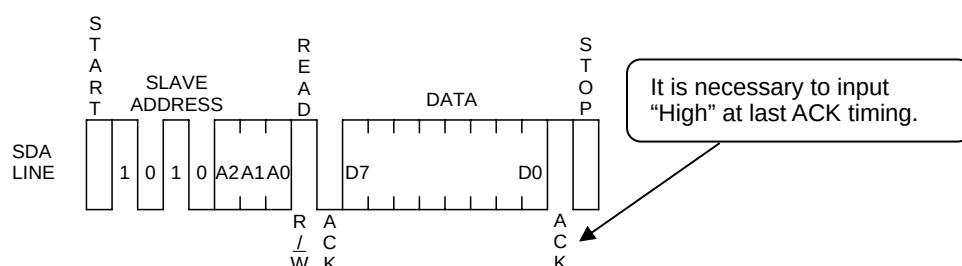


Figure 35. Current Read Cycle Timing

- Random Read operation allows the Master to access any memory location indicated by word address.
- In cases where the previous operation is Random or Current Read (which includes Sequential Read), the internal address counter is increased by one from the last accessed address (n). Thus Current Read outputs the data of the next word address (n+1).
- If an Acknowledge is detected and no STOP condition is generated by the Master (μ -COM), the device will continue to transmit data. (It can transmit all data (2kbit 256word))
- If an Acknowledge is not detected, the device will terminate further data transmissions and await a STOP condition before returning to standby mode.
- If an Acknowledge is detected with the "Low" level (not "High" level), the command will become Sequential Read, and the next data will be transmitted. Therefore, the Read command is not terminated. In order to terminate Read input Acknowledge with "High" always, then input a STOP condition.

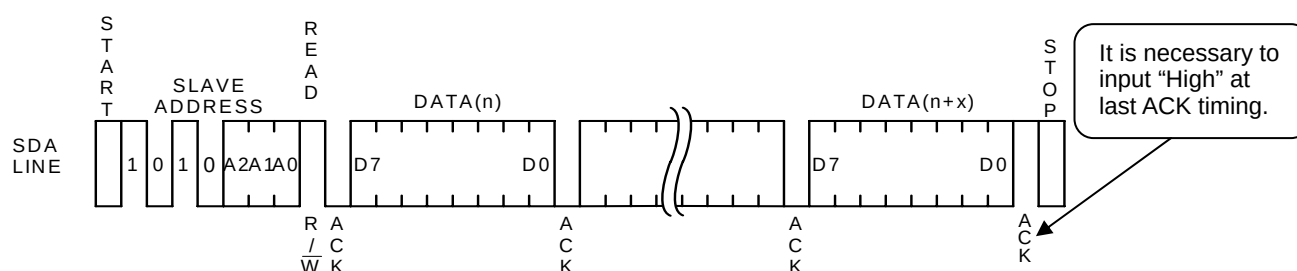


Figure 36. Sequential Read Cycle Timing (With Current Read)

●Software Reset

Execute software reset in the event that the device is in an unexpected state after power up and/or the command input needs to be reset. Below are three types (Figure 37-(a), (b), (c)) of software reset:

- During dummy clock, release the SDA BUS (tied to Vcc by a pull-up resistor) .
- During this time the device may pull the SDA line Low for Acknowledge or the outputting of read data.
- If the Master sets the SDA line to High, it will conflict with the device output Low, which can cause current overload and result in instantaneous power down, which may damage the device.

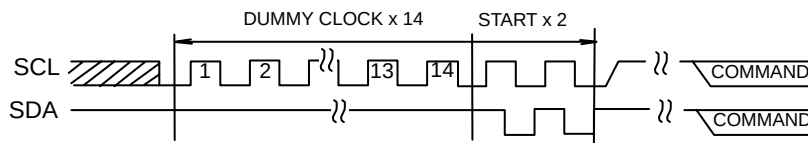


Figure 37-(a). DUMMY CLOCK x 14 + START+START

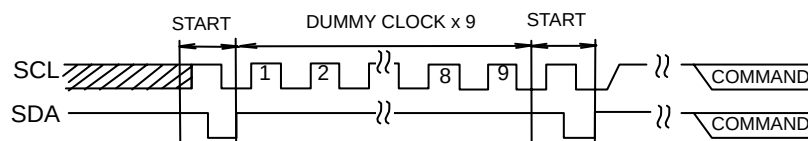


Figure 37-(b). START + DUMMY CLOCK x 9 + START

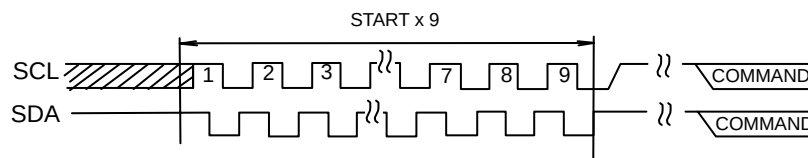


Figure 37-(c). START x 9

* COMMAND starts with start condition.

●Acknowledge polling

Since the IC ignores all input commands during the internal write cycle, no ACK signal will be returned.

When the Master sends the next command after the Write command, if the device returns an ACK signal it means that the program is completed. No ACK signal indicates that the device is still busy.

Using Acknowledge polling decreases the waiting time by $t_{WR}=5\text{ms}$.

When operating Write or Current Read after Write, first transmit the Slave address ($R/\bar{W}$ is "High" or "Low"). After the device returns the ACK signal continue word address input or data output.

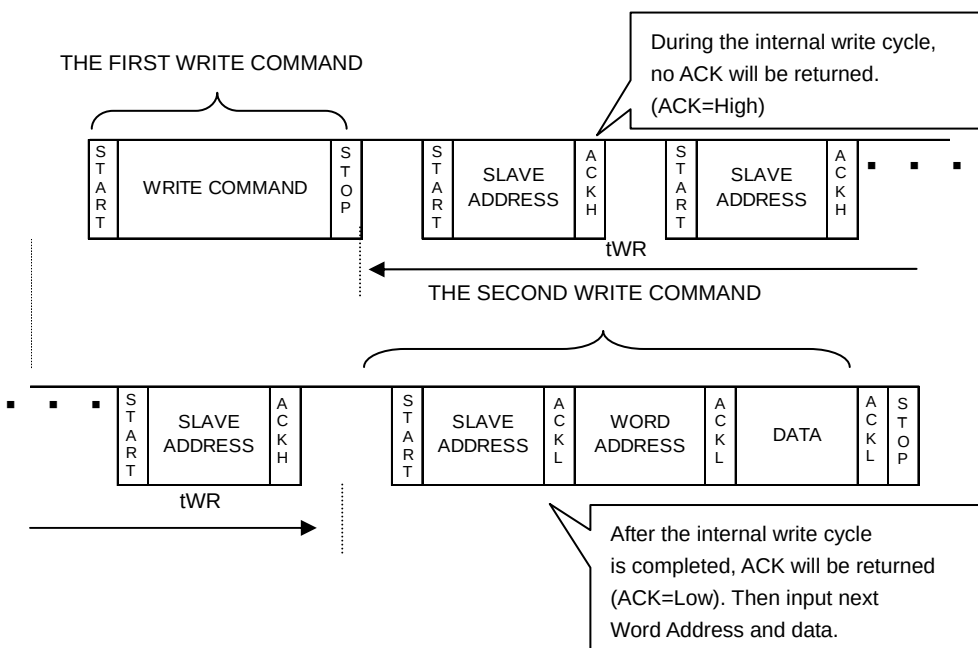


Figure 38. Successive Write Operation By Acknowledge Polling

●WP effective timing

WP is normally fixed at "H" or "L". However, in case WP needs to be controlled in order to cancel the Write command, pay attention to "WP effective timing" as follows:

The Write command is canceled by setting WP to "H" within the WP cancellation effective period.

The period from the START condition to the rising edge of the clock (which takes in the data D0 - the first byte of the Page Write data) is the 'invalid cancellation period'. WP input is considered inconsequential during this period. The setup time for the rising edge of the SCL, which takes in D0, must be more than 100ns.

The period from the rising edge of SCL (which takes in the data D0) to the end of internal write cycle (t_{WR}) is the 'effective cancellation period'. When WP is set to "H" during t_{WR} , Write operation is stopped, making it necessary to rewrite the data.

It is not necessary to wait for t_{WR} (5ms max.) after stopping the Write command by WP because the device is in standby mode.

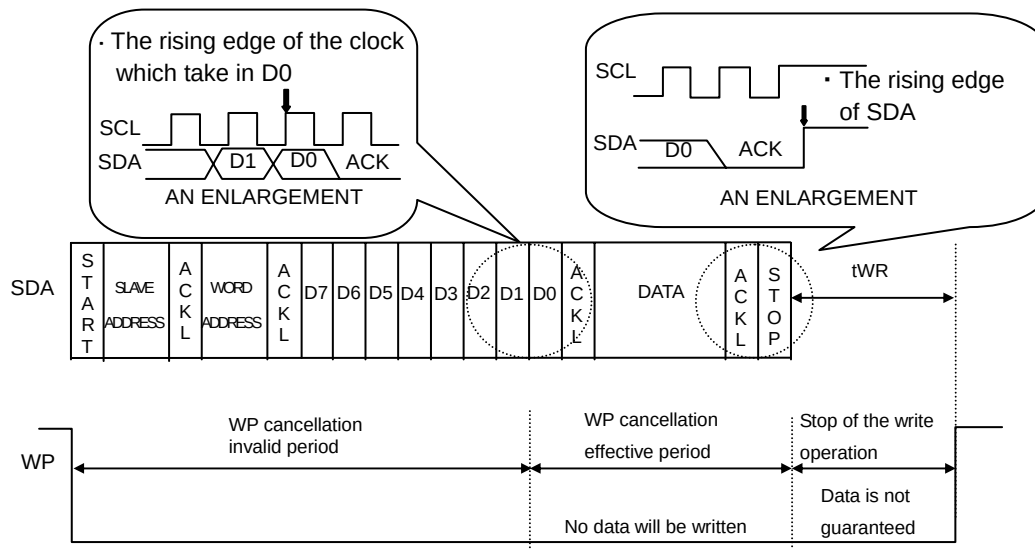


Figure 39. WP effective timing

●Command cancellation from the START and STOP conditions

Command input is canceled by successive inputs of START and STOP conditions. (Refer to Figure 40)

However, during ACK or data output, the device may set the SDA line to Low, making operation of the START and STOP conditions impossible, and thus preventing reset. In this case execute reset by software. (Refer to Figure 37)

The internal address counter will not be determined when operating the Cancel command by the START and STOP conditions during Random, Sequential or Current Read. Operate a Random Read in this case.

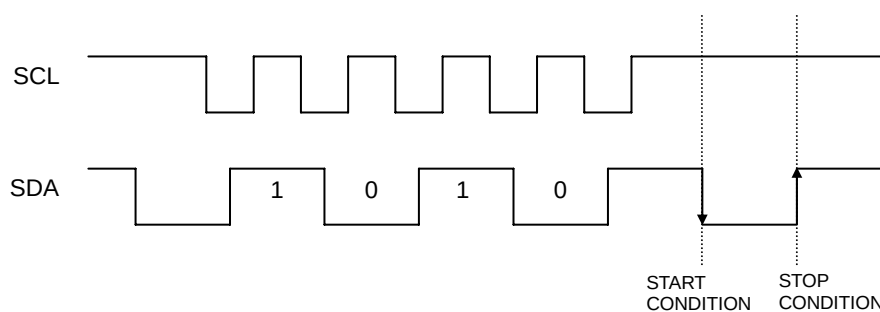


Figure 40. Command cancellation by the START and STOP conditions during input of the Slave Address

● I/O Circuit

○ SDA Pin Pull-up Resistor

A pull-up resistor is required because SDA is an NMOS open drain. Determine the resistor value of (R_{PU}) by considering the V_{IL} and I_L, and V_{OL}-I_{OL} characteristics. If a large R_{PU} is chosen, the clock frequency needs to be slow. A smaller R_{PU} will result in a larger operating current.

○ Maximum R_{PU}

The maximum of R_{PU} can be determined by the following factors.

- ① The SDA rise time determined by R_{PU} and the capacitance of the BUS line (C_{BUS}) must be less than t_R.

In addition, all other timings must be kept within the AC specifications.

- ② When the SDA BUS is High, the voltage A at the SDA BUS is determined from the total input leakage (I_L) of all devices connected to the BUS. R_{PU} must be higher than the input High level of the microcontroller and the device, including a noise margin 0.2V_{CC}.

$$V_{CC} - I_L R_{PU} - 0.2V_{CC} \geq V_{IH}$$

$$\therefore R_{PU} \leq \frac{0.8V_{CC} - V_{IH}}{I_L}$$

Examples: When V_{CC} = 3V, I_L = 10μA, V_{IH} = 0.7V_{CC}
According to ②

$$R_{PU} \leq \frac{0.8 \times 3 - 0.7 \times 3}{10 \times 10^{-6}} \\ \leq 300 \text{ [k}\Omega\text{]}$$

○ Minimum R_{PU}

The minimum value of R_{PU} is determined by following factors.

- ① Meets the condition that V_{OLMAX} = 0.4V, I_{OLMAX} = 3mA when the output is Low.

$$\frac{V_{CC} - V_{OL}}{R_{PU}} \leq I_{OL}$$

$$\therefore R_{PU} \geq \frac{V_{CC} - V_{OL}}{I_{OL}}$$

- ② V_{OLMAX} = 0.4V must be lower than the input Low level of the microcontroller and the EEPROM including the recommended noise margin of 0.1V_{CC}.

$$V_{OLMAX} \leq V_{IL} - 0.1V_{CC}$$

$$R_{PU} \geq \frac{3 - 0.4}{3 \times 10^{-3}} \\ \geq 867 \text{ [}\Omega\text{]}$$

and $V_{OL} = 0.4 \text{ [V]}$
 $V_{IL} = 0.3 \times 3$
 $= 0.9 \text{ [V]}$

so that condition ② is met

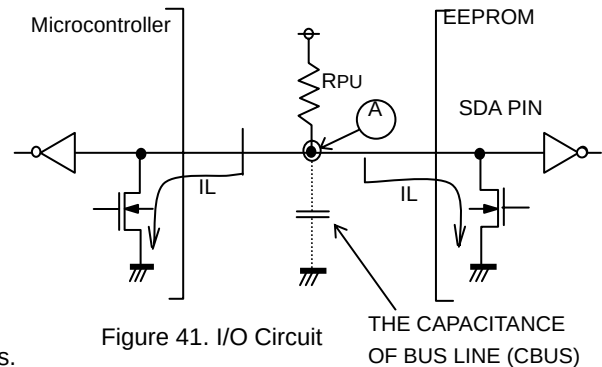


Figure 41. I/O Circuit

THE CAPACITANCE OF BUS LINE (CBUS)

○ SCL Pin Pull-up Resistor

When SCL is controlled by the CMOS output the pull-up resistor at SCL is not required.

However, should SCL be set to Hi-Z, connection of a pull-up resistor between SCL and V_{CC} is recommended.

Several kΩ are recommended for the pull-up resistor in order to drive the output port of the microcontroller.

● A0, A1, A2, WP Pin connections

○ Device Address Pin (A0, A1, A2) connections

The status of the device address pins is compared with the device address sent by the Master. One of the devices that is connected to the identical BUS is selected. Pull up or down these pins or connect them to V_{CC} or GND. Pins that are not used as device address (N.C.Pins) may be High, Low, or Hi-Z.

○ W/P Pin connection

The WP input allows or prohibits write operations. When WP is High, only Read is available and Write to all address is prohibited. Both Read and Write are available when WP is Low.

In the event that the device is used as a ROM, it is recommended that the WP input be pulled up or connected to V_{CC}.

When both READ and WRITE are operated, the WP input must be pulled down or connected to GND or controlled.

●Microcontroller connection

○Concerning Rs

The open drain interface is recommended for the SDA port in the I²C BUS. However, if the Tri-state CMOS interface is applied to SDA, insert a series resistor (Rs) between the SDA pin of the device and the pull up resistor R_{PU} is recommended, since it will serve to limit the current between the PMOS of the microcontroller, and the NMOS of the EEPROM. Rs also protects the SDA pin from surges. Therefore, Rs is able to be used though open drain in/out of the SDA port.

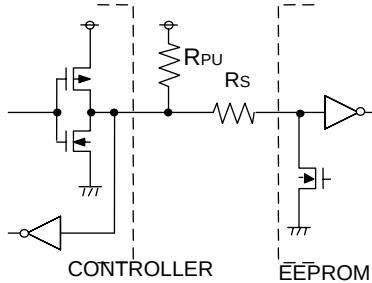


Figure 42. I/O Circuit

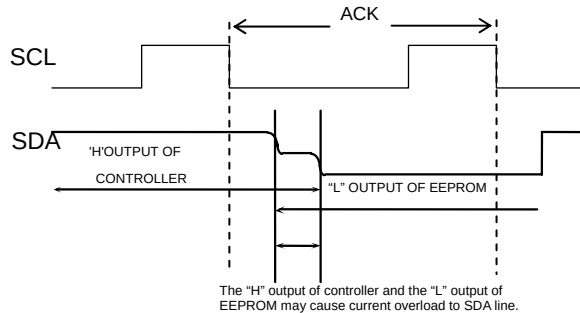


Figure 43. Input/Output Collision Timing

○Rs Maximum

The maximum value of Rs is determined by following factors.

- ①SDA rise time determined by R_{PU} and the capacitance value of the BUS line (CBUS) of SDA must be less than t_R. In addition, the other timings must be within the timing conditions of the AC.
- ②When the output from SDA is Low, the voltage of the BUS at ④ is determined by R_{PU}, and Rs must be lower than the input Low level of the microcontroller, including recommended noise margin (0.1V_{CC}).

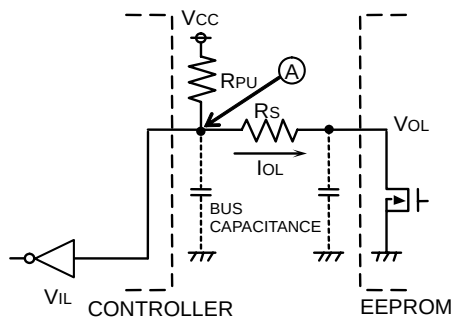


Figure 44. I/O Circuit

$$\frac{(V_{CC}-V_{OL}) \times R_S}{R_{PU}+R_S} + V_{OL} + 0.1V_{CC} \leq V_{IL}$$

$$\therefore R_S \leq \frac{V_{IL}-V_{OL}-0.1V_{CC}}{1.1V_{CC}-V_{IL}} \times R_{PU}$$

Examples : When V_{CC}=3V V_{IL}=0.3V_{CC} V_{OL}=0.4V R_{PU}=20kΩ

$$\text{According to ② } R_S \leq \frac{0.3 \times 3 - 0.4 - 0.1 \times 3}{1.1 \times 3 - 0.3 \times 3} \times 20 \times 10^3 \leq 1.67 \text{ [k}\Omega\text{]}$$

○Rs Minimum

The minimum value of Rs is determined by the current overload during BUS conflict.

Current overload may cause noises in the power line and instantaneous power down.

The following conditions must be met, where "I" is the maximum permissible current, which depends on the V_{CC} line impedance as well as other factors. "I" current must be less than 10mA for EEPROM.

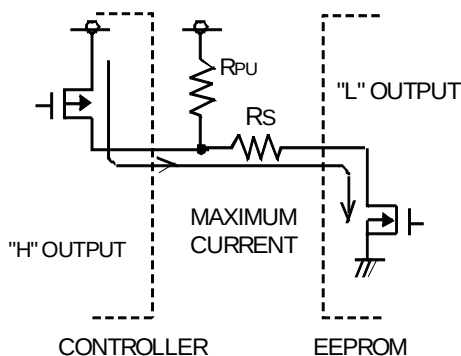


Figure 45. I/O Circuit

$$\frac{V_{CC}}{R_S} \leq I$$

$$\therefore R_S \geq \frac{V_{CC}}{I}$$

Examples: When V_{CC}=3V, I=10mA

$$R_S \geq \frac{3}{10 \times 10^{-3}} \geq 300 \text{ [}\Omega\text{]}$$

●I²C BUS Input / Output equivalent circuits

OInput (A0,A2,SCL)

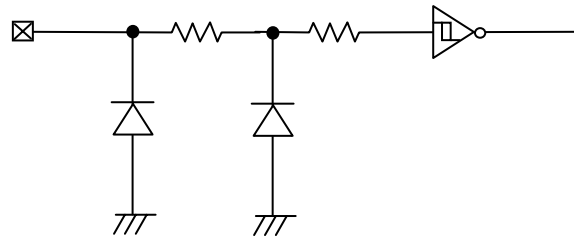


Figure 46. Input Pin Circuit

OInput / Output (SDA)

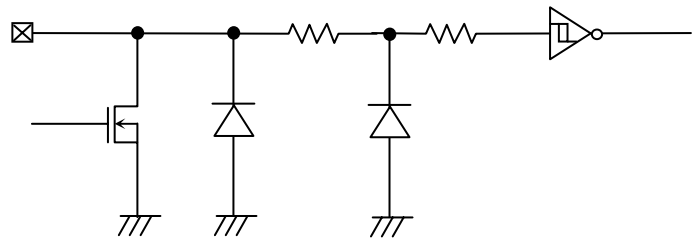


Figure 47. Input / Output Pin Circuit

OInput (A1)

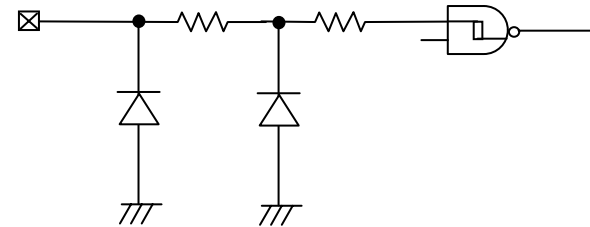


Figure 48. Input Pin Circuit

OInput (WP)

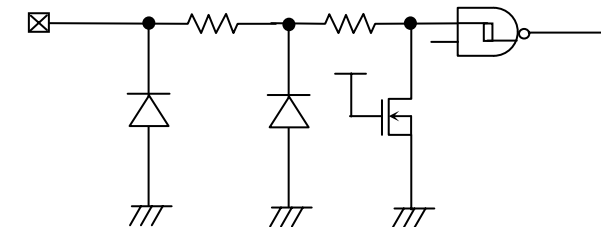


Figure 49. Input Pin Circuit

●Power Supply Notes

Vcc increases through the low voltage region where the internal circuit of IC and the microcontroller are unstable. In order to prevent malfunction, the IC has P.O.R and LVCC functionality. During power up, ensure that the following conditions are met to guaranty P.O.R. and LVCC operability.

1. "SDA='H'" and "SCL='L' or 'H'".
2. Follow the recommended conditions of tR, tOFF, Vbot so that P.O.R. will be activated during power up.

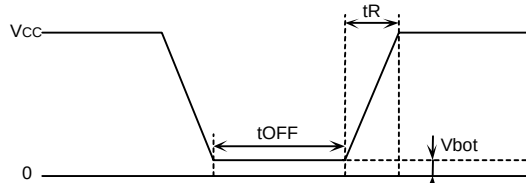


Figure 50. Rise waveform diagram

Recommended conditions of tR, tOFF, Vbot

tR	tOFF	Vbot
Below 10ms	Above 10ms	Below 0.3V
Below 100ms	Above 10ms	Below 0.2V

3. Prevent SDA and SCL from being "Hi-Z".

In case that condition 1 and/or 2 cannot be met, take following actions.

- A) If unable to keep Condition 1 (SDA is "Low" during power up)

→Make sure that SDA and SCL are "High" as in the figure below.

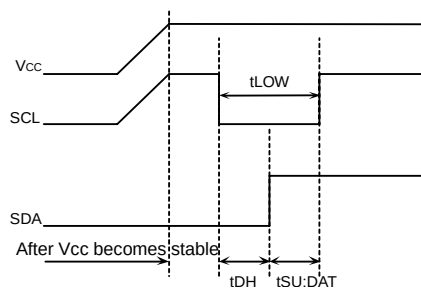


Figure 51. SCL='H' and SDA='L'

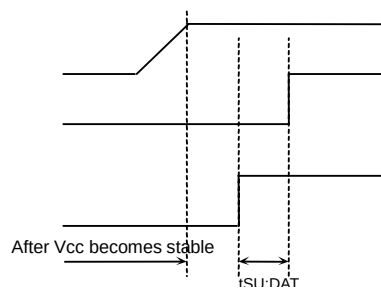


Figure 52. SCL='L' and SDA='L'

- B) If unable to keep Condition 2

→After the power stabilizes, execute software reset. (See Figure 37)

- C) If unable to keep either Condition 1 or 2

→Follow Instruction A first, then B

●LVCC Circuit

The LVCC circuit prevents Write operation at low voltage and prevents inadvertent writing. A voltage below the LVCC voltage (1.2V typ.) prohibits Write operation.

●Vcc Noise

○Bypass Capacitor

Noise and surges on the power line may cause abnormal function. It is recommended that bypass capacitors (0.1μF) be attached between Vcc and GND externally.

●Notes for Use

- 1) Described numeric values and data are design representative values, and the values are not guaranteed.
- 2) We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our LSI.
- 3) Absolute maximum ratings
If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.
- 4) GND electric potential
Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is lower than that of GND terminal.
- 5) Heat design
In consideration of permissible dissipation in actual use condition, carry out heat design with sufficient margin.
- 6) Terminal to terminal short circuit and wrong packaging
When to package LSI on to a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of short circuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.
- 7) Use in a strong electromagnetic field may cause malfunction, therefore, evaluate design sufficiently

Status of this document

The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document formal version takes priority.

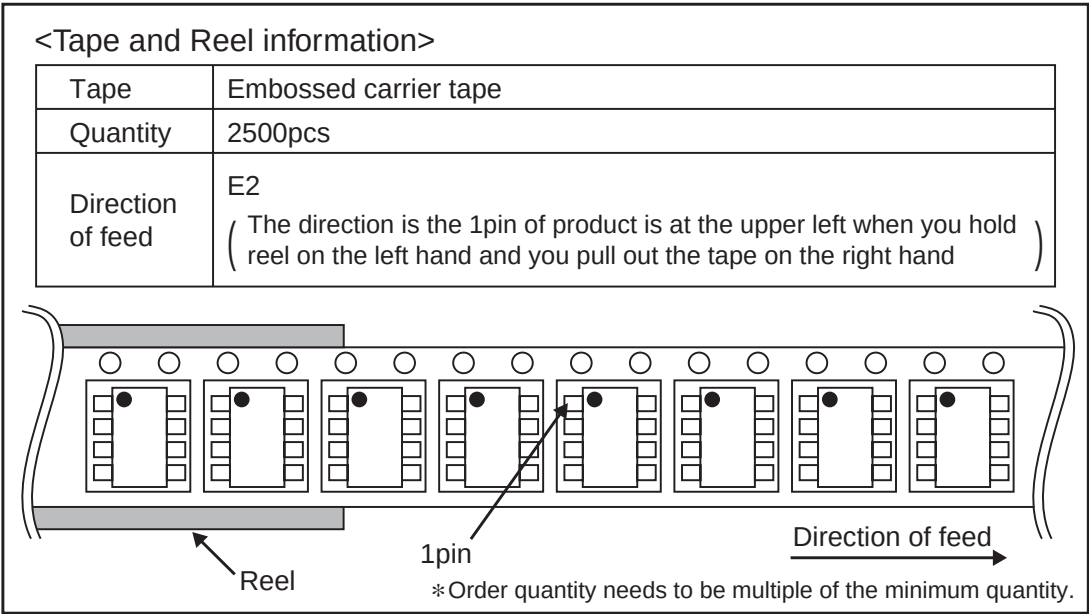
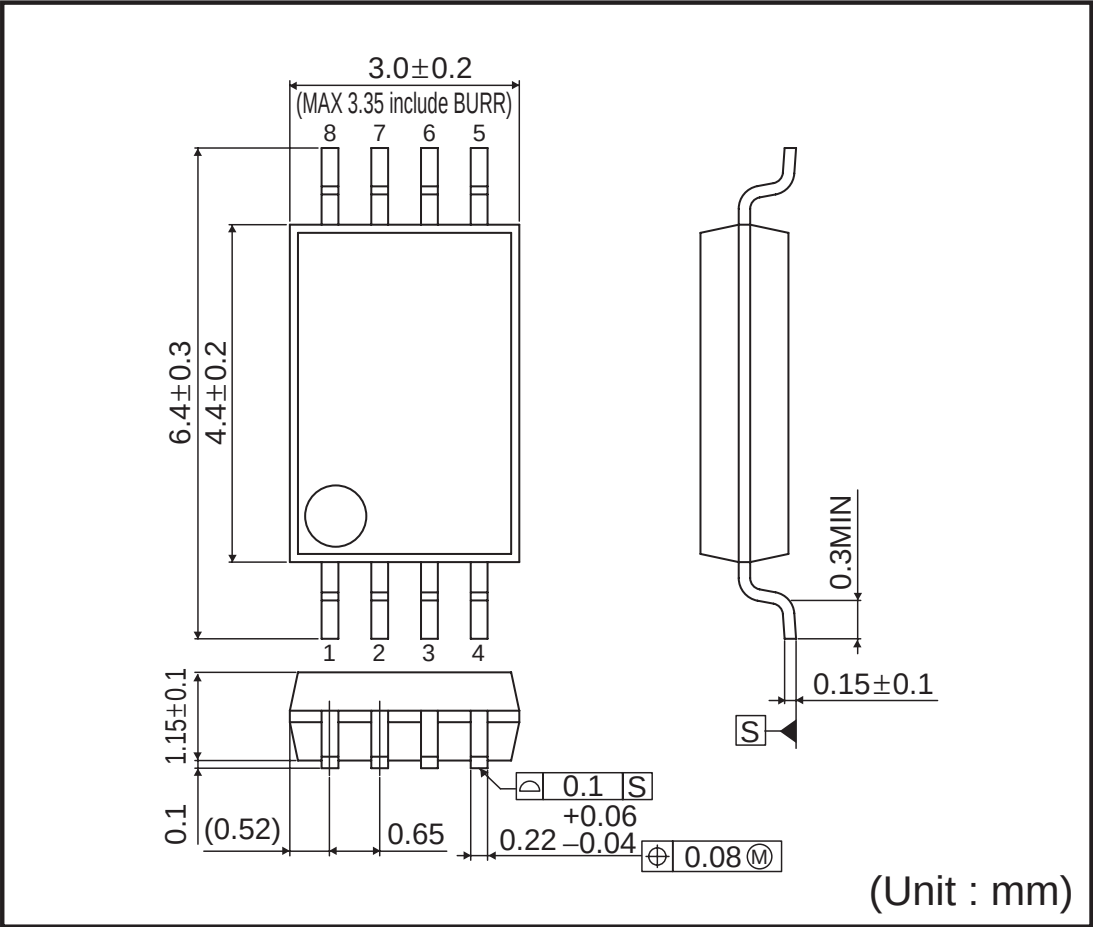
●Ordering Information

Product Code Description

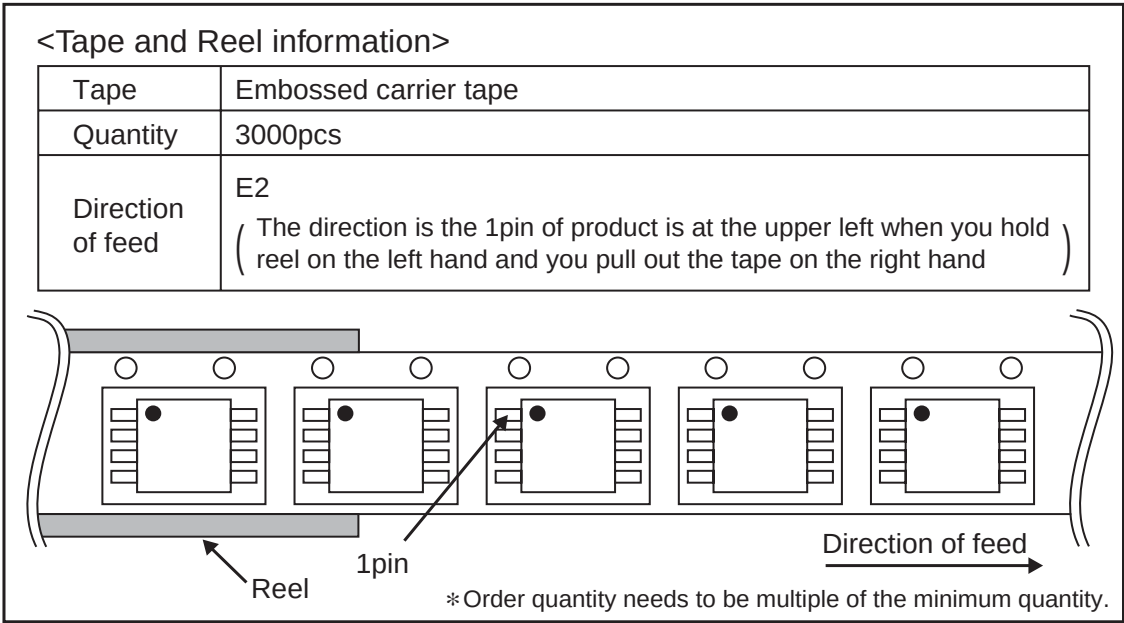
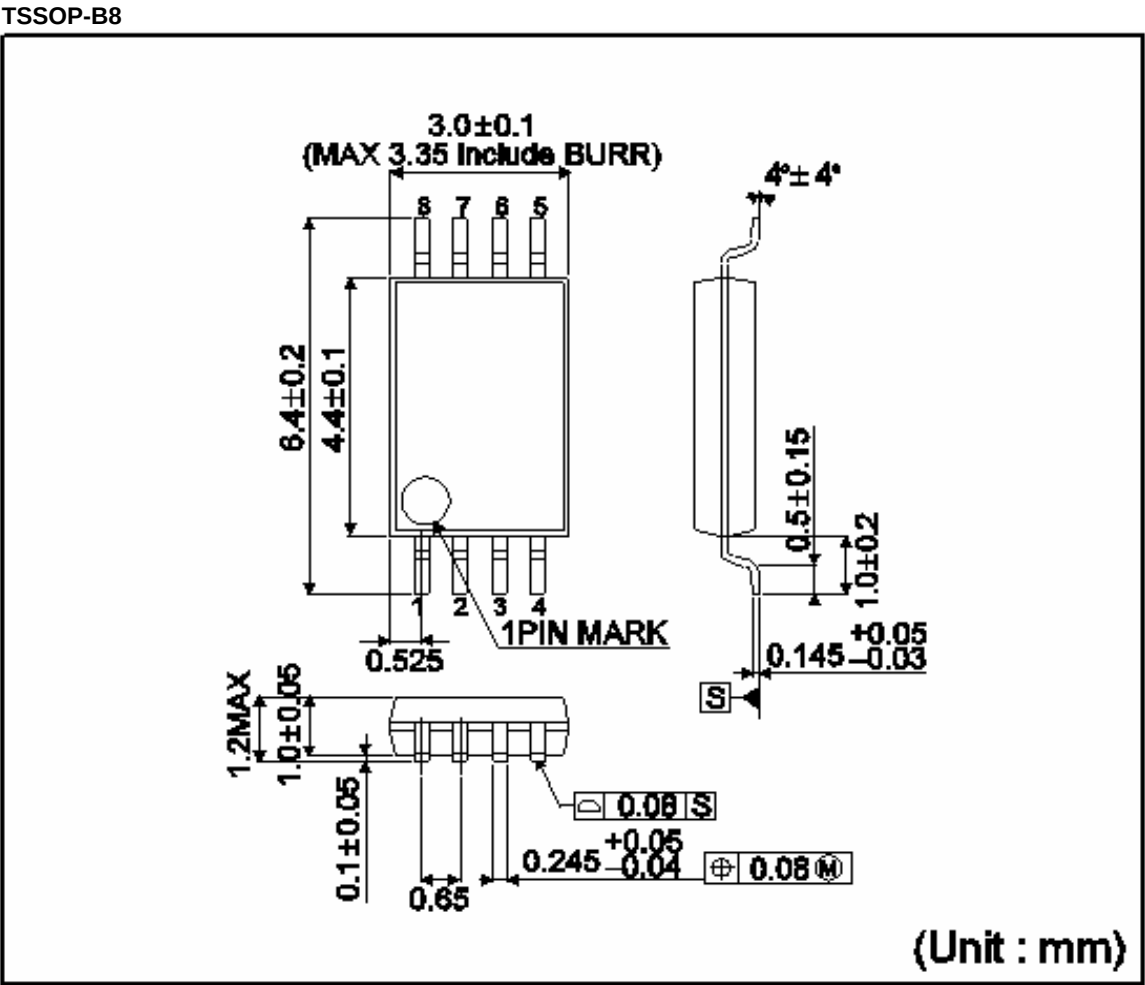
	B	R	3	4	L	0	2	x	x	x	-	W	x	x
BUS type														
34 : I ² C														
Operating temperature/ Power source Voltage														
-40°C to +85°C/ 1.7V to 5.5V														
Capacity														
02=2K														
Package														
FV : SSOP-B8														
FVT : TSSOP-B8														
Double Cell														
Packaging and forming specification														
E2 : Embossed tape and reel (SSOP-B8 , TSSOP-B8)														

●Physical Dimension Tape and Reel Information

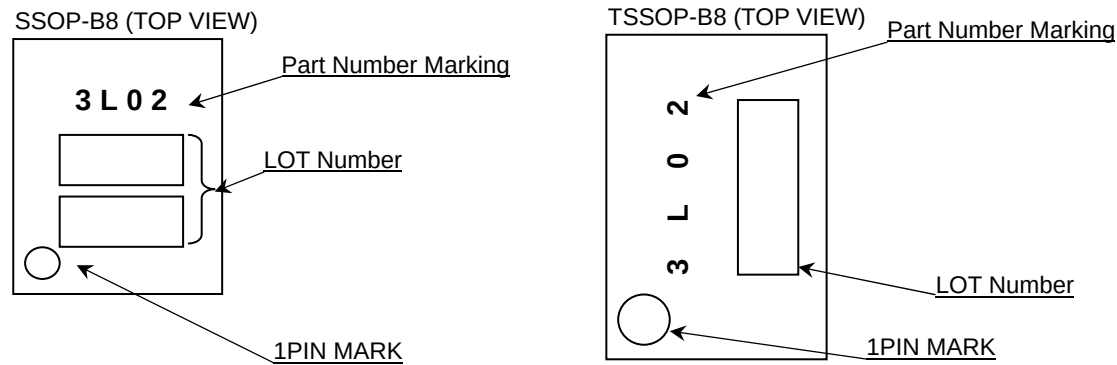
SSOP-B8



●Physical Dimension Tape and Reel Information - continued



●Marking Diagrams



●Revision History

Date	Revision	Changes
27.Aug.2012	001	New Release

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CLASS IV		CLASS III	

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