5.0V to 14V, 3.0A 1ch Buck Converter with Integrated FET

BD9859EFJ

General Description

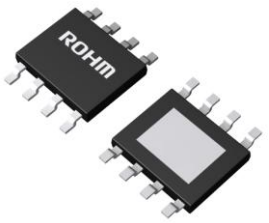
The BD9859EFJ is a high-efficiency step-down switching regulator with built-in power MOSFET switch. This device can operate over a wide range of input voltages and is flexible enough to produce output voltages from 1.0V up to 70% of the supply voltage, depending on the external resistor values. The built-in N-Channel FET switch has a very high absolute maximum rating of 15V and is capable of handling current of up to 3.0 A. The implementation of current-mode control for this switching regulator gives the advantage of a high-speed load response. The device has a fixed switching frequency of 750kHz, allowing the use of smaller output inductors and capacitors. Also, its phase compensation network, although external to the device, is very simple and requires a minimal number of components, making the construction of a compact power supply really easy.

Key Specifications

- Input Voltage Range: 5.0V to 14V
- Output Voltage Range: 1.0V to 0.7xVCC
- Output Current: 3.0A (Max)
- Switching Frequency: 750kHz(Typ)
- High Side Nch FET ON-Resistance 100mΩ(Typ)
- Nch FET ON-Resistance for Pew-Charge: 5Ω(Typ)
- Standby Current: 0μA (Typ)
- Operating Temperature Range: -40°C to +85°C

Package

W (Typ) x D (Typ) x H (Max)



HTSOP-J8
4.90mm x 6.00mm x 1.00mm

Features

- 1.0V±1.0% Feedback Voltage
- Built-In Soft Start Function
- Built-In Over Current Protect, Under Voltage Lockout, and Thermal Shutdown Circuits
- ON/OFF Control through EN Pin

Applications

Generally for Household Equipment with 9V/12V Lines

Typical Application Circuit

(Input 12V, Output 5.0V/ 2.5A)

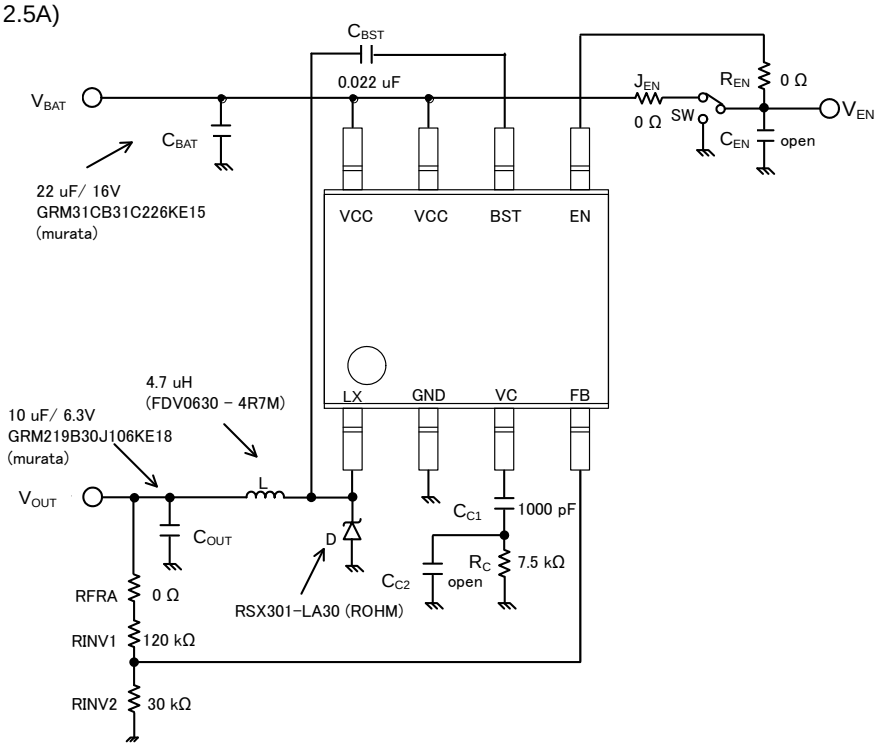


Figure 1. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

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Pin Configuration

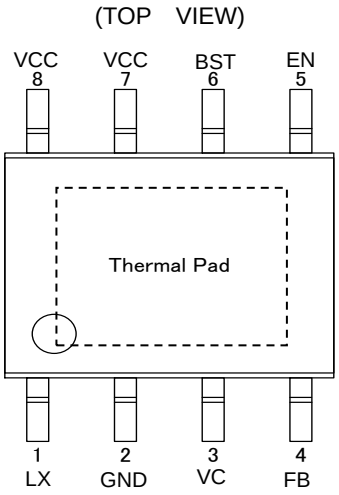

Figure 2. Pin Configuration

Pin Description

Pin No.	Pin Name	Function
1	LX	Power switch node
2	GND	Ground pin
3	VC	Error amplifier output pin
4	FB	Feedback pin
5	EN	Stand-by ON/OFF pin
6	BST	High-side gate driver pin
7	VCC	Voltage input pin
8	VCC	Voltage input pin

Block Diagram

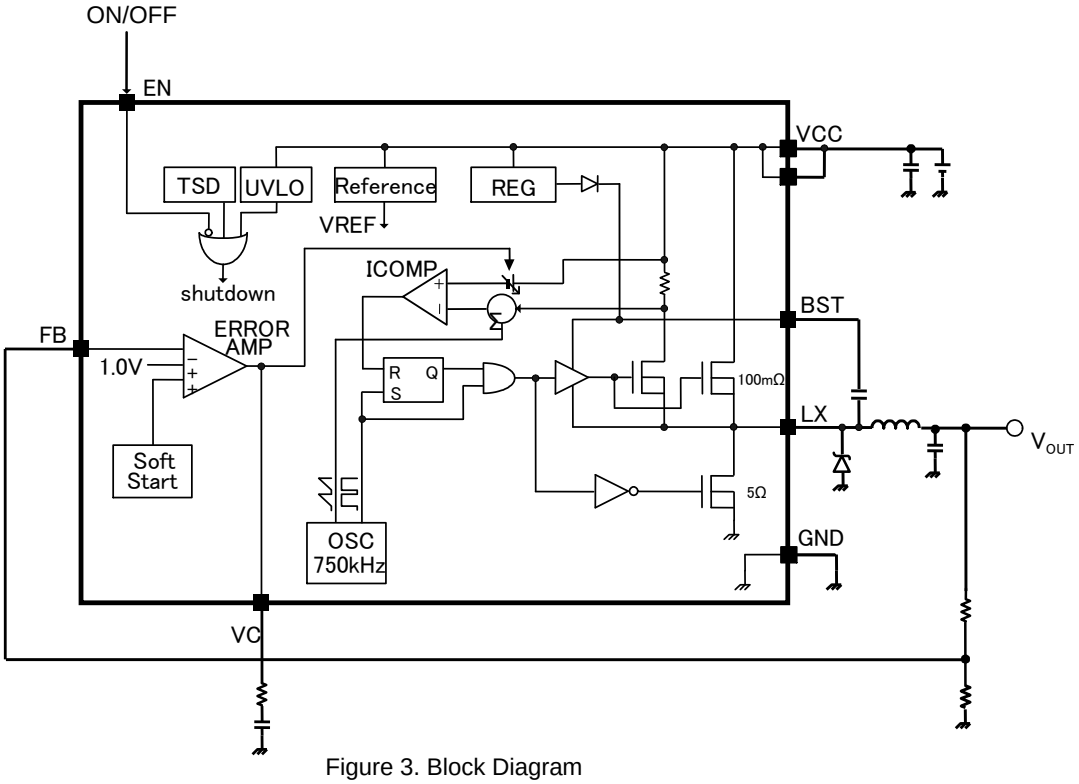

Figure 3. Block Diagram

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Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	15	V
BST Pin Voltage	V_{BST}	22	V
BST-LX Voltage	ΔV_{BST}	7	V
EN Pin Voltage	V_{EN}	15	V
LX Pin Voltage	V_{LX}	15	V
FB Pin Voltage	V_{FB}	7	V
VC Pin Voltage	V_C	7	V
High-Side FET Drain Current	I_{DH}	3	A
Power Dissipation	Pd	3.76 (Note 1)	W
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

(Note 1) When mounted on a 4-layer PCB of 70mm x 70mm x 1.6 mm. Reduce by 30.08mW/°C for Ta over 25°C.

Caution: An excess in the absolute maximum ratings, such as supply voltage, operating temperature, etc., can damage the device, making it impossible to identify the cause, such as a short circuit or an open circuit. If there is any possibility of exposure over the rated values, please consider adding circuit protection devices such as fuses.

Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	5.0 to 14	V
Output Voltage	V_{OUT}	1.0 to 0.7xVCC	V

Electrical Characteristics (Unless otherwise specified, Ta=25°C, V_{CC}=12V, V_O=5V, V_{EN}=3V)

Parameter		Symbol	Rating			Unit	Conditions
			Min	Typ	Max		
【Circuit Current】							
Stand-by Circuit Current		I_{ST}	–	0	10	μA	V_{EN}=0V
Circuit Current		I_{CC}	–	2.8	5.6	mA	V_{FB}=1.2V
【Under Voltage Lock Out (UVLO) Block】							
UVLO Threshold Voltage		V_{UV}	4.2	4.4	4.6	V	
Hysteresis		V_{UVHY}	-	200	400	mV	
【Oscillator Block】							
Oscillation Frequency		f_{OSC}	675	750	825	kHz	
Maximum Duty Cycle		D_{MAX}	75	85	95	%	
【Error Amp】							
FB Threshold Voltage		V_{FB}	0.990	1.000	1.010	V	
Input Bias Current		I_{FB}	-1.0	0	+1.0	μA	V_{FB}=0V
Error Amp Transconductance		G_M	70	140	280	μA/V	I_C=±10μA,V_C=1.5V
Soft Start Period		t_{SOFT}	2.0	4.0	6.0	ms	
【Output】							
LX High Side FET ON-Resistance		R_{ON_H}	–	100	200	mΩ	
LX Low Side ON-Resistance		R_{ON_L}	–	5	10	Ω	
OCP Detection Current		I_{OCP}	3.5	5.5	–	A	
【CTL】							
EN Threshold Voltage	ON	V_{EN_ON}	2.0	–	14	V	
	OFF	V_{EN_OFF}	-0.3	–	+0.3	V	
EN Pin Input Current		I_{EN}	2.5	7.5	15	μA	V_{EN}=3V

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Typical Performance Curves

Unless otherwise specified, Ta=25°C, V_{CC}=12V, V_O=5V, V_{EN}=3V)

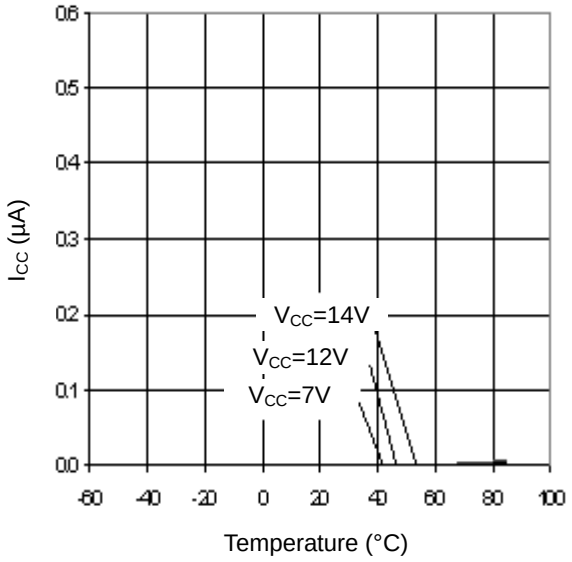

Figure 4. Standby Circuit Current vs Temperature

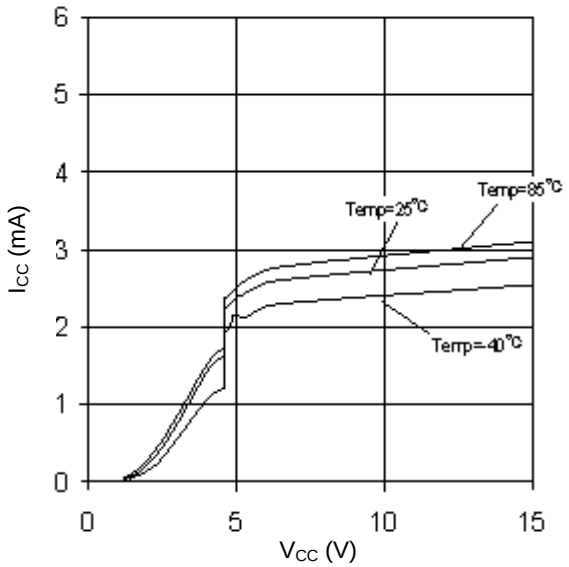

Figure 5. Circuit Current vs V_{CC}

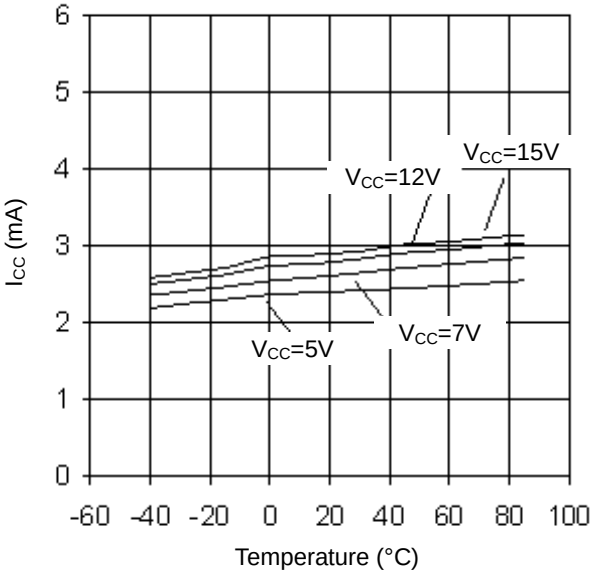

Figure 6. Circuit Current vs Temperature

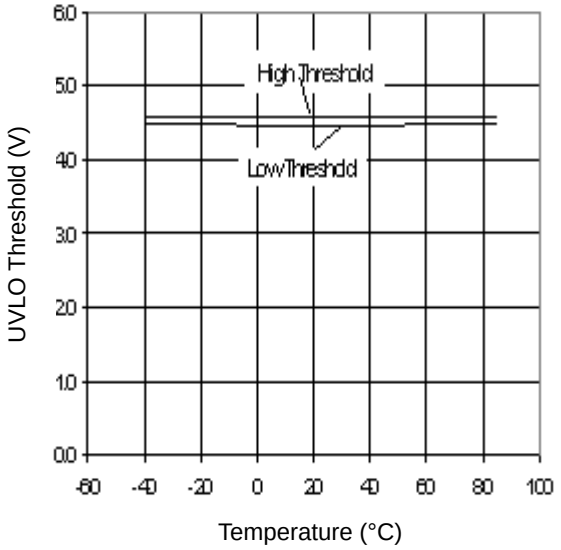

Figure 7. UVLO Threshold Voltage vs Temperature

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Typical Performance Curves - continued

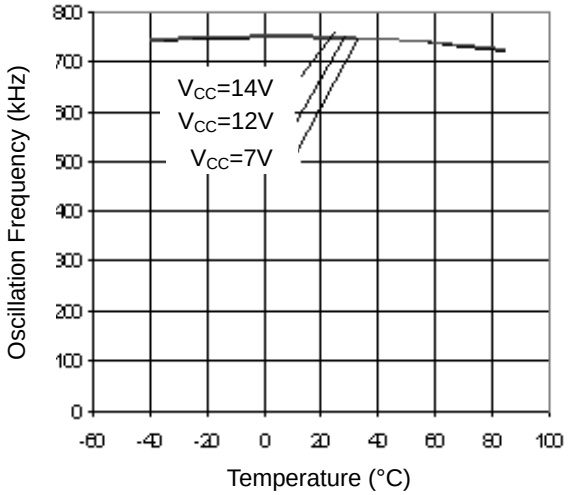

Figure 8. Oscillation Frequency vs Temperature

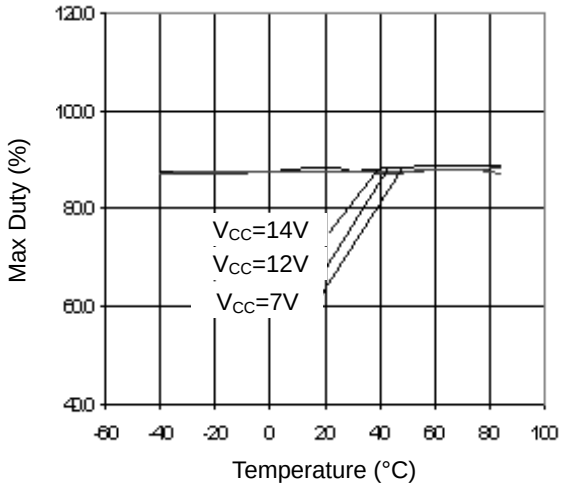

Figure 9. Maximum Duty Cycle vs Temperature

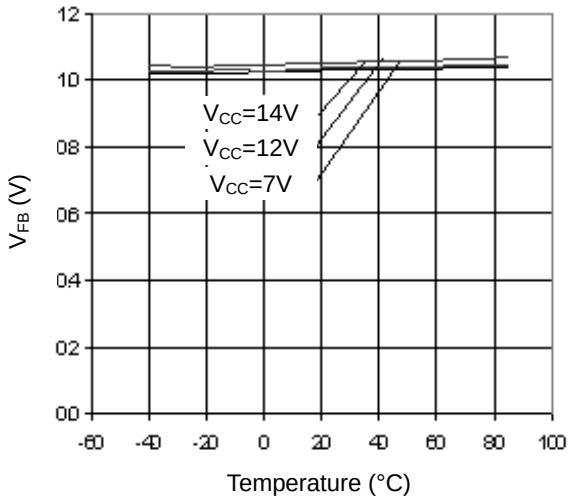

Figure 10. FB Threshold Voltage vs Temperature

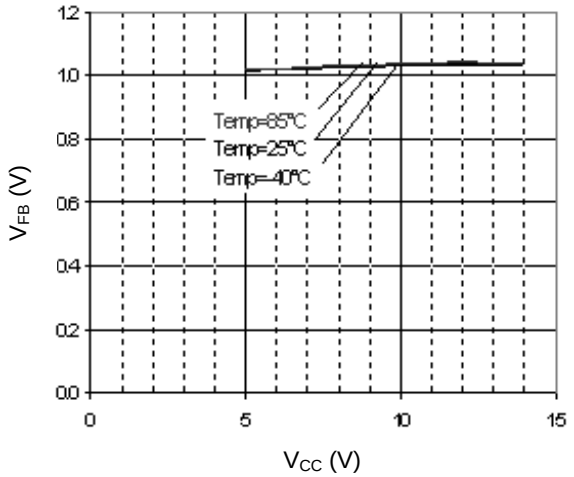

Figure 11. FB Threshold Voltage vs V_{CC}

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Typical Performance Curves - continued

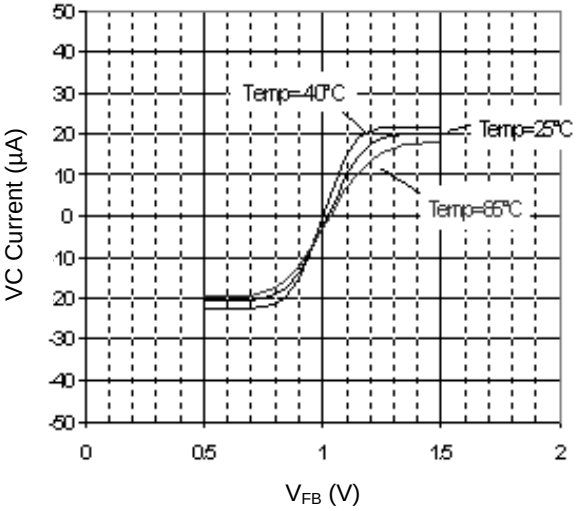

Figure 12. VC Current vs FB Voltage

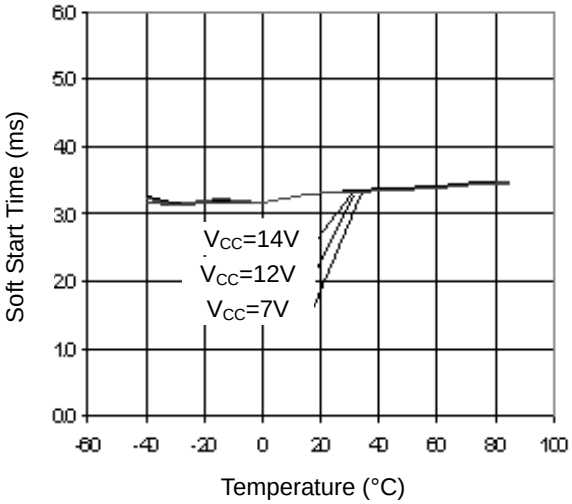

Figure 13. Soft Start Time vs Temperature

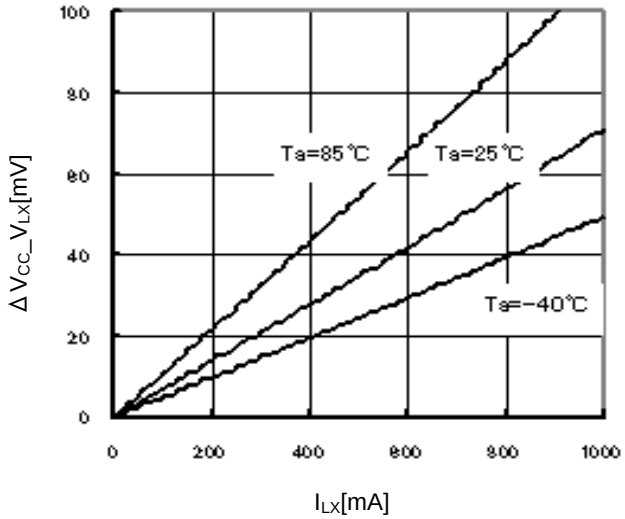

Figure 14. High Side FET ON-Resistance Temperature Characteristics

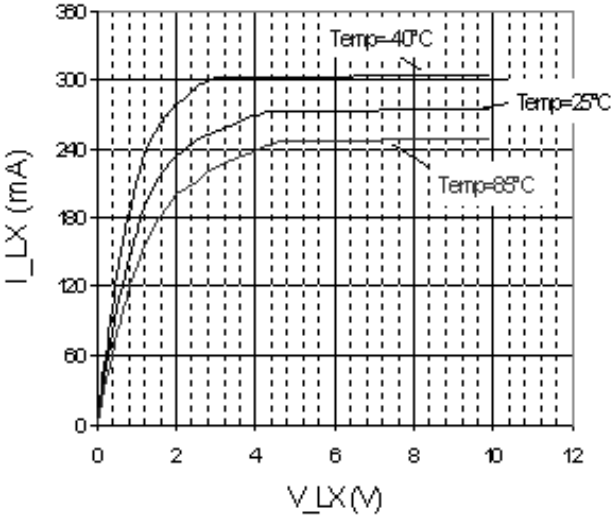

Figure 15. Low Side ON-Resistance Temperature Characteristics

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Typical Performance Curves - continued

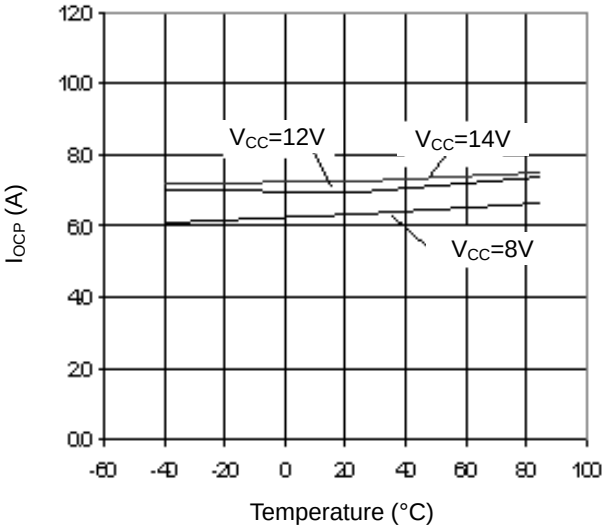

Figure 16. OCP Detect Current vs Temperature

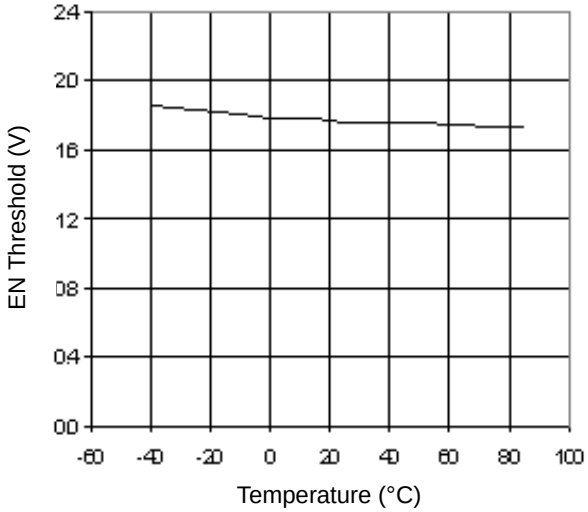

Figure 17. EN Threshold Voltage vs Temperature

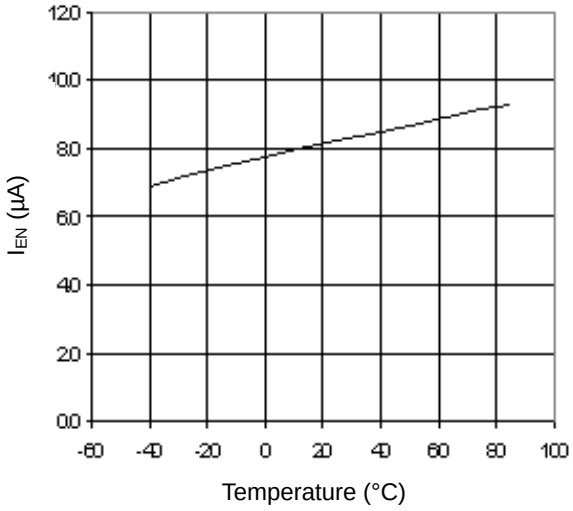

Figure 18. EN Pin Input Current vs Temperature

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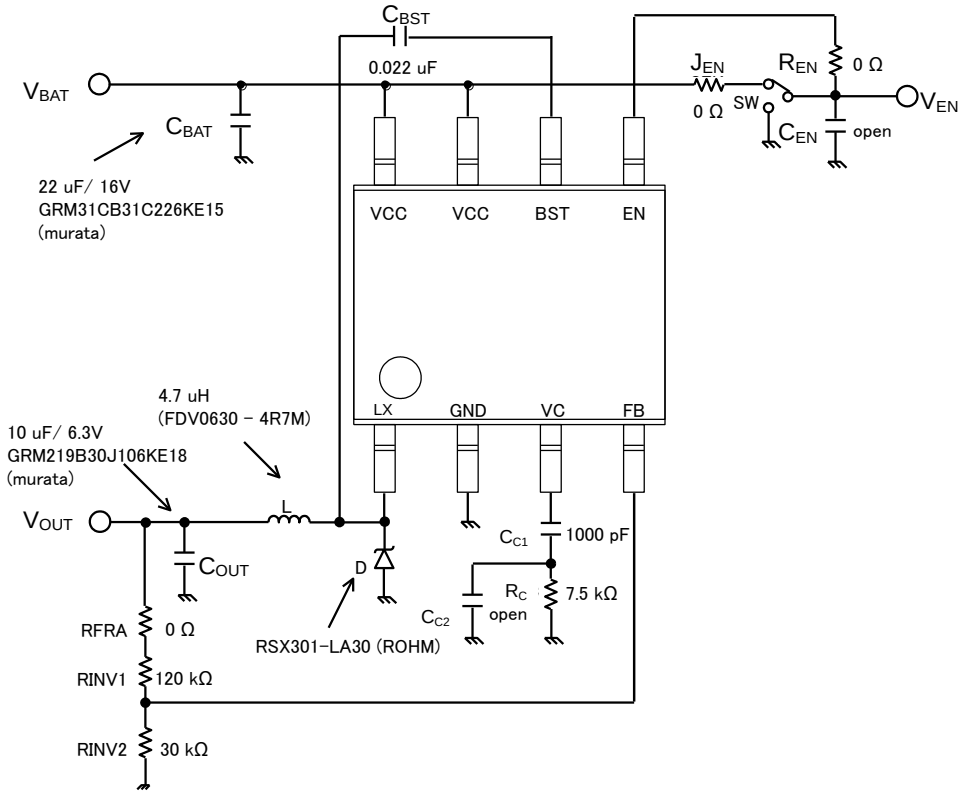
Application Information

1. Reference Application Circuit (Input 12V, Output 5.0V/ 2.5A)



2. Block Description

(1) Reference
This block generates the 1.0V internal reference voltage of the Error Amp.

(2) REG
This block produces the gate drive voltage of the power transistor and a 5V regulated internal power supply.

(3) OSC
This block creates the 750 kHz internal clock signal.

(4) Soft Start
The soft-start circuit slows down the rise of the output voltage during start-up to prevent inrush current. The soft-start period of 4ms is internally set, allowing the Error Amp reference voltage to reach 1.0V and the output to reach the set voltage level only after 4 ms from pulling the EN pin high.

(5) ERROR AMP
The error amplifier senses the output voltage, compares it to the 1.0V internal reference voltage, and produces the control signal for the ICOMP block. The output of this error amplifier appears at the VC pin, where a capacitor and a resistor are connected for phase compensation. (See page 13)

(6) ICOMP
This block is a Pulse-Width Modulator circuit that controls the output transistors' driver. It compares the sum of an internally generated ramp, and a voltage proportional to the switching current, to the output of the Error Amp, setting the width of the output pulse.

(7) Nch FET SW
This is an internal switch that powers the output through the output LC filter. It has an absolute maximum rating of 15 V and ON-Resistance of 100mΩ. Also, it has a current rating of 3.0 A, which should not be exceeded even by ripple currents.

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(8) UVLO
This is a circuit that prevents error in the device operation due to either excessive or insufficient power supply voltage. It monitors the voltage level at VCC pin and also the output of REG block. Once VCC voltage falls below 4.4V, the UVLO circuit disables the device and resets the soft-start circuit. Typical UVLO Hysteresis is 200 mV.

(9) TSD
This circuit protects the device from damages due to excessive heat and power dissipation. When the TSD circuit is triggered by temperature exceeding the 150°C Maximum Junction Temperature, it shuts down the device. Once temperature falls below the threshold set by a hysteresis, the device resumes operation.

(10) EN
The voltage level at the EN pin controls whether the device is ON or OFF. The device is ON if the voltage at EN is 2.0V or higher and is OFF when EN pin is at 0V or open. A 400kΩ pull-down resistor is internally connected to the EN pin.

3. Application Performance Characteristics(Example of Reference Application Circuit)

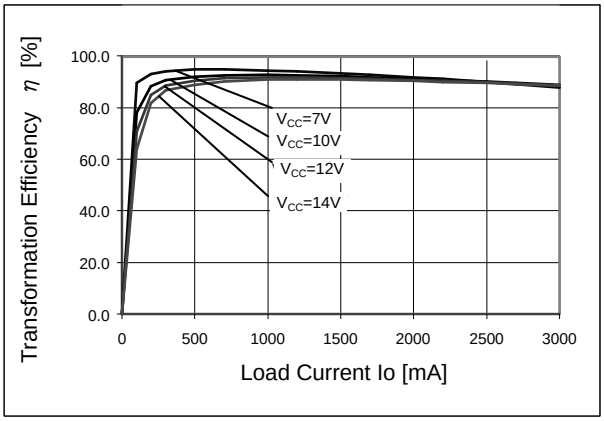

Figure 19. Electric Power Conversion Rate

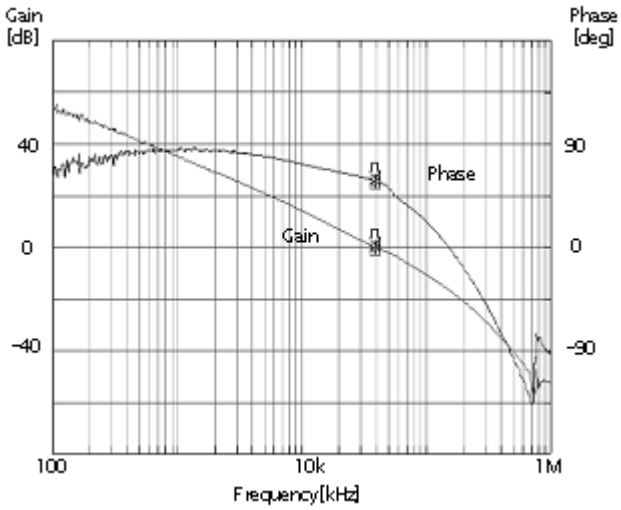

Figure 20. Frequency Response Characteristics（I_O=1.5A）

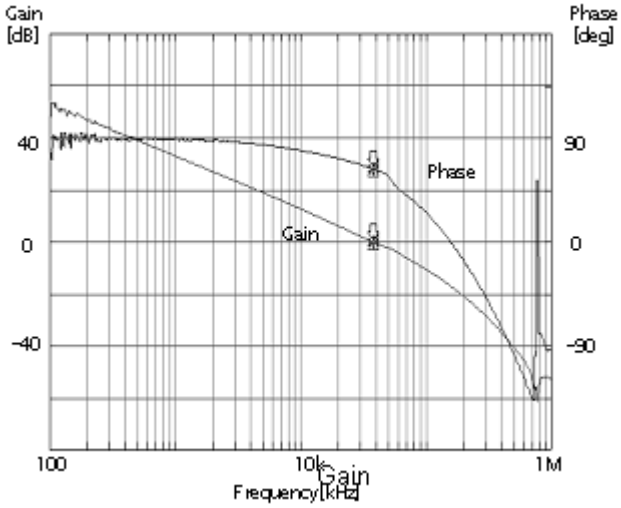

Figure 21. Frequency Response Characteristics （I_O=3.0A）

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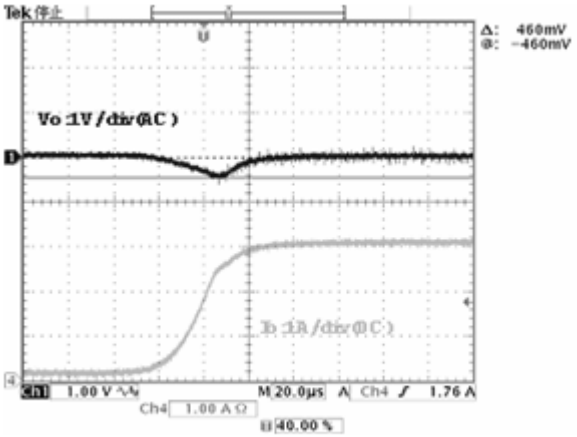

Figure 22. Load Response Characteristics
（I_O=0A to 3A）

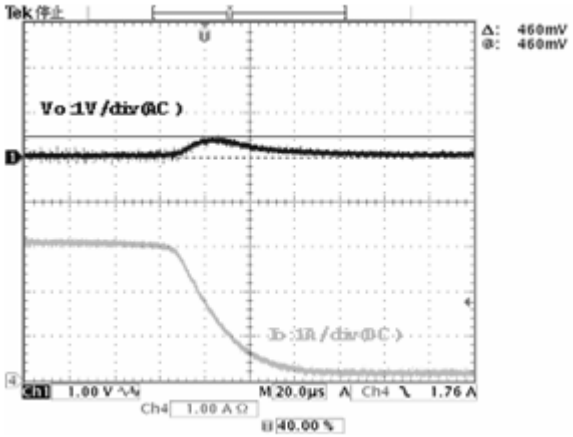

Figure 23. Load Response Characteristics
（I_O=3A to 0A）

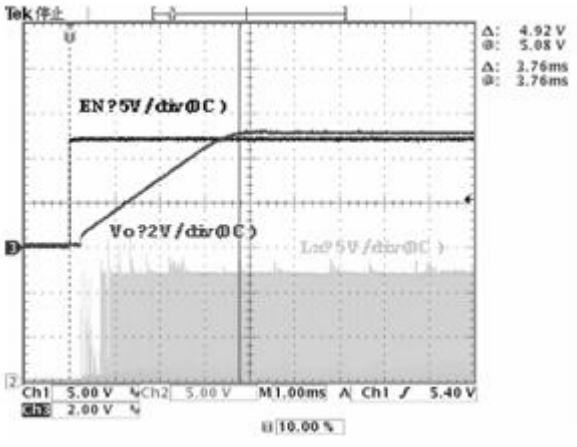

Figure 24. Operation Waveform

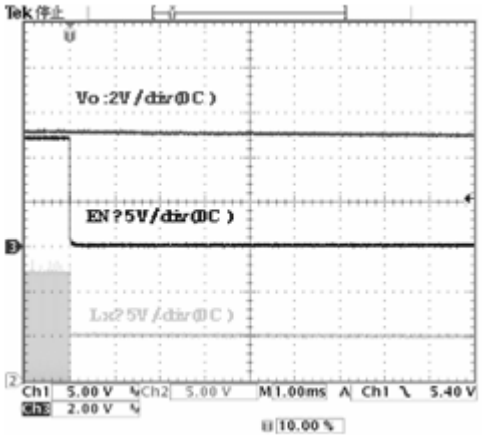

Figure 25. Stop Waveform

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4. Evaluation Board Pattern (Reference)

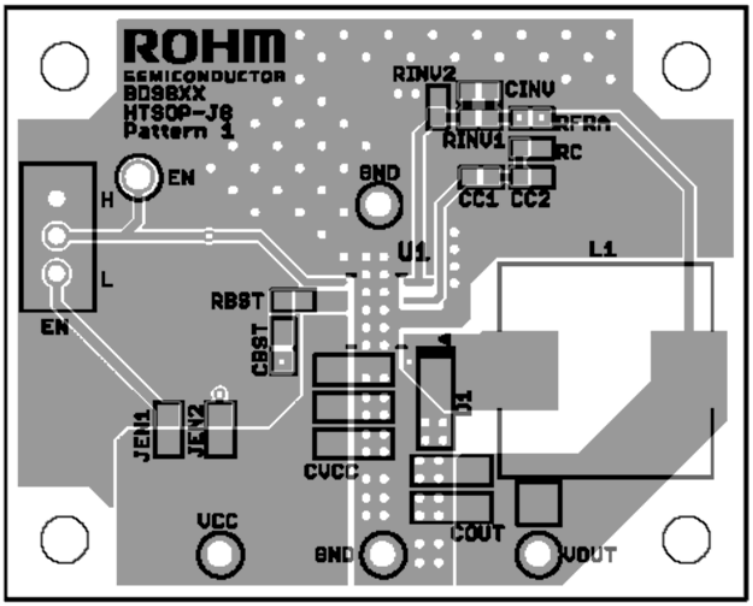

Figure 26. Evaluation Board Pattern

(1) Make the heat sink plate of the bottom layer a plane of low impedance.
(2) Because large currents flow into the lines of VCC, LX, PGND, make the patterns as wide as possible.

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5. Guide in Selecting External Components

(1) Inductor

To continuously supply current to a load, this DC-DC converter needs an LC filter that will smoothen its output voltage. The shield-type inductor is the recommended type of inductor for this purpose. The inductor that will be used should be rated for the peak current, Ipeak, shown below and should have a low DC resistance.

$$I_{PEAK} = I_{OUT} + \Delta I_L/2 \quad [A] \qquad (1)$$

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f} \quad [A] \qquad (2)$$

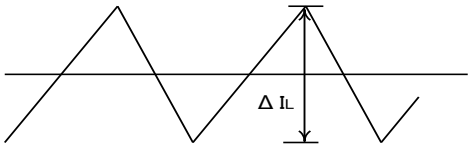


Figure 27. Inductor Current

where:
η is the Efficiency
ΔI_L is the Output Ripple Current
f is the Switching Frequency

The size of the inductor greatly influences output ripple so careful selection of inductance value should be observed. As seen in the expression for ripple current, ΔI_L, below, choosing a large value of inductance makes ΔI_L smaller. The effect will also be the same when higher switching frequency is chosen. As a guide, select the inductance suitable for inductor current that is 20% to 50% higher that maximum. Sufficient margin is necessary to avoid the inductor from going to magnetic saturation when the current through it exceeds its current rating. Magnetic saturation of the inductor can cause decline in the efficiency and oscillations on the output.

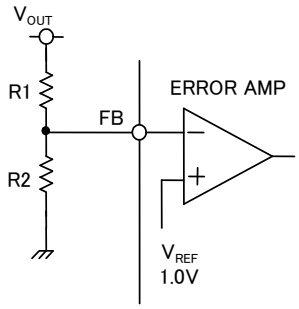
(2) Output Capacitor

A low-ESR ceramic capacitor is the recommended type of capacitor for reducing output ripple voltage. Aside from DC bias characteristics, also consider the output ripple in selecting the appropriate output capacitor. Ensure that the maximum rating of the capacitor has enough margin for the output ripple voltage, which is determined by the following:

$$Vpp = \Delta I_L \times \frac{1}{2\pi \times f \times C_O} + \Delta I_L \times R_{ESR} \quad [V] \qquad (3)$$

(3) Output Voltage Setting

The ERROR AMP's internal reference voltage is 1.0V. The output voltage of the BD9876EFJ DC-DC converter can be determined by the following:



$$Vo = \frac{(R1 + R2)}{R2} \times 1.0 \quad [V] \qquad (4)$$

Figure 28. How to Set Feedback Resistors

(4) Boost Capacitor

Connect a laminated ceramic capacitor with value 0.022μF between the BST and LX pins.

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(5) Phase Compensation

The stability and the responsiveness of the power supply are controlled through the VC pin, which is the output of the Error Amp. The combination of poles and zeroes that determine these two characteristics is set by the combination of resistors and capacitors connected in series to the VC pin, which, from the reference application circuit on Page 8, are C_{C1}, C_{C2}, and R_C.

The DC gain of the feedback loop can be calculated using the following:

$$Adc = R_I \times G_{CS} \times A_{EA} \times \frac{V_{FB}}{V_{OUT}}$$

Where:

V_{FB} is the Feedback Voltage (1.0V)
A_{EA} is the Voltage Gain of Error Amplifier (60dB typ)
G_{CS} is the Transconductance of Current Sense Amplifier (6A/V typ)
R_l is the Output Load Resistance

There are two important poles in the control loop of this DC/DC converter.
The first occurs with/through the output resistance of Phase compensation Capacitor (C_{C1}) and error amplifier.
The other one occurs at the output capacitor and load resistor.
These poles appear in the frequency as shown below.

$$f_{p1} = \frac{G_{EA}}{2\pi \times C_{C1} \times A_{EA}}$$

$$f_{p2} = \frac{1}{2\pi \times C_{OUT} \times R_I}$$

Where

G_{EA} is the Transconductance of Error Amplifier (Typ: 140µA/V).

In the same control loop, one zero becomes important. With the zero occurring because of phase compensation capacitor C_{C1} and phase compensation resistor R_C, the following frequency appears.

$$f_{Z1} = \frac{1}{2\pi \times C_{C1} \times R_C}$$

Also, if the output capacitor's value and ESR are both big, there are cases when another important zero is present in the control loop. This is the ESR zero, which occurs due to the capacitance and ESR of the output capacitor. It exists in the following frequency.

$$f_{ZESR} = \frac{1}{2\pi \times C_{OUT} \times R_{ESR}} \qquad \text{(ESR zero)}$$

In this case, the third pole determined by the second phase compensation capacitor (C_{C2}) and phase correction resistor (R_C) is used to correct the ESR zero's effect in the loop gain. This pole exists in the frequency shown below.

$$f_{p3} = \frac{1}{2\pi \times C_{C2} \times R_C} \qquad \text{(Pole that corrects ESR zero)}$$

The goal of phase compensation design is to create a system that can obtain the necessary frequency and phase margin for the application circuit.

The cross-over frequency or the frequency at which the gain of the feedback loop becomes "0" is very important. When this frequency becomes low, line regulation and load response becomes poor and when it becomes high, on the other hand, the feedback loop becomes unstable. As a recommendation, set the cross-over frequency to be, at most, 5% of the switching frequency.

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The following are the guidelines in selecting the phase compensation elements.

(a) The phase compensation resistor (R_C) will set the cross-over frequency. Calculation of R_C's value is done using the expression below. fc is the desired cross-over frequency, which should be, at most, 5% of the device's switching frequency, fs.

$$R_C = \frac{2\pi \times C_{OUT} \times f_C}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}} < \frac{2\pi \times C_{OUT} \times 0.1 \times f_S}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}}$$

(b) The phase compensation capacitor (C_{C1}) sets the phase margin. In an application with a typical inductor value of about several µH to 20µH, the suitable phase margin can be acquired by setting the zero of the compensation network to ¼ or below of the cross-over frequency. C_{C1} can be calculated using the following expression, where R_C is the phase compensation resistor.

$$C_{C1} > \frac{4}{2\pi \times R_C \times f_C}$$

R_C is the Phase Compensation Resistor.

(c) A second phase compensation capacitor, C_{C2} is necessary if the ESR zero of the output capacitor exists somewhere below half of the switching frequency, or, in other words, if the following expression is true.

$$\frac{1}{2\pi \times C_{OUT} \times R_{ESR}} < \frac{f_S}{2}$$

In case C_{C2} will be added, match the frequency of the third pole to the frequency of ESR zero, fp3. C_{C2} is determined by:

$$C_{C2} = \frac{C_{OUT} \times R_{ESR}}{R_C}$$

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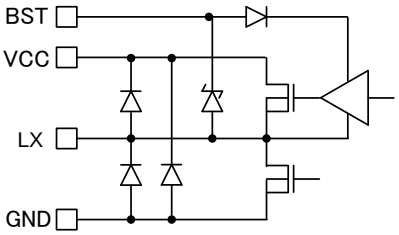
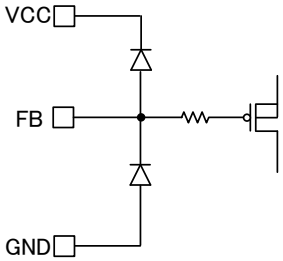
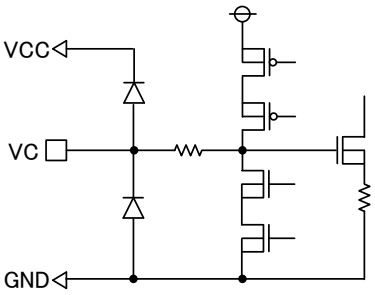
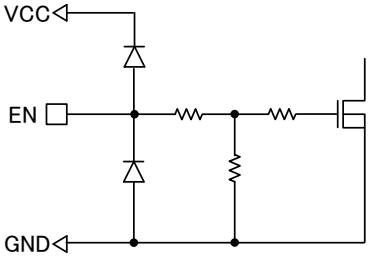
I/O Equivalent Schematic

Pin No	Pin Name	Pin Equivalent Schematic		Pin No	Pin Name	Pin Equivalent Schematic
1 2 6 7 8	LX GND BST VCC VCC			4	FB	
3	VC			5	EN	

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

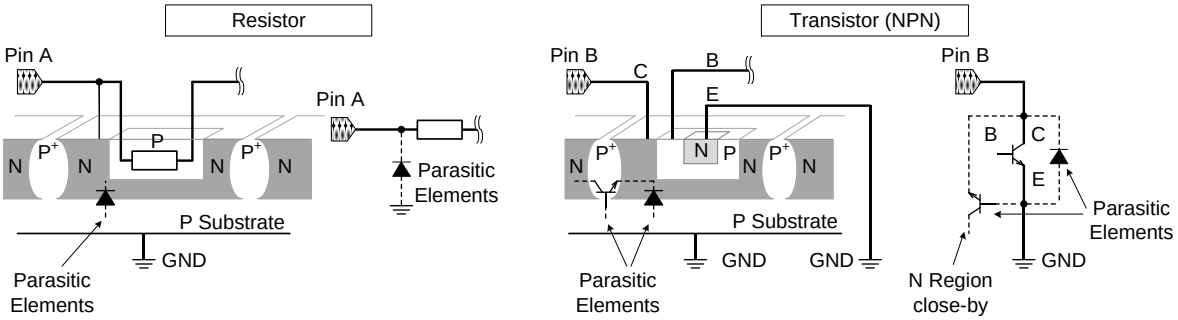

Figure 29. Example of monolithic IC structure

13. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

14. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

15. About High-side Nch FET

Please use within 2.0A contained ripple current, because the absolute maximum rating of high-side Nch FET is 2.0A.

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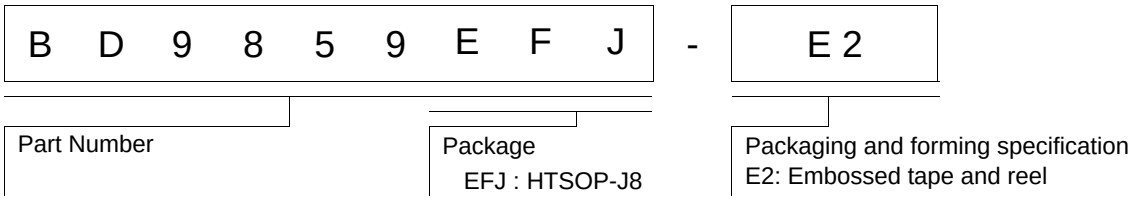
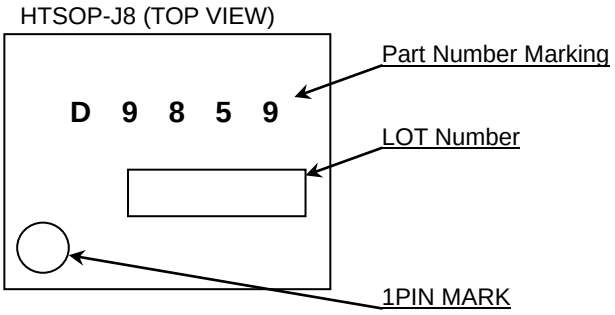
Ordering Information



Marking Diagram



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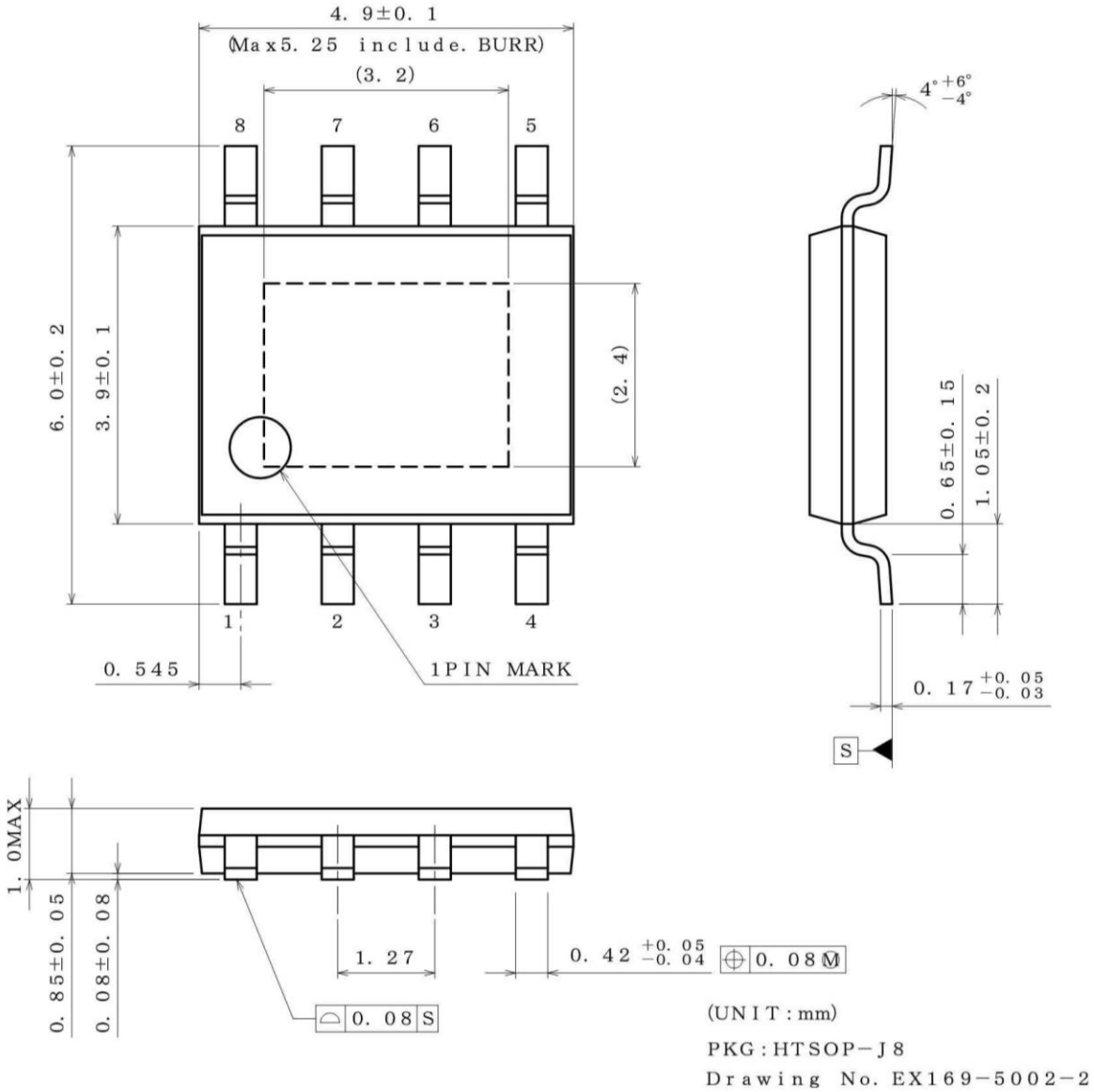
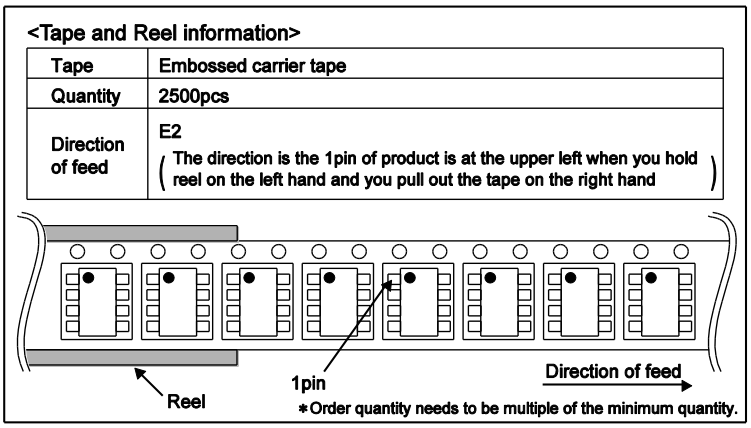
Physical Dimension, Tape and Reel Information

Package Name	HTSOP-J8





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Revision History

Date	Revision	Changes
04.Nov.2014	001	New Release
22,Jan,2016	002	P1. (Key Specifications) Output Voltage range: 1.0V -> 1.0V to 0.7xVCC P3.(Recommended Operation Conditions) Output Voltage: 1.0 -> 1.0 to 0.7xVCC

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

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4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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