

MAX 104 segments (SEG26×COM4)

# Multifunction LCD Segment Driver

**BU97941FV-LB**

This is the product guarantees long time support in Industrial market.

## Features

- Long Time Support Product for Industrial Applications.
- Integrated RAM for Display Data (DDRAM): 26 x 4 bit (Max 104 Segments)
- LCD Drive Output: 4 Common Output, 26 Segment Output
- Integrated 4ch LED Driver Circuit
- Support Standby Mode
- Integrated Power-On-Reset Circuit (POR)
- Integrated Oscillator Circuit
- No External Component
- Low Power Consumption Design
- Independent Power Supply for LCD Driving

## Applications

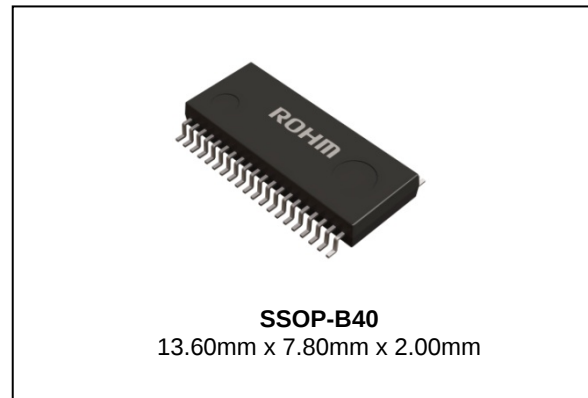
- Industrial Equipment
- Telephone
- FAX
- Portable Equipment (POS, ECR, PDA etc.)
- DSC
- DVC
- Car Audio
- Home Electrical Appliance
- Meter Equipment
- Etc.

## Key Specifications

- Supply Voltage Range: +1.8V to +3.6V
- LCD Drive Power Supply Range: +2.7V to +5.5V
- Operating Temperature Range: -40°C to +85°C
- Max Segments: 104 Segments
- Display Duty: Static, 1/3, 1/4 Selectable
- Bias: Static, 1/3
- Interface: 3wire Serial Interface

## Package

W (Typ.) x D (Typ.) x H (Max.)



## Typical Application Circuit

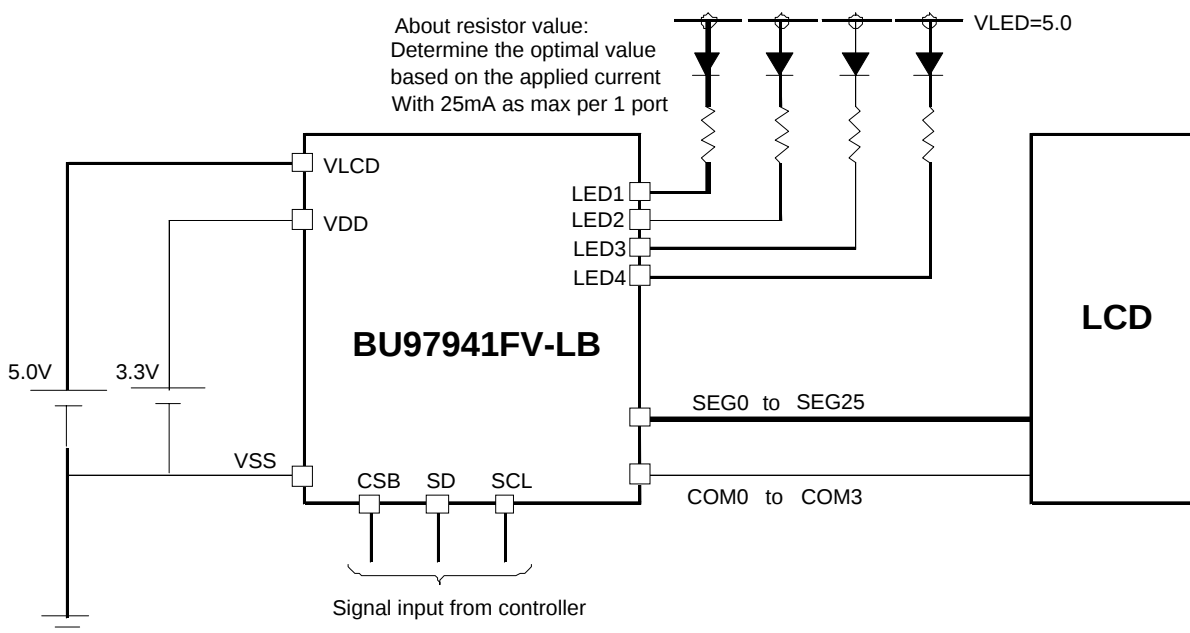


Figure 1. Typical application circuit

Block Diagram / Pin Configuration / Pin Description

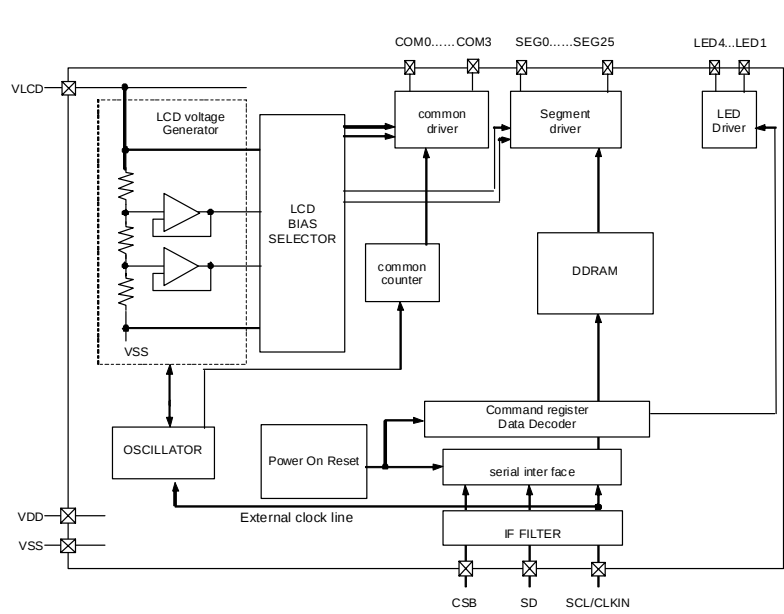


Figure 2. Block Diagram

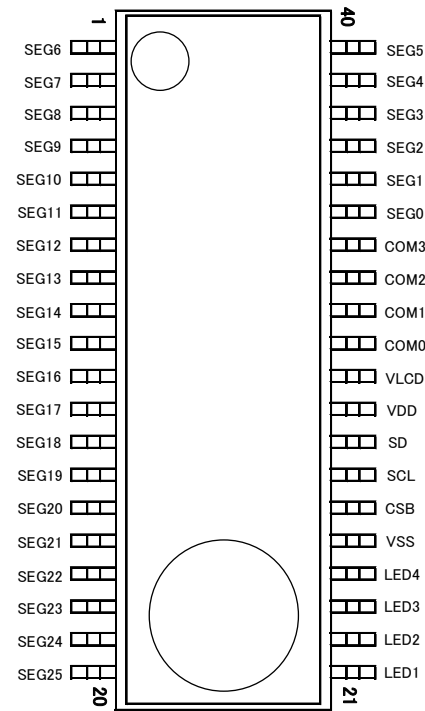


Figure 3. Pin Configuration (TOP VIEW)

Table 1. Pin Description

| Pin Name   | Pin No.             | I/O | Setting when not in use | Function                                                                                                           |
|------------|---------------------|-----|-------------------------|--------------------------------------------------------------------------------------------------------------------|
| CSB        | 26                  | I   | VDD                     | Chip select: "L" active                                                                                            |
| SCL        | 27                  | I   | VSS                     | Serial data transfer clock                                                                                         |
| SD         | 28                  | I   | VSS                     | Input serial data                                                                                                  |
| VDD        | 29                  | -   | -                       | Power supply for LOGIC                                                                                             |
| VSS        | 25                  | -   | -                       | External clock input terminal (for display/PWM using selectable)<br>Support Hi-Z input mode at internal clock mode |
| VLCD       | 30                  | -   | -                       | GND                                                                                                                |
| COM0 to 3  | 31 to 34            | O   | OPEN                    | Power supply for LCD                                                                                               |
| SEG0 to 25 | 1 to 20<br>35 to 40 | O   | OPEN                    | COMMON output for LCD                                                                                              |
| LED1 to 4  | 21 to 24            | O   | OPEN                    | LED driver output                                                                                                  |

## Absolute Maximum Ratings (VSS=0V)

| Item                        | Symbol | Ratings                | Unit | Remarks                               |
|-----------------------------|--------|------------------------|------|---------------------------------------|
| Power Supply Voltage1       | VDD    | -0.3 to +4.5           | V    | Power supply                          |
| Power Supply Voltage2       | VLCD   | -0.5 to +7.0           | V    | Voltage for Liquid crystal display    |
| Power Supply Voltage2       | VLED   | -0.5 to +7.0           | V    | Voltage for LED driving port terminal |
| Power Dissipation           | Pd     | 0.8 <sup>(Note1)</sup> | W    |                                       |
| Input Voltage Range         | VIN    | -0.5 to VDD+0.5        | V    |                                       |
| Operating Temperature Range | Topr   | -40 to +85             | °C   |                                       |
| Storage Temperature Range   | Tstg   | -55 to +125            | °C   |                                       |
| Output Current              | Iout1  | 5                      | mA   | SEG output                            |
|                             | Iout2  | 5                      | mA   | COM output                            |
|                             | Iout3  | 50                     | mA   | LED output (per 1 port)               |

(Note1) Decreases 8mW per 1°C when using at 1 Ta=25°C or higher. (During ROHM standard board mounting)

(Board size : 74.2mm × 74.2mm × 1.6mm Material : FR4 Glass-epoxy board Copper foil : Land pattern only)

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

## Recommended Operating Conditions (Ta=-40°C to +85°C, VSS=0V)

| Item                  | Symbol | Min | Typ | Max | Unit | Remarks                                 |
|-----------------------|--------|-----|-----|-----|------|-----------------------------------------|
| Power Supply Voltage1 | VDD    | 1.8 | -   | 3.6 | V    | Power supply                            |
| Power Supply Voltage2 | VLCD   | 2.7 | -   | 5.5 | V    | Voltage for Liquid crystal Display      |
| Output Current        | Iout1  | -   | -   | 25  | mA   | LED Output (per LED1 port)              |
|                       | Iout2  | -   | -   | 100 | mA   | LED Output (LED port current total sum) |

## Electrical Characteristics

DC Characteristics (Ta=-40°C to +85°C, VDD=1.8V to 3.6V, VLCD=2.7V to 5.5V, VSS=0V)

| Item                                        | Symbol   | Limit Value  |      |        | Unit | Condition                                            |
|---------------------------------------------|----------|--------------|------|--------|------|------------------------------------------------------|
|                                             |          | Min          | Typ  | Max    |      |                                                      |
| "H" level Input Voltage                     | VIH      | 0.8VDD       | -    | VDD    | V    | SD, SCL, CSB                                         |
| "L" level Input Voltage                     | VIL      | VSS          | -    | 0.2VDD | V    | SD, SCL, CSB                                         |
| Hysteresis Width                            | VH       | -            | 0.2  | -      | V    | SCL, VDD=3.3V, Ta=25°C                               |
| "H" level Input Current                     | IIH1     | -            | -    | 5      | μA   | SD, SCL, CSB, VI=3.6V                                |
| LED Off Leak                                | OFF LEAK | 5            | 0    | 5      | μA   | LED VI=5.5V                                          |
| "H" level Output Voltage <sup>(Note2)</sup> | VOH1     | VLCD<br>-0.4 | -    | -      | V    | Iload=-50μA, VLCD=5.0V<br>SEG0 to SEG25              |
|                                             | VOH2     | VLCD<br>-0.4 | -    | -      | V    | Iload=-50μA, VLCD=5.0V<br>COM0 to COM3               |
| "L" level Output Voltage <sup>(Note2)</sup> | VOL1     | -            | -    | 0.4    | V    | Iload= 50μA, VLCD=5.0V<br>SEG0 to SEG25              |
|                                             | VOL2     | -            | -    | 0.4    | V    | Iload= 50μA, VLCD=5.0V<br>COM0 to COM3               |
|                                             | VOL4     | -            | 0.11 | 0.5    | V    | Iload=20mA, VLCD=5.0V<br>LED1 to 4                   |
| Output Voltage <sup>(Note2)</sup>           | VOUT1    | 2.73         | 3.33 | 3.93   | V    | Iload=±50μA, VLCD=5.0V, SEG0 to 25,<br>COM0 to 3     |
|                                             | VOUT2    | 1.07         | 1.67 | 2.27   | V    | Iload=±50μA, VLCD=5.0V, SEG0 to 25,<br>COM0 to 3     |
| Supply Current <sup>(Note1)</sup>           | IstVDD   | -            | 3    | 10     | μA   | Input pin ALL 'L',<br>Display off, Oscillation off   |
|                                             | IstVLCD  | -            | 0.5  | 5      | μA   | Input pin ALL 'L',<br>Display off, Oscillation off   |
|                                             | IVDD1    | -            | 8    | 15     | μA   | VDD=3.3V, Ta=25°C<br>1/3bias, fFR=64Hz, Output open  |
|                                             | IVLCD1   | -            | 10   | 15     | μA   | VLCD=5.0V, Ta=25°C<br>1/3bias, fFR=64Hz, Output open |

(Note1) During power save mode 1, frame inversion.

(Note2) Iload: When setting the load of 1 pin only.

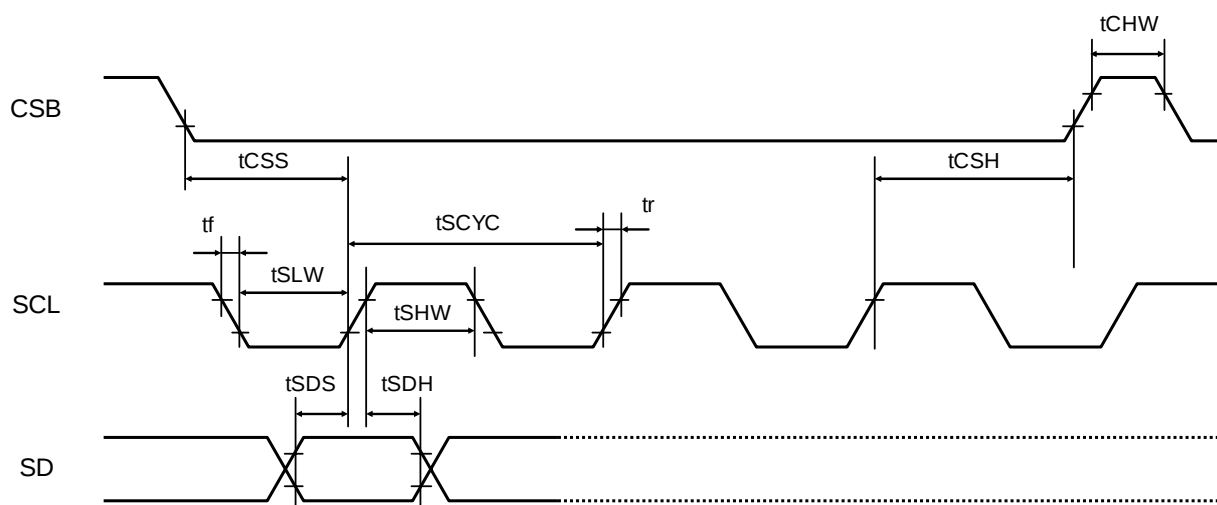
**Electrical Characteristics – continued**

Oscillation Frequency Characteristics (Ta=-40°C to +85°C, VDD=1.8V to 3.6V, VLCD=2.7V to 5.5V, VSS=0V)

| Item              | Symbol | Limit Value |     |      | Unit | Condition                           |
|-------------------|--------|-------------|-----|------|------|-------------------------------------|
|                   |        | Min         | Typ | Max  |      |                                     |
| Frame Frequency 1 | fFR1   | 76.5        | 85  | 93.5 | Hz   | VDD=3.3V, Ta=25°C, fFR=85Hz setting |
| Frame Frequency 2 | fFR2   | 68          | 85  | 97.0 | Hz   | VDD=2.5V to 3.6V, fFR=85Hz setting  |
| Frame Frequency 3 | fFR3   | 59.7        | -   | 68   | Hz   | VDD=1.8V to 2.5V, fFR=85Hz setting  |

MPU Interface Characteristics (Ta=-40°C to +85°C, VDD=1.8V to 3.6V, VLCD=2.7V to 5.5V, VSS=0V)

| Item                | Symbol | Limit Value |     |     | Unit | Condition |
|---------------------|--------|-------------|-----|-----|------|-----------|
|                     |        | Min         | Typ | Max |      |           |
| Input Rise Time     | tr     | -           | -   | 50  | ns   |           |
| Input Fall Time     | tf     | -           | -   | 50  | ns   |           |
| SCL Cycle           | tSCYC  | 250         | -   | -   | ns   |           |
| “H” SCL pulse width | tSHW   | 50          | -   | -   | ns   |           |
| “L” SCL pulse width | tSLW   | 50          | -   | -   | ns   |           |
| SD Setup Time       | tSDS   | 50          | -   | -   | ns   |           |
| SD Hold Time        | tSDH   | 50          | -   | -   | ns   |           |
| CSB Setup Time      | tCSS   | 50          | -   | -   | ns   |           |
| CSB Hold Time       | tCSH   | 50          | -   | -   | ns   |           |
| “H” CSB pulse width | tCHW   | 50          | -   | -   | ns   |           |

**Figure 4. Serial Interface Timing**

I/O Equivalence Circuit

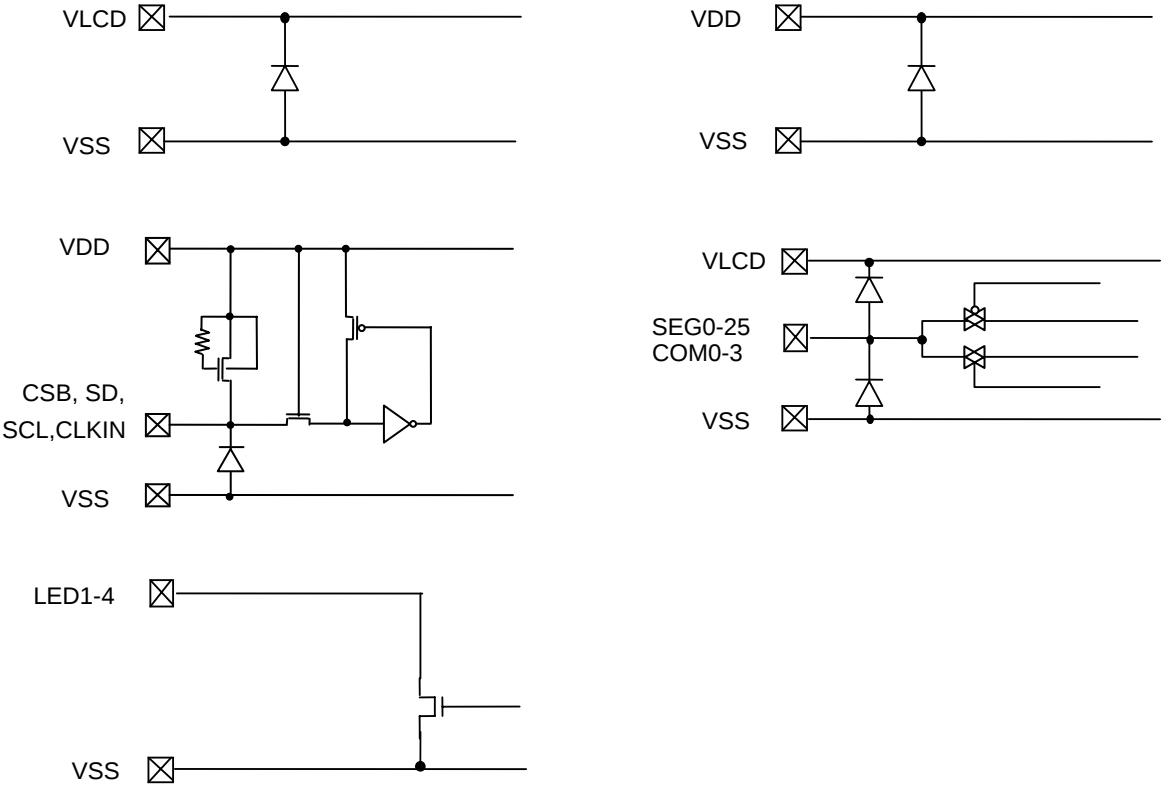


Figure 5. I/O equivalence circuit

Example of Recommended Circuit

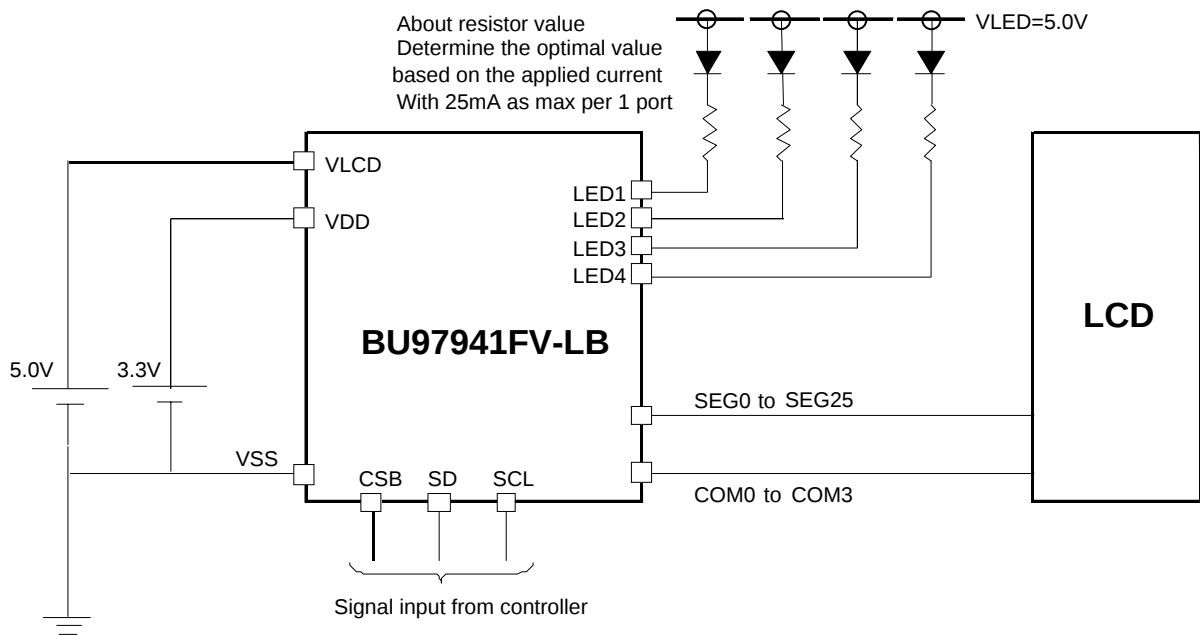


Figure 6. Recommended circuit example

## Function Description

### Command /Data Transfer Method

#### 3-SPI (3-wire Serial Interface)

This device is controlled by a 3-wire signal: CSB, SCL, SD.

First, Interface Counter is initialized with CSB="H".

Setting CSB = "L" enables SD and SCL inputs.

Each command starts with Command or data judgment bit (D/C) as MSB data, followed by D6 to D0 (this is while CSB="L"). Internal data is latched at the rising edge of SCL, and then the data is converted to an 8-bit parallel data at the falling edge of the 8th CLK.

When CSB changes from "L" to "H" and the data being transferred is less than 8 bits, command and data being transferred will be cancelled.

To start sending command again, please set CSB to "L". Then, be sure to input a 1-byte command.

Also, when DDRAM data becomes input state through RAMWR command, the device cannot accept command inputs. In order to input again, please start up CSB.

If CSB is set to "H", the data input state is cancelled and if "CSB" is set to "L" again, command will be received.

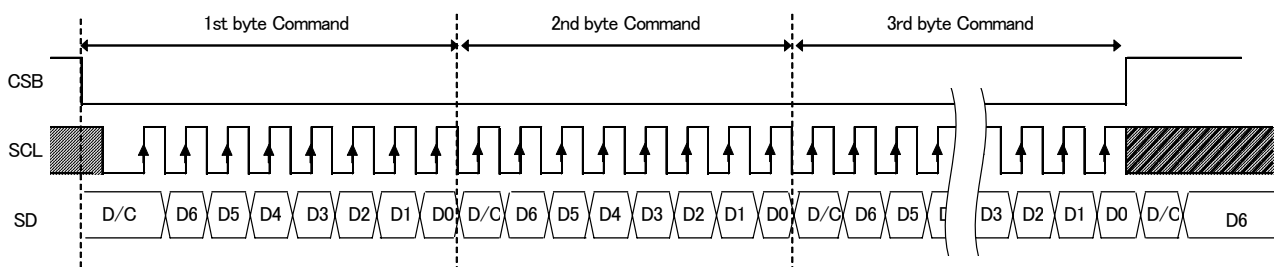
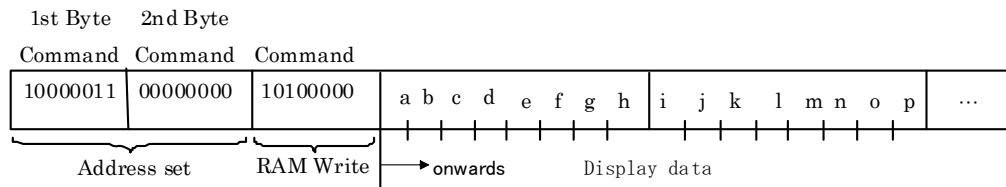


Figure 7. 3-SPI Data Transfer Format

### Write and Transfer Method of Display Data

This device has display data ram of 26×4=104bit.

The handling of display data with write and the handling of DDRAM data and Address and display are as follows:



Binary 8-bit data is written to DDRAM. The starting address is set with the Address set command, and is automatically incremented per 4bit data received.

Next, by transferring data, data can be written continuously to DDRAM.

(When continuously writing data to DDRAM, after writing to the final address 19h(SEG25), address will return to 00h (SEG0) through auto increment.)

|     |   | DDRAM address |       |       |       |       |       |       |       |     |        |        |        |      |  |
|-----|---|---------------|-------|-------|-------|-------|-------|-------|-------|-----|--------|--------|--------|------|--|
|     |   | 00            | 01    | 02    | 03    | 04    | 05    | 06    | 07    | ... | 17h    | 18h    | 19h    |      |  |
| BIT | 0 | a             | e     | i     | m     |       |       |       |       |     |        |        |        | COM0 |  |
|     | 1 | b             | f     | j     | n     |       |       |       |       |     |        |        |        | COM1 |  |
|     | 2 | c             | g     | k     | o     |       |       |       |       |     |        |        |        | COM2 |  |
|     | 3 | d             | h     | l     | p     |       |       |       |       |     |        |        |        | COM3 |  |
|     |   | SEG 0         | SEG 1 | SEG 2 | SEG 3 | SEG 4 | SEG 5 | SEG 6 | SEG 7 |     | SEG 23 | SEG 24 | SEG 25 |      |  |

Writing to RAM is done per 4bit. When CSB is set to 'H' and the data is less than 4 bits, the writing of RAM will be cancelled. (Transfer of command is done per 8bit.)

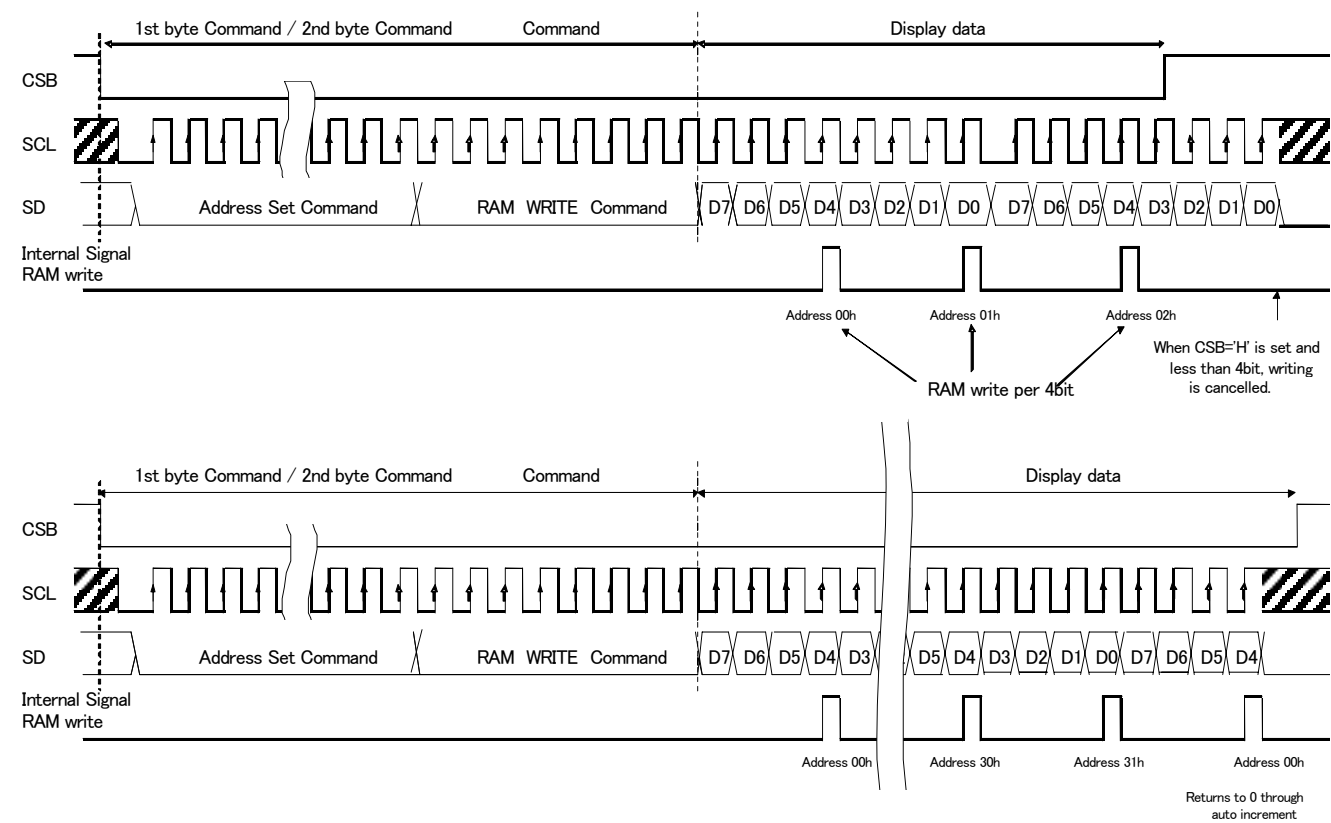


Figure 8. Display Data Transfer Method

## LCD Driver Bias / Duty Circuit

Voltage is generated for LCD driver.

Buffer amplifier is integrated with low power consumption possible.

(Note1) Line and frame inversion can be set by MODESET command.

(Note2) 1/4duty, 1/3duty, and static duty can be set by DISCTL command.

For each liquid crystal display waveform, refer to "Liquid crystal Display Waveform".

## Reset Initial State

The default condition after executing Software Reset is as follows:

Display is turned OFF

Each command register enters Reset state

DDRAM address is initialized

(Note) DDRAM data is not initialized. Therefore, it is recommended to write initial values to all DDRAM before Display on.

## Command / Function Table

Function Description Table

| NO | Command                           | Function                                  |
|----|-----------------------------------|-------------------------------------------|
| 1  | Mode Set (MODESET)                | Liquid crystal Display setting            |
| 2  | Display control (DISCTL)          | LCD setting1                              |
| 3  | Address set (ADSET)               | LCD setting2                              |
| 4  | LED control (LEDCTL)              | LED board ON/OFF setting                  |
| 5  | RAM WRITE (RAMWR)                 | RAM Write Start setting                   |
| 6  | All Pixel ON (APON)               | All display ON                            |
| 7  | All Pixel OFF (APOFF)             | All display OFF                           |
| 8  | All Pixel On/Off mode off (NORON) | Normal display APON/APOFF setting release |
| 9  | Software Reset (SWRST)            | Software reset                            |

## Command Description

D/C (MSB) is a bit for command or data judgment.

For details, see 3-wire Serial Interface Command, Data Transfer Method.

### 1. Mode Set Command (MODESET)

|                  | MSB |    |    |    |    | LSB |    |    |     |       |
|------------------|-----|----|----|----|----|-----|----|----|-----|-------|
|                  | D/C | D6 | D5 | D4 | D3 | D2  | D1 | D0 | Hex | Reset |
| 1st byte Command | 1   | 0  | 0  | 0  | 0  | 0   | 0  | 1  | 81h | -     |
| 2nd byte Command | 0   | 0  | 0  | 0  | P3 | P2  | P1 | P0 | -   | 00h   |

#### Display setting

| Setting     | P3 | Reset state |
|-------------|----|-------------|
| Display OFF | 0  | ○           |
| Display ON  | 1  |             |

Display OFF : Oscillation circuit operation OFF, Liquid crystal power supply circuit operation OFF with frame cycle. Display OFF state (Output : VSS level)

Display ON : Oscillation circuit operation ON, Liquid crystal power supply circuit ON. Read operation from DDRAM starts. Display ON state with frame cycle.

(Note) LED port is not affected by the ON/OFF state of Display.

The output state of LED port is determined by the setting of the LEDCTL command.

#### Liquid crystal Drive Waveform Setting

| Setting         | P2 | Reset state |
|-----------------|----|-------------|
| Frame inversion | 0  | ○           |
| Line inversion  | 1  |             |

#### Power save mode (Low current consumption mode) setting

| Setting          | P1 | P0 | Reset state |
|------------------|----|----|-------------|
| Power save mode1 | 0  | 0  | ○           |
| Power save mode2 | 0  | 1  |             |
| Normal mode      | 1  | 0  |             |
| High power mode  | 1  | 1  |             |

(Note) Use high power mode at VLCD>3V or higher.

#### (Reference Current Consumption Data)

| Setting           | Current Consumption |
|-------------------|---------------------|
| Power save mode 1 | ×1.0                |
| Power save mode 2 | ×1.7                |
| Normal mode       | ×2.7                |
| High power mode   | ×5.0                |

(Note) The current consumption data above is reference data and changes according to panel load.

## 2. (2)Display control command (DISCTL)

|                  | MSB |    |    |    |    |    |    | LSB |     |       |
|------------------|-----|----|----|----|----|----|----|-----|-----|-------|
|                  | D/C | D6 | D5 | D4 | D3 | D2 | D1 | D0  | Hex | Reset |
| 1st byte Command | 1   | 0  | 0  | 0  | 0  | 0  | 1  | 0   | 82h | -     |
| 2nd byte Command | 0   | 0  | 0  | 0  | P3 | P2 | P1 | P0  | -   | 02h   |

## Duty setting

| Setting           | P3 | P2 | Reset state |
|-------------------|----|----|-------------|
| 1/4duty (1/3bias) | 0  | 0  | ○           |
| 1/3duty (1/3bias) | 0  | 1  |             |
| Static (1/1bias)  | 1  | *  |             |

(\*: Don't care)

At 1/3duty setting, the display / blink data for COM3 are invalid.

(COM3: same waveform with COM1)

At 1/1duty (Static) setting, the display / blink data for COM1 to 3 are invalid.

(Note) COM1 to 3: same waveform with COM0

Be careful in sending display data.

For sample output waveform of SEG/COM with duty setting, see "Liquid crystal Display Waveform".

## Frame Frequency Setting

| Setting<br>(When 1/4, 1/3, 1/1duty) | P1 | P0 | Reset state |
|-------------------------------------|----|----|-------------|
| (128Hz, 130Hz, 128Hz)               | 0  | 0  |             |
| (85Hz, 86Hz, 64Hz)                  | 0  | 1  | ○           |
| (64Hz, 65Hz, 48Hz)                  | 1  | 0  |             |
| (51Hz, 52Hz, 32Hz)                  | 1  | 1  |             |

The relationship with frame frequency (FR), internal osc frequency and dividing number is below:

| DISCTL<br>(P1,P0) | Divide  |         |         | FR [Hz] |         |         |
|-------------------|---------|---------|---------|---------|---------|---------|
|                   | 1/4duty | 1/3duty | 1/1duty | 1/4duty | 1/3duty | 1/1duty |
| (0,0)             | 160     | 156     | 160     | 128     | 131.3   | 128     |
| (0,1)             | 240     | 237     | 320     | 85.3    | 86.4    | 64      |
| (1,0)             | 320     | 315     | 428     | 64      | 65      | 47.9    |
| (1,1)             | 400     | 393     | 640     | 51.2    | 52.1    | 32      |

When calculating the OSC frequency from the measurement value of frame frequency, use the following equation:

“OSC frequency = Frame Frequency (Measurement value) × Dividing number”

Dividing number: Using the values of Frame Frequency setting (P1, P0) and duty setting (P3, P2), determine the values from the table above.

Ex) (P1,P0)= (0,1), (P3,P2)= (0,1) → Dividing number= 237

(Note) The value of FR in the table above is the Frame Frequency calculated as OSC Frequency = 20.48KHz (typ).

## 3. Address set command (ADSET)

| MSB              |     |    |    |    | LSB |    |    |    |     |       |  |
|------------------|-----|----|----|----|-----|----|----|----|-----|-------|--|
| MSB              | D/C | D6 | D5 | D4 | D3  | D2 | D1 | D0 | Hex | Reset |  |
| 1st byte Command | 1   | 0  | 0  | 0  | 0   | 0  | 1  | 1  | 83h | -     |  |
| 2nd byte Command | 0   | 0  | 0  | P4 | P3  | P2 | P1 | P0 | -   | 00h   |  |

Sets the starting RAM address for normal display.

Address can be set from 00h to 1Bh.

Setting is prohibited for addresses not written above.

Address during Reset is 00h.

When writing to RAM, a separate RAM WRITE setting is needed.

## 4. LED control command (LEDCTL)

| MSB              |     |    |    |    | LSB |    |    |    |     |       |  |
|------------------|-----|----|----|----|-----|----|----|----|-----|-------|--|
| MSB              | D/C | D6 | D5 | D4 | D3  | D2 | D1 | D0 | Hex | Reset |  |
| 1st byte Command | 1   | 0  | 0  | 0  | 0   | 1  | 0  | 1  | 85h | -     |  |
| 2nd byte Command | 0   | 0  | 0  | 0  | P3  | P2 | P1 | P0 | -   | 00h   |  |

Sets the driver of the LED port. Setting during Reset is 00h.

The relationship between each parameter and the Drive board is as follows:

|         | LED1<br>P0 | LED2<br>P1 | LED3<br>P2 | LED4<br>P3 |
|---------|------------|------------|------------|------------|
| LED ON  | 1          | 1          | 1          | 1          |
| LED OFF | 0          | 0          | 0          | 0          |

(Note) Please input CSB="H" after LEDCTL command is issued.

To avoid noise and reset interface.

## 5. RAM WRITE command (RAMWR)

| MSB                          |              |    |    |    | LSB |    |    |    |     |        |  |
|------------------------------|--------------|----|----|----|-----|----|----|----|-----|--------|--|
|                              | D/C          | D6 | D5 | D4 | D3  | D2 | D1 | D0 | Hex | Reset  |  |
| 1st byte Command             | 1            | 0  | 1  | 0  | 0   | 0  | 0  | 0  | A0h | -      |  |
| 2nd byte Command             | Display data |    |    |    |     |    |    |    |     | Random |  |
|                              | . . . .      |    |    |    |     |    |    |    |     |        |  |
| n <sup>th</sup> byte Command | Display data |    |    |    |     |    |    |    |     | Random |  |

The input data after command setting is the data input for display.

Be sure to send this command after setting the ADSET command.

The display data is transferred per 4bit. (For details, see "Write and Transfer Method of Display Data.")

## 6. All Pixel ON command (APON)

| MSB              |     |    |    |    | LSB |    |    |    |     |       |  |
|------------------|-----|----|----|----|-----|----|----|----|-----|-------|--|
|                  | D/C | D6 | D5 | D4 | D3  | D2 | D1 | D0 | Hex | Reset |  |
| 1st byte Command | 1   | 0  | 0  | 1  | 0   | 0  | 0  | 1  | 91h | -     |  |

Regardless of the contents of DDRAM, the SEG output will enter all light up mode. (Pin that selects SEG output)

## 7. All Pixel OFF command (APOFF)

| MSB              |     |    |    |    |    |    | LSB |    |     |       |
|------------------|-----|----|----|----|----|----|-----|----|-----|-------|
|                  | D/C | D6 | D5 | D4 | D3 | D2 | D1  | D0 | Hex | Reset |
| 1st byte Command | 1   | 0  | 0  | 1  | 0  | 0  | 0   | 0  | 90h | -     |

Regardless of the contents of DDRAM, the SEG output will enter all light up mode. (Pin that selects SEG output)

## 8. All Pixel ON/OFF mode off (NORON)

| MSB              |     |    |    |    |    |    | LSB |    |     |       |
|------------------|-----|----|----|----|----|----|-----|----|-----|-------|
|                  | D/C | D6 | D5 | D4 | D3 | D2 | D1  | D0 | Hex | Reset |
| 1st byte Command | 1   | 0  | 0  | 1  | 0  | 0  | 1   | 1  | 93h | -     |

APON / OFF mode is cancelled and switches to normal display mode. (Pin that selects SEG output)  
After reset, NORON is set and becomes normal display state.

## 9. Software Reset command (SWRST)

| MSB              |     |    |    |    |    |    | LSB |    |     |       |
|------------------|-----|----|----|----|----|----|-----|----|-----|-------|
|                  | D/C | D6 | D5 | D4 | D3 | D2 | D1  | D0 | Hex | Reset |
| 1st byte Command | 1   | 0  | 0  | 1  | 0  | 0  | 1   | 0  | 92h | -     |

This IC will be reset by this command.

Liquid crystal Drive Waveform

1/4Duty

Line inversion

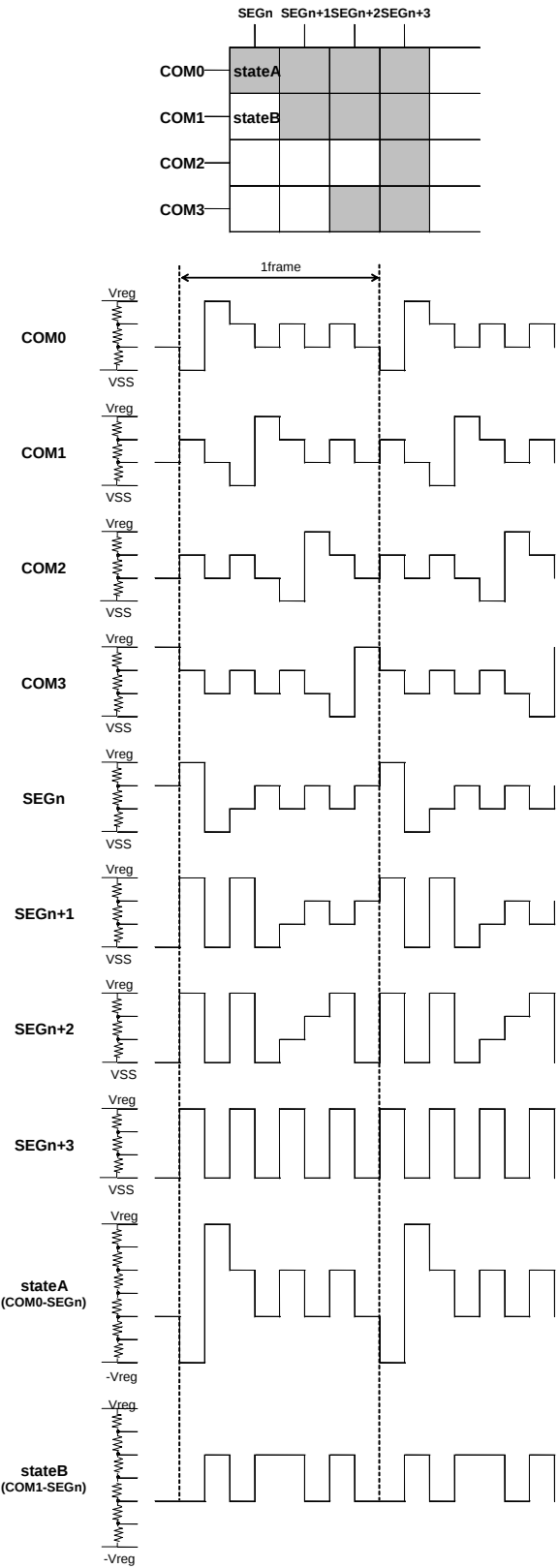


Figure 9. LCD Drive Waveform during Line inversion

Frame inversion

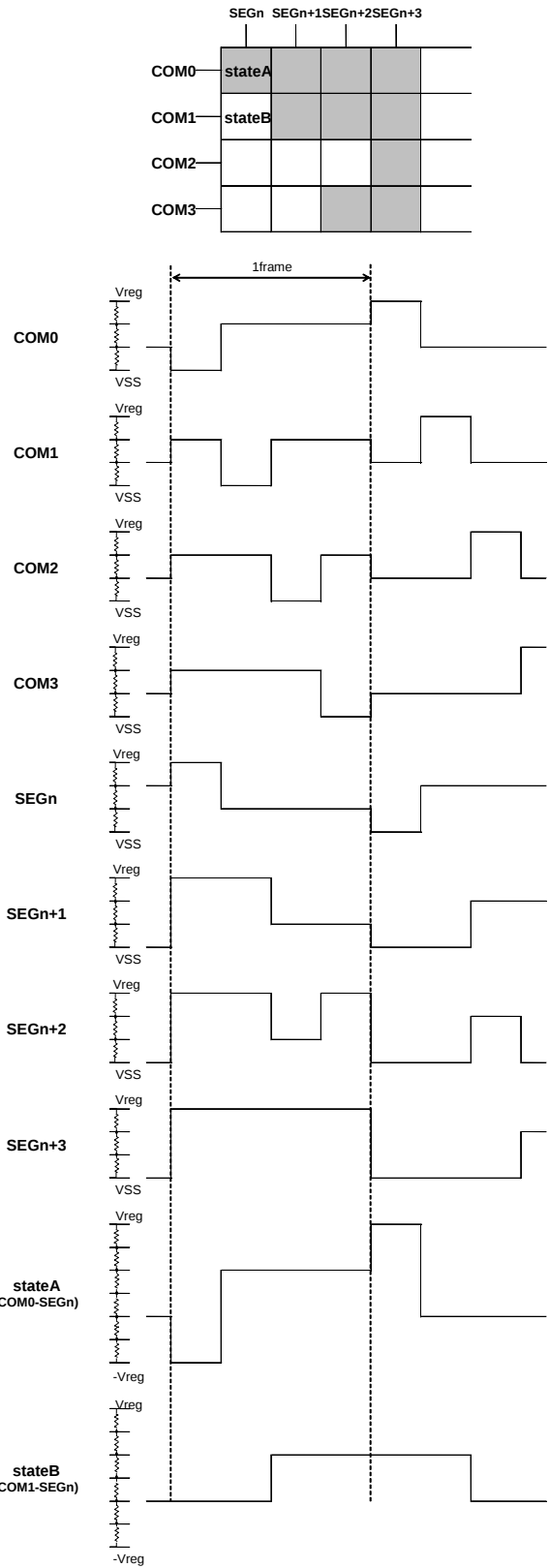
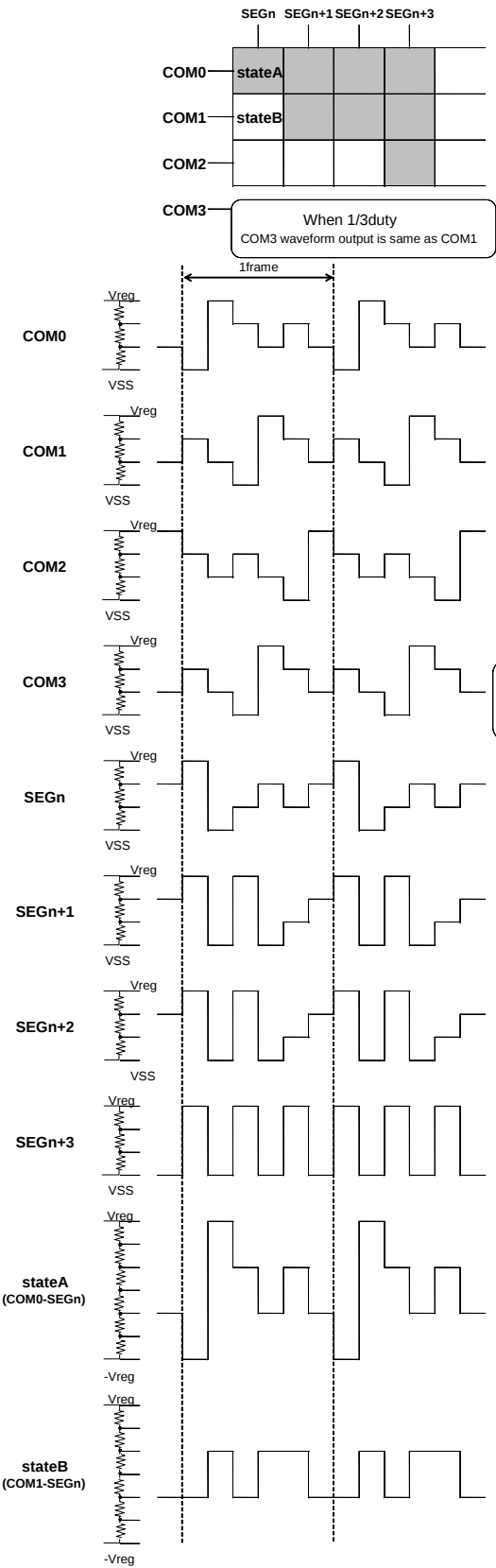


Figure 10. LCD Drive Waveform during Frame inversion

1/3Duty  
Line inversion



Frame inversion

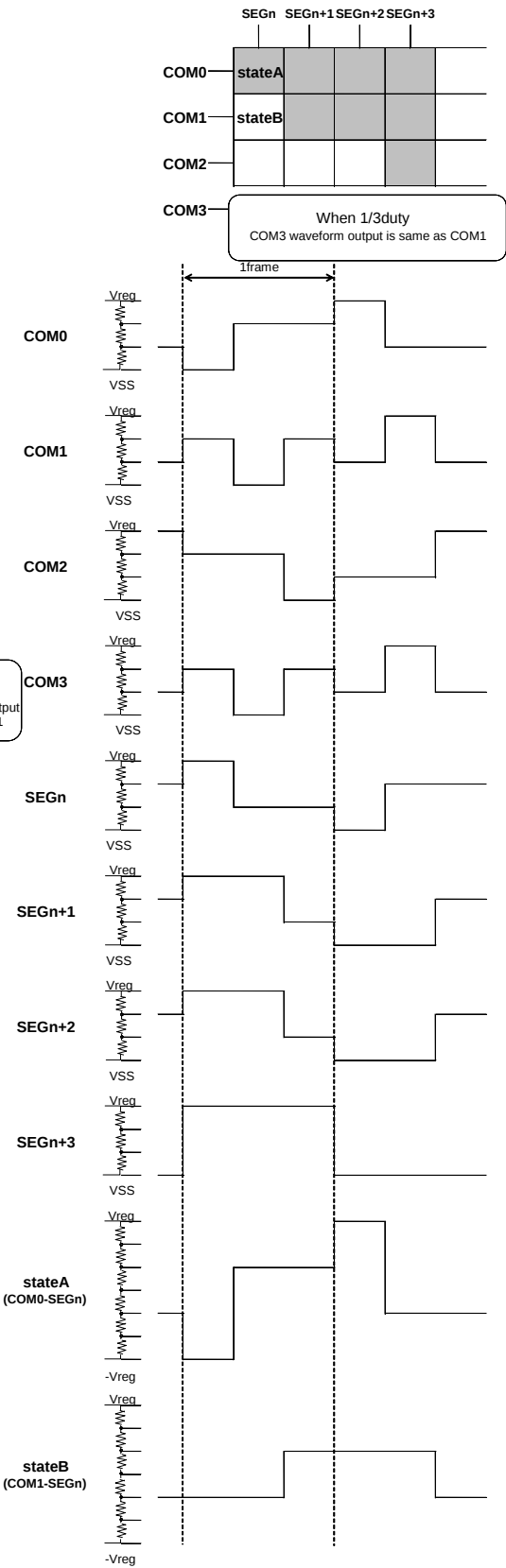


Figure 11. LCD Drive Waveform during Line inversion

Figure 12. LCD Drive Waveform during Frame inversion

1/1Duty (Static)

Line inversion

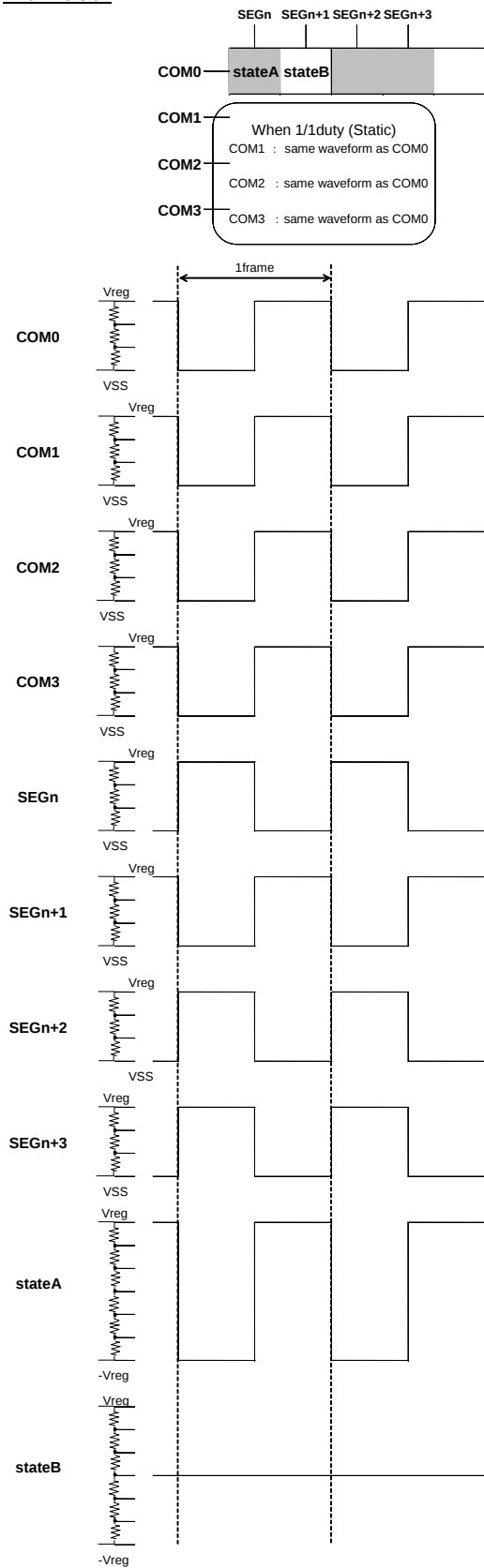


Figure 13.LCD Drive Waveform during Line inversion

Frame inversion

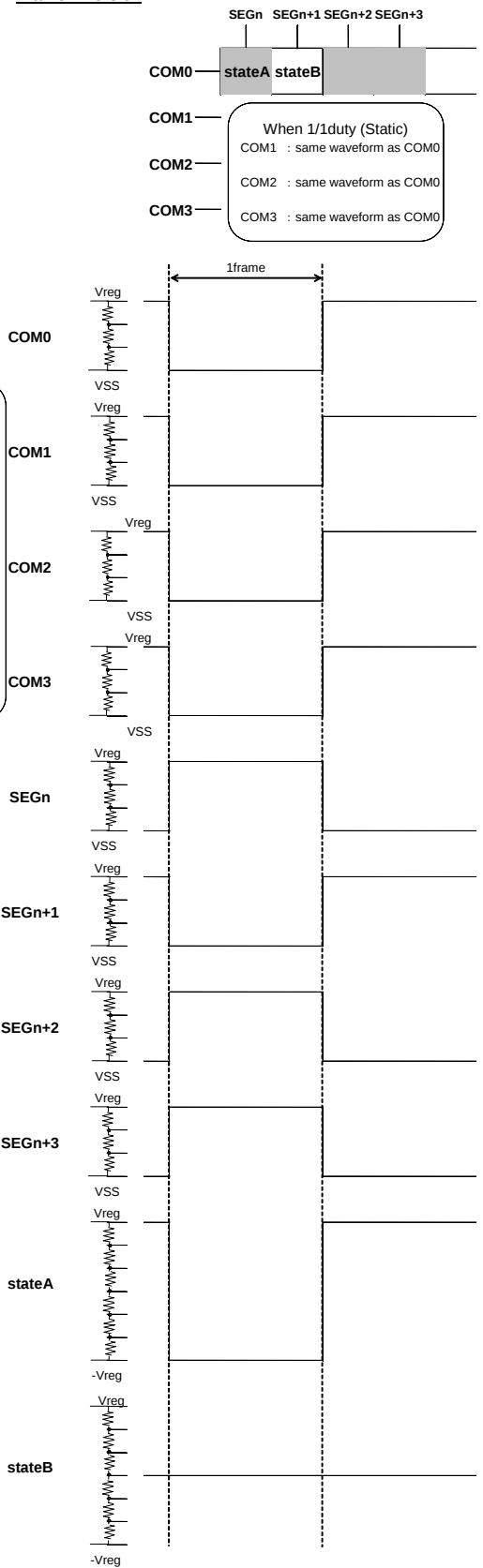
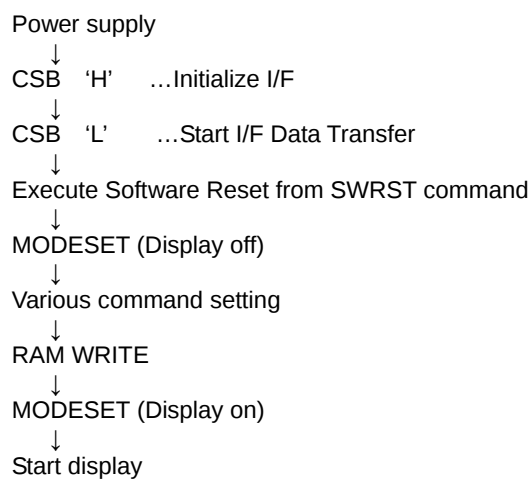


Figure 14. LCD Drive Waveform during Frame inversion

## Initialization Sequence

Execute the following sequence after power supply and start display after the IC has initialized.



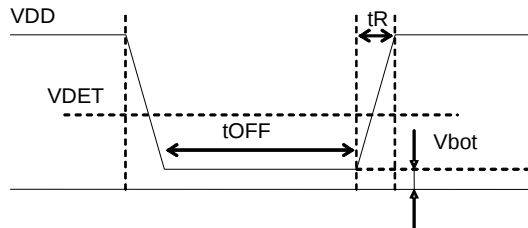
After inserting power supply, each register value, DDRAM address and DDRAM data are random prior to initialization.

**Caution during Power supply ON/OFF****POR circuit**

During power supply rise, because the IC internal circuit and reset pass through an area of unstable low voltage and VDD starts up, there is a risk that the inside of the IC is not completely reset and wrong operation might occur. In order to prevent this, P.O.R circuit and Software Reset functions are incorporated. In order to ensure that operation, do as follows during power supply rise:

1. Set power up conditions to meet the recommended  $t_R$ ,  $t_{OFF}$  and  $V_{bot}$  specs below in order to ensure POR operation. (POR circuit uses VDET type)

(Note) The voltage detection of POR differs depending on the used environment etc.  
In order to assure the operation of POR, it is recommended to make  $V_{bot} = 0.5V$  or lower.

Recommended conditions of  $t_R$ ,  $t_{OFF}$ ,  $V_{bot}$ 

| $t_R$         | $t_{OFF}$     | $V_{bot}$     | VDET     |
|---------------|---------------|---------------|----------|
| 10ms or lower | 1ms or higher | 0.5V or lower | TYP 1.2V |

(Note) VDET is integrated POR detection level

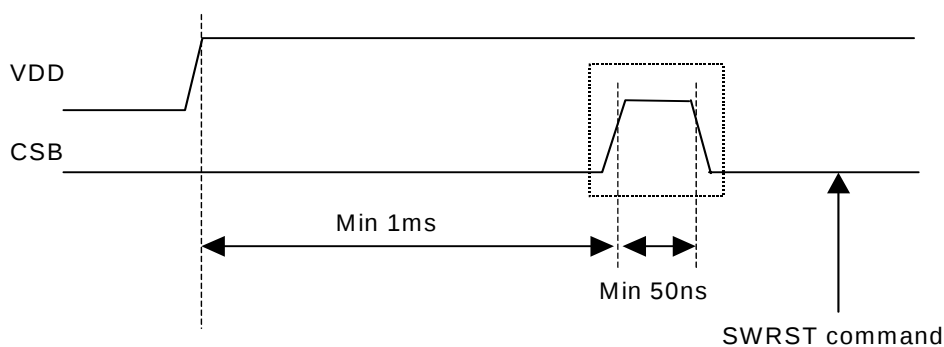
**Figure 15. Rise Waveform**

2. When the conditions are not met, do the following countermeasures after power supply ON:

1. Set CSB to 'H'.
2. Turn ON the CSB and execute SWRST command.

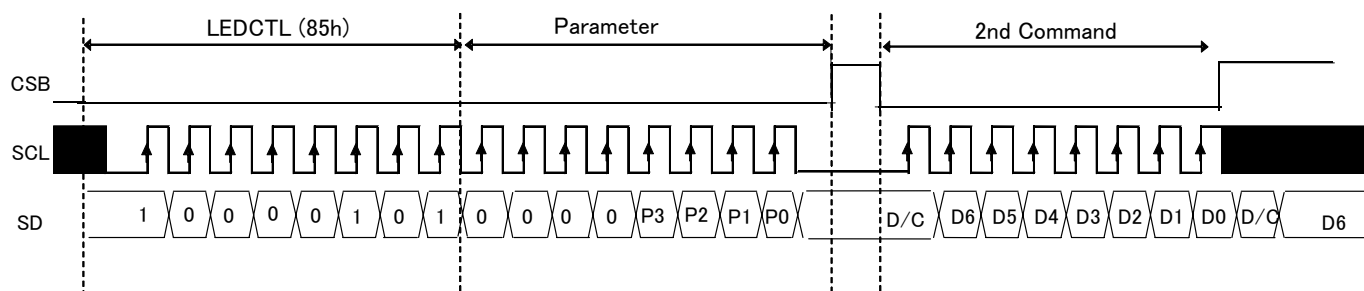
In order for the SWRST command to take effect for sure, it is recommended to start up CSB after 1ms after the VDD level has reached 90%.

※Since the state is irregular until SWRST command input after power supply ON, countermeasure through Software Reset is not the perfect substitute for P.O.R function so it is important to be careful.

**Figure 16. SWRST command sequence**

**Attention about using LEDCTL (85h) command**

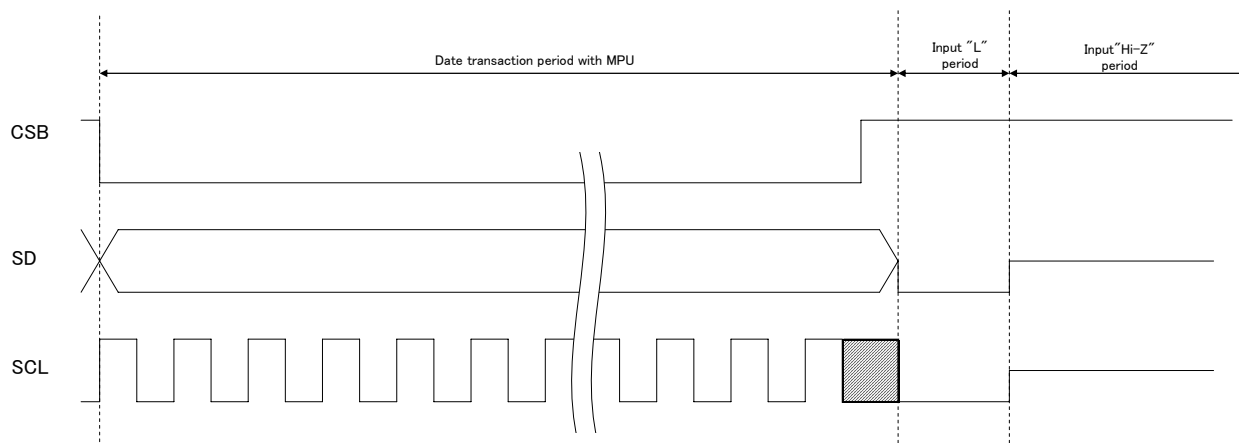
Please input CSB="H" after LEDCTL command is issued. To avoid noise and reset interface.



**Figure 17. Recommended sequence when using LEDCTL (85h) command**

**Attention about input port pull down**

Satisfy the following sequence if input terminals are pulled down by external resistors (In case MPU output Hi-Z).



**Figure 18. Recommended sequence when input ports are pulled down**

BU97941FV-LB adopts a 5V tolerant I/O for the digital input. This circuit includes a bus-hold function to keep the level of HIGH. A pull down resistor of below 10KΩ shall be connected to the input terminals to transit from HIGH to LOW because the bus-hold transistor turns on during the input's HIGH level. (Refer to the Figure 5. I/O Equivalent Circuit)

A higher resistor than 10KΩ (approximate) causes input terminals being steady by intermediate potential between HIGH and LOW level so unexpected current is consumed by the system.

The potential depends on the pull down resistance and bus-hold transistor's resistance.

As the bus-hold transistor turns off upon the input level cleared to LOW a higher resistor can be used as a pull down resistor if an MPU sets SD and SCL lines to LOW before it releases the lines.

The LOW period preceding the MPU's bus release shall be at least 50ns as same as a minimum CLK width (tSLW).

## Operational Notes

### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

### 5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

### 6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

### 7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

### 8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

### 9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

### 10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

**Operational Notes – continued****11. Unused Input Pins**

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

**12. Regarding the Input Pin of the IC**

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

**13. Ceramic Capacitor**

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

**14. Area of Safe Operation (ASO)**

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

**15. Thermal Shutdown Circuit(TSD)**

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature ( $T_j$ ) will rise which will activate the TSD circuit that will turn OFF all output pins. When the  $T_j$  falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

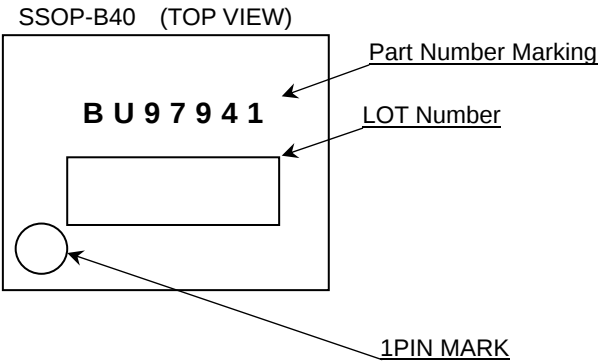
**16. Over Current Protection Circuit (OCP)**

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

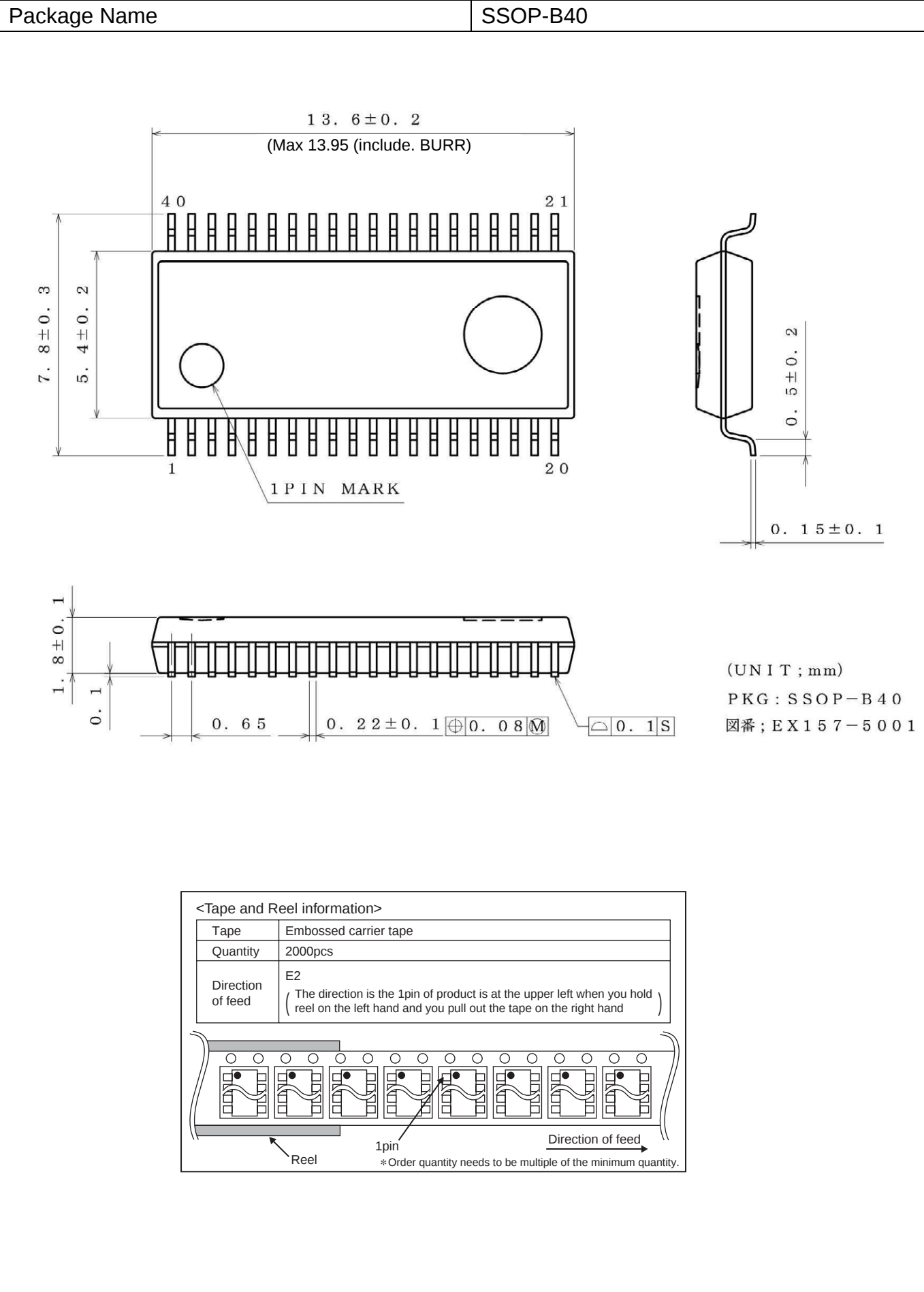
Ordering Information

|                   |  |  |  |  |               |  |  |  |  |                                          |         |  |  |  |
|-------------------|--|--|--|--|---------------|--|--|--|--|------------------------------------------|---------|--|--|--|
| B U 9 7 9 4 1 F V |  |  |  |  |               |  |  |  |  | -                                        | L B E 2 |  |  |  |
| Part Number       |  |  |  |  | Package       |  |  |  |  | Product class                            |         |  |  |  |
|                   |  |  |  |  | FV : SSOP-B40 |  |  |  |  | LB for Industrial applications           |         |  |  |  |
|                   |  |  |  |  |               |  |  |  |  | Packaging and forming specification      |         |  |  |  |
|                   |  |  |  |  |               |  |  |  |  | E2: Embossed tape and reel<br>(SSOP-B40) |         |  |  |  |

Marking Diagram



Physical Dimension, Tape and Reel Information



## Revision History

| Date        | Revision | Changes                                                                                                                          |
|-------------|----------|----------------------------------------------------------------------------------------------------------------------------------|
| 23.Aug.2013 | 001      | New Release                                                                                                                      |
| 26.Feb.2014 | 002      | Delete sentence "and log life cycle" in General Description and Futures.<br>Applied new style (change of the size of the title). |

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|-----------|-----------|------------|-----------|
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| CLASS IV  |           | CLASS III  |           |

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  - [h] Use of the Products in places subject to dew condensation
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8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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