12V to 76V input voltage range 3A output current

1ch Buck Converter Integrated FET

BD9G341AEFJ

General Description

The BD9G341AEFJ is a buck switching regulator with integrated 150mΩ power MOSFET. Current mode architecture provides fast transient response and a simple phase compensation setup. The operating frequency is programmable from 50kHz to 750kHz. Additional protection features are included such as Over Current Protection, Thermal shutdown and Under voltage lockout. The under voltage lockout and hysteresis can be set by external resistor .

Features

- Wide input voltage range from 12V to 76V.
- Integrated 80V/3.5A/150mΩ NchFET.
- Current mode.
- Variable frequency from 50kHz to 750kHz.
- Accurate reference voltage.(1.0 V±1.5 %).
- Precision ENUVLO threshold (±3%).
- Soft-start function
- 0uA Standby current
- Over Current Protection (OCP), Under Voltage Lockout(UVLO), Thermal-Shutdown(TSD),Over Voltage Protection (OVP)
  Thermally enhanced HTSOP-J8 package

Applications

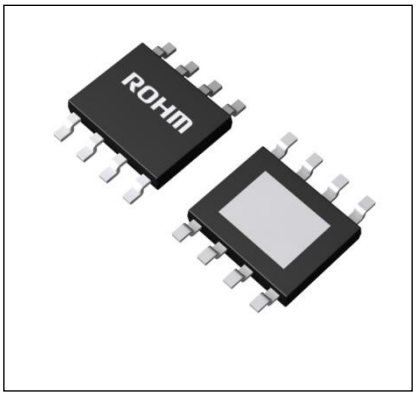
- Industrial distributed power applications.
- Battery powered equipment.

Key specifications

■ Input voltage	12 to 76[V]
■ Ref voltage(Ta=25°C)	±1.5[%]
(Ta=-40 to 85°C)	±2.0[%]
■ Max output current	3 [A] (Max.)
■ Operating Temperature	-40°C to 85°C
■ Max junction temperature	150°C

Package(s)

HTSOP-J8 4.90mm x 6.00mm x 1.00mm



Typical Application Circuit

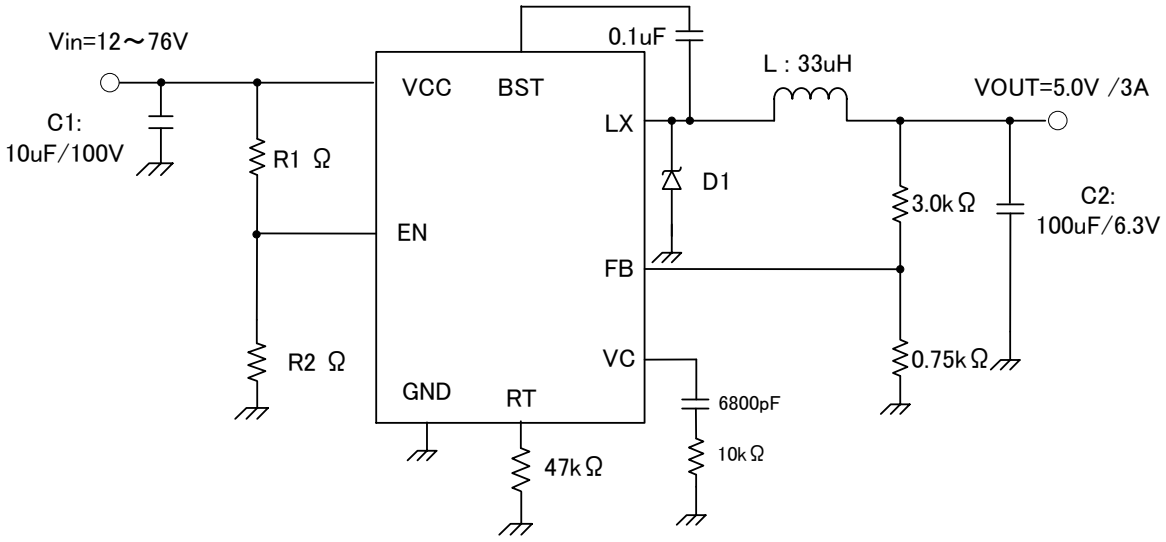


Figure 1. Typical Application Schematic

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

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Pin Configuration

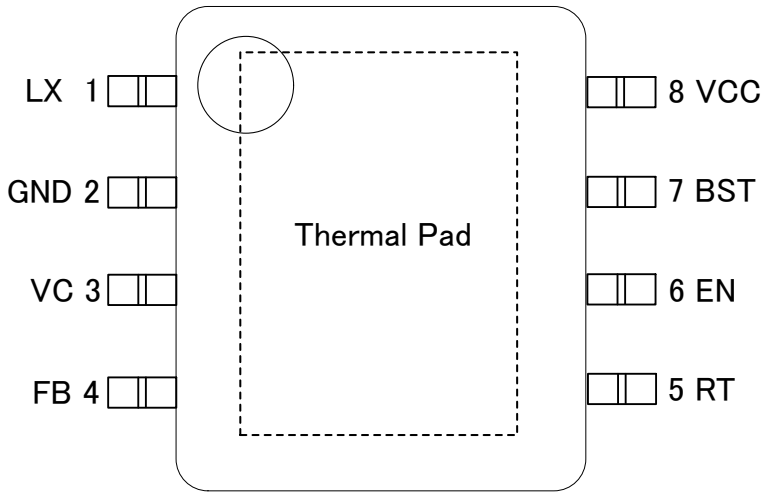

Figure 2.Pin Configuration (TOP VIEW)

Pin Description

Pin No.	Pin Name	Description
1	LX	Switching node. It should be connected as near as possible to the schottky barrier diode, and inductor.
2	GND	Ground pin. GND pattern is kept from the current line of input capacitor to output capacitor.
3	VC	The output of the internal error amplifier. The phase compensation implementation is connected between this pin to GND.
4	FB	Voltage feedback pin. This pin is the error-amp input with the DC voltage is set at 1.0V with feed-back operation.
5	RT	The internal oscillator frequency set pin. The internal oscillator is set with a single resistor connected between this pin and the GND pin. Recommended frequency range is 50kHz to 750kHz
6	EN	Shutdown pin. If the voltage of this pin is below 1.3V,the regulator will be in a low power state. If the voltage of this pin is between 1.3V and 2.4V. The IC will be in standby mode. If the voltage of this pin is above 2.6V, the regulator is operational. An external voltage divider can be used to set under voltage threshold. If this pin is left open circuit. when converter is operating. This pin output 10uA source current. If this pin is left open circuit, a 10uA pull up current source configures the regulator fully operational.
7	BST	Boost input for bootstrap capacitor The external capacitor is required between the BST and the Lx pin. A 0.1uF ceramic capacitor is recommended.
8	VCC	Input supply voltage pin.
-	Thermal Pad	Connect to GND.

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Block Diagram

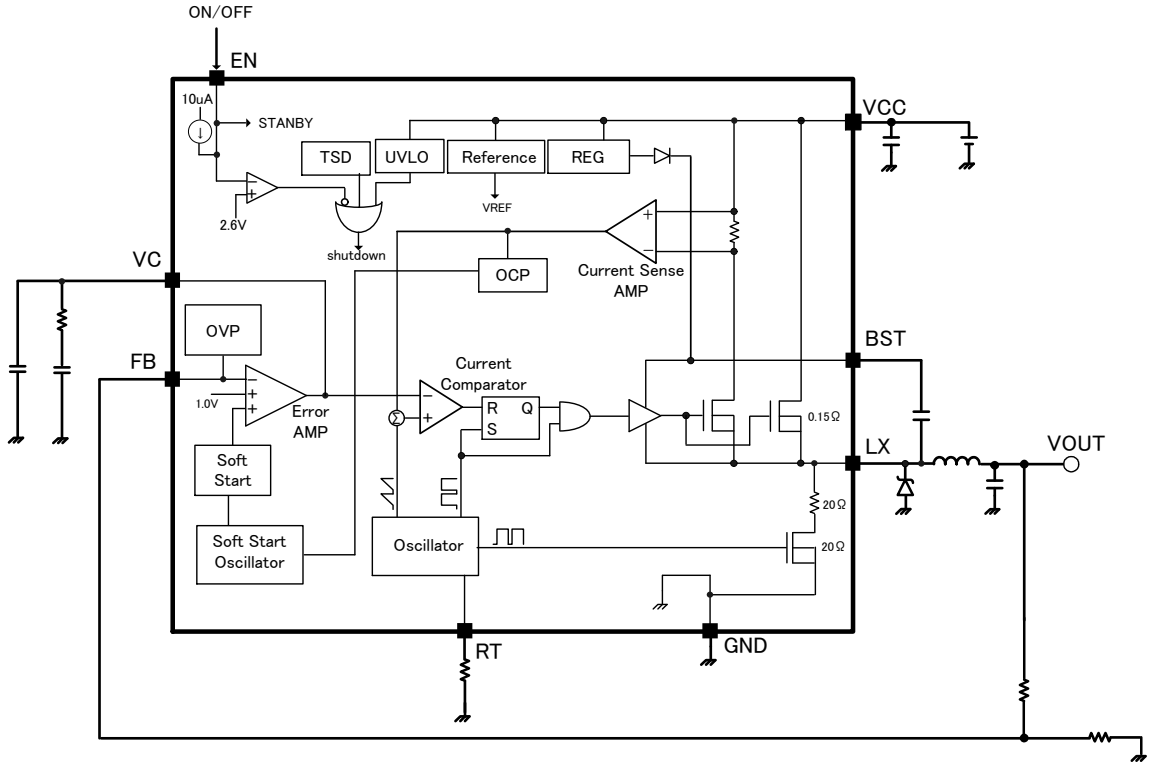

Figure 3.Block Diagram

Description of Block(s)

1. Reference
   This block generates inner reference voltage.

2. REG
   This block generates 8V reference voltage for bootstrap.

3. OSC
   This block generates inner CLK.
   The internal oscillator is set with a single resistor connected between this pin and the GND pin.
   Recommended frequency range is 50 kHz to 750 kHz. If RT pin connect to 47kohm, frequency is set 200 kHz.

4. Soft Start
   Soft Start of the output voltage of regulator prevents in-rush current during Start-up.
   Soft Start time is 20msec (typ)

5. ERROR AMP
   This is an error amplifier what detects output signal, and outputs PWM control signal.
   Internal reference voltage is set to 1.0V.

6. ICOMP
   This is a comparator that outputs PWM signal from current feed-back signal and error-amp output for current-mode.

7. Nch FET SW
   This is a 80V/150mΩ-Power Nch MOSFET SW that converts inductor current of DC/DC converter
   Since the current rating of this FET is 3.5A, it should be used within 3.5A including the DC current and ripple current of the coil.

8. UVLO
   This is a Low Voltage Error Prevention Circuit.
   This prevents internal circuit error during increase of Power supply Voltage and during decline of Power supply Voltage.
   It monitors VCC Pin Voltage and internal REG Voltage, When VCC Voltage becomes 11V and below, UVLO turns OFF all Output FET and turns OFF the DC/DC Comparator Output, and the Soft Start Circuit resets.
   Now this Threshold has Hysteresis of 200mV.

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9. EN
Shutdown function. If the voltage of this pin is below 1.3V, the regulator will be in a low power state. If the voltage of this pin is between 1.3V and 2.4V will be standby mode. If the voltage of this pin is above 2.6V, the regulator is operational. An external voltage divider can be used to set under voltage threshold. If this pin is left open circuit. when converter is operating. This pin output 10uA source current. If this pin is left open circuit, a 10uA pull up current source configures the regulator fully operational. When IC turn off, EN pin is pulled down by pull down resistor that sink above 10uA.

10. OCP
Over current protection
If the current of power MOSFET is over 6.0A (typ), this function reduces duty pulse –by- pulse and restricts the over current. If IC detects OCP 2 times sequentially, the device will stop and after 20 msec restart.

11. TSD
This is Thermal Shutdown Detection
When it detects an abnormal temperature exceeding Maximum Junction Temperature (Tj=150°C), it turns OFF all Output FETs, and turns OFF the DC/DC Comparator Output. When Temperature falls, and the IC automatically returns

12. OVP
Over voltage protection.
Output voltage is monitored with FB terminal, and output FET is turned off when it becomes 120% of set-point voltage.

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Maximum input voltage	VCC	80	V
BST to GND	VBST	85	V
Maximum input current	Imax	3.5	A
BST to LX	⊿VBST	15	V
EN to GND	VEN	80	V
LX to GND	VLX	80	V
FB to GND	VFB	7	V
Power Dissipation	Pd	3.76 (NOTE1)	W
Operating Temperature	Topr	-40 to +85	°C
Storage Temperature	Tstg	-55 to +150	°C
Junction Temperature	Tjmax	150	°C

(NOTE1)During mounting of 70×70×1.6t mm 4layer board.Reduce by 5.4mW for every 1°C increase..(Above 25°C)

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Electrical Characteristics (Unless otherwise specified Ta=25°C, VCC=48V, Vo=5V,EN=3V,RT=47kΩ **)**

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
【Circuit Current】						
Stand-by current of VCC	Ist	—	0	10	µA	VEN=0V
Circuit current of VCC	Icc	—	1.5	2.0	mA	FB=1.5V
【Under Voltage Lock Out (UVLO)】						
Detect Voltage	Vccuv	10.4	11	11.6	V	
Hysteresis width	Vuvhy	—	200	300	mV	
【Error Amp】						
FB threshold voltage	VFBN	0.985	1.000	1.015	V	Ta=25°C
	VFBA	0.980	1.000	1.020	V	Ta=-40 to 85°C
FB Input bias current	IFB	-1	0	1	uA	VFB=2.0V
VC source current	Isource	15	40	65	uA	
VC sink current	Isink	-65	-40	-15	uA	
Soft start time	Tsoft	15	20	25	msec	
Error amplifier DC gain	AVEA	—	10000	—	V/V	
Trans conductance	GEA	—	300	—	µA/V	
【Current Sense Amp 】						
VC to switch current trans conductance	G_{CS}	—	10	—	A/V	
【OCP】						
Detect current	Iocp	3.5	6.0	—	A	
OCP latch count	NOCP	—	2	—	count	
OCP latch hold time	TOCP	15	20	25	msec	
【Output】						
Lx NMOS ON resistance	RonH	—	150	—	mΩ	
【CTL】						
EN Pin inner REG on voltage ON	VENON	1.3	—	2.4	V	
EN Pin IC output on threshold	Venuv	2.52	2.6	2.68	V	IC on or off threshold
EN pin	IEN	9.0	10.0	11.0	µA	VEN=3V
【Oscillator】						
Oscillator frequency	Fosc	180	200	220	kHz	RT:R=47kΩ
Forced off time	Toff	—	—	500	nsec	

Recommended Operating Ratings(Ta=25°C)

Item	Symbol	Rating			Unit
		Min	Typ	Max	
Power Supply Voltage	VCC	12	—	76	V
Output voltage	VOUT	1.0(Note2)	—	VCC(Note3)	V
Output current	IOUT	-	—	3.0	A
Oscillator frequency	Fosc	50	—	750	kHz

(Note2) Restricted by minduty=f × MinOn Time (f :frequency)
If the voltage of Vcc × minduty [V] lower than 1V, this value is minimum output.
(Note3) Restricted by maxduty =1-f × forced off time
The maximum output is (Vcc– Iout*Ron) × maxduty

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Typical Performance Characteristics
(Unless otherwise specified, Ta=25°C, VCC=24V, VOUT=5V)

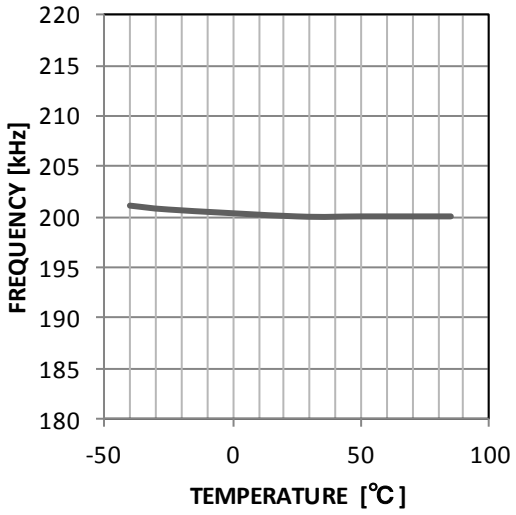

Fig.4 Oscillator Frequency - Temperature

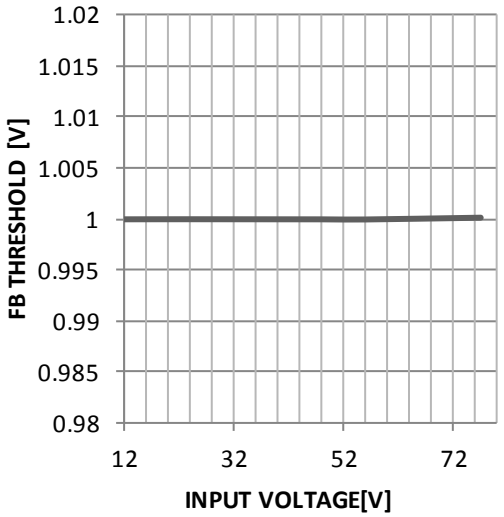

Fig.5 FB Threshold Voltage- Input Voltage

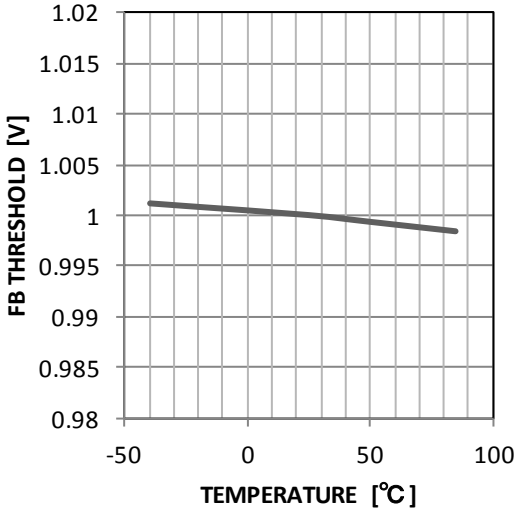

Fig.6 FB Threshold Voltage - Temperature

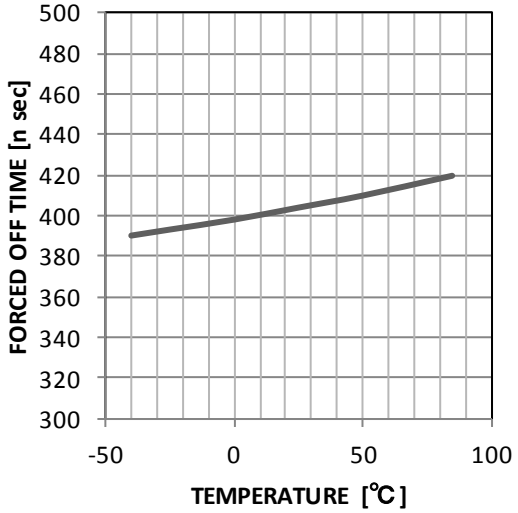

Fig.7 Forced off time - Temperature

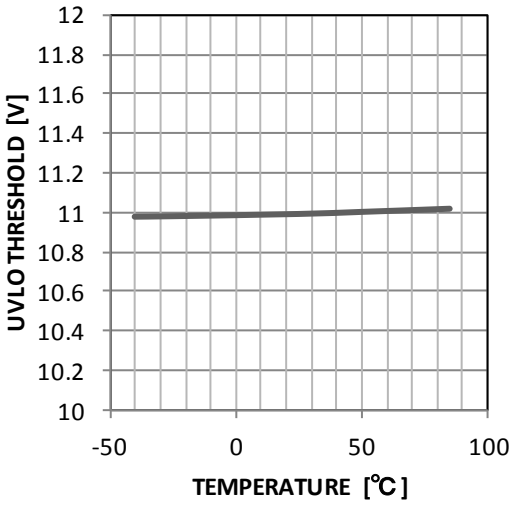

Fig.8 UVLO Threshold Voltage - Temperature

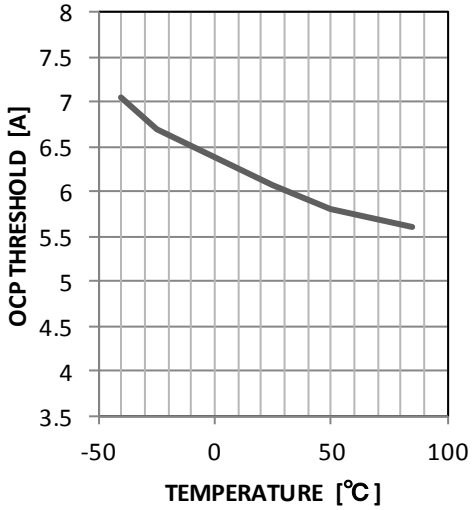

Fig.9 OCP Detect Current - Temperature

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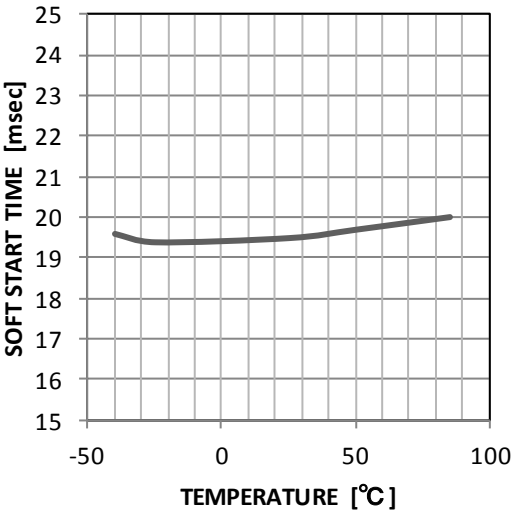

Fig.10 Soft Start Time - Temperature

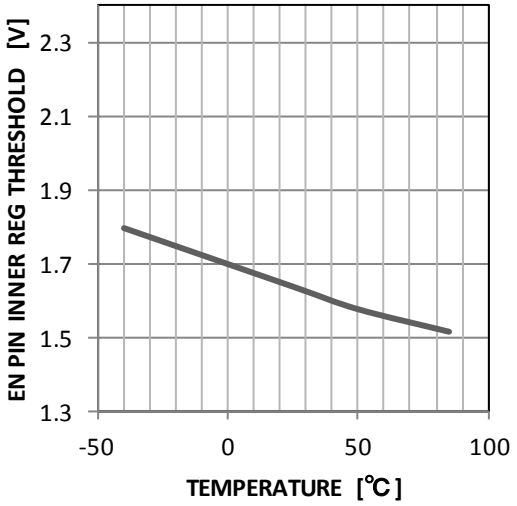

Fig.11 EN Pin Inner REG ON Threshold - Temperature

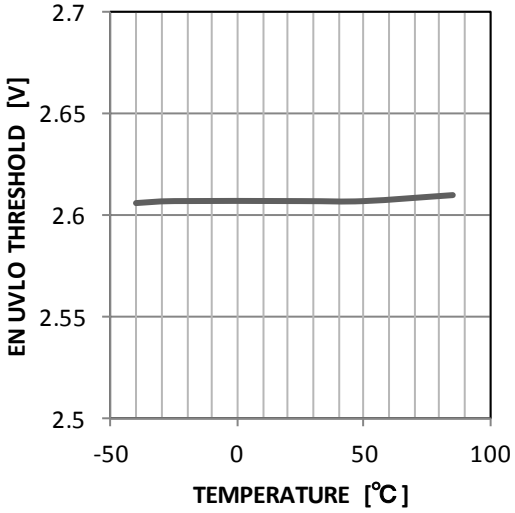

Fig.12 ENUVLO Threshold - Temperature

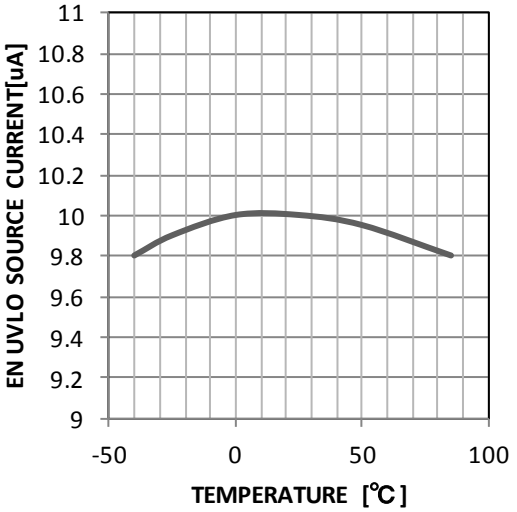

Fig.13 EN Source Current - Temperature

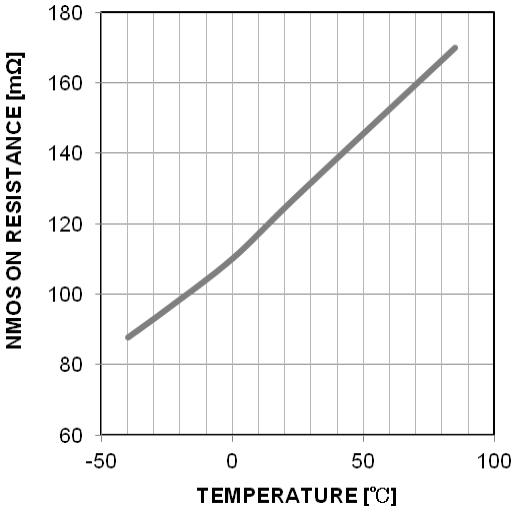

Fig.14 NMOS ON Resistance -Temperature

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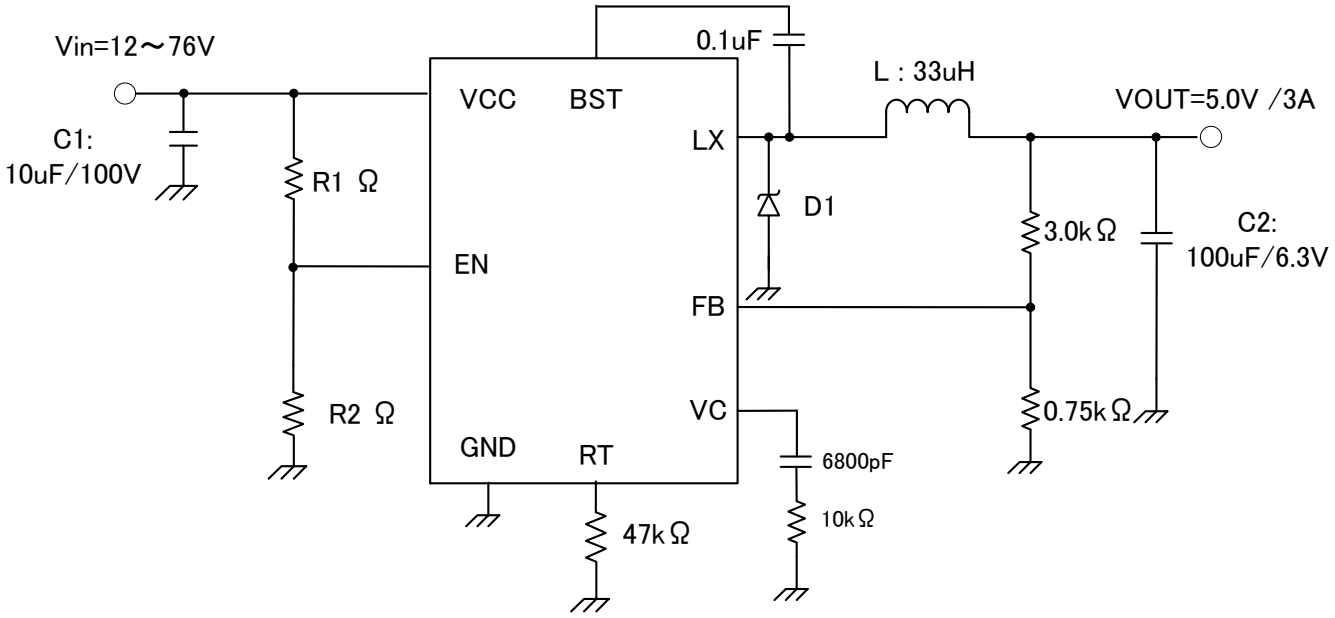
Reference Characteristics of Typical Application Circuits

Vout=5V , f=200kHz



Parts :	L	:SUMIDA	CDRH129HF	33μH
	C1	:TDK	C5750X7S2A106K	10μF/100V
	C2	:TDK	C4532X5R0J107M	100μF/6.3V
	D1	:Rohm	RB095B-90	

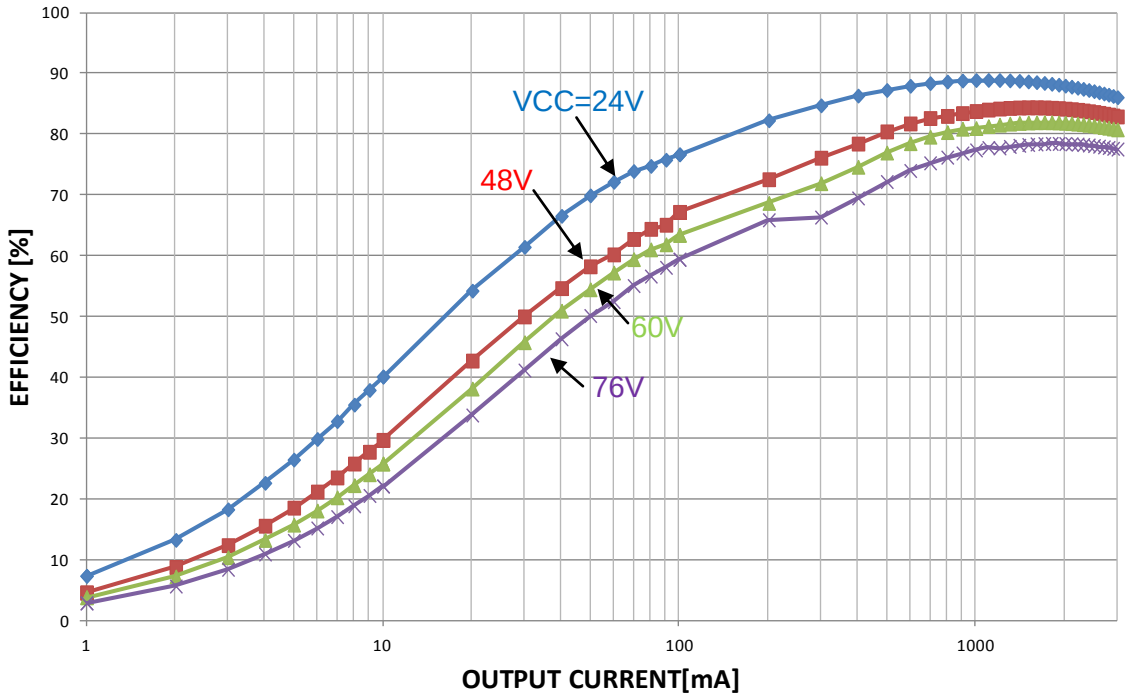


Fig.15 Efficiency – Output Current

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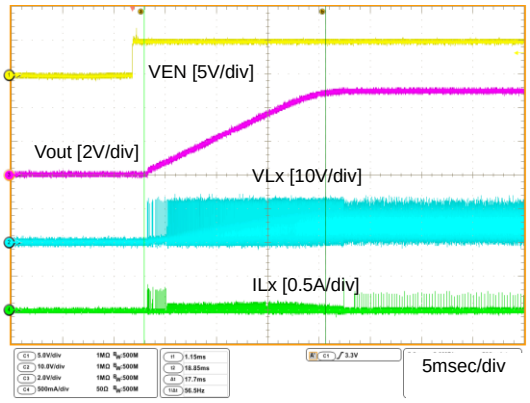

Fig.16 Start-up Characteristics

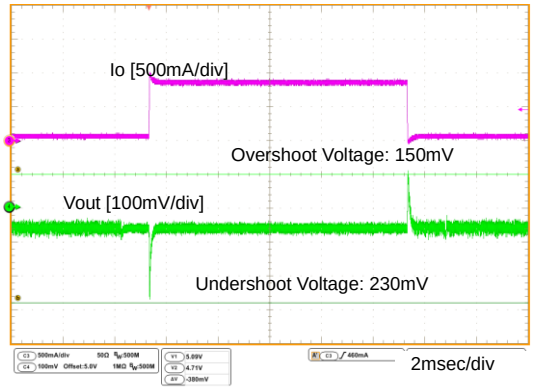

Fig.17 Load Response
Iout:100mA ⇔1A

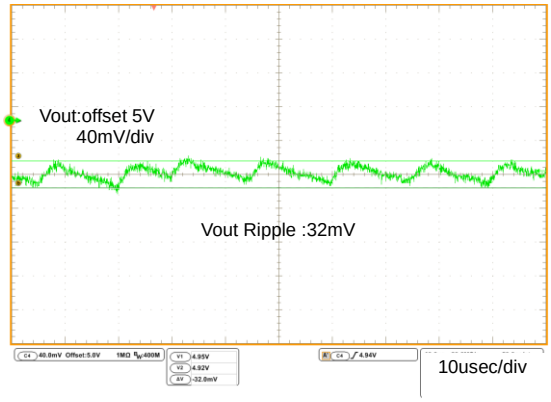

Fig.18 Lx Switching/Vout Ripple
Io = 100mA

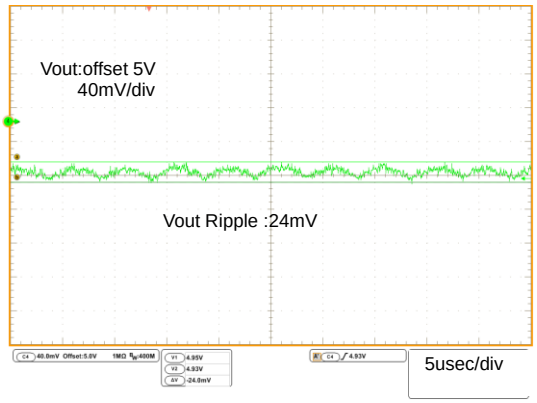

Fig.19 Lx Switching/Vout Ripple
Io=1A

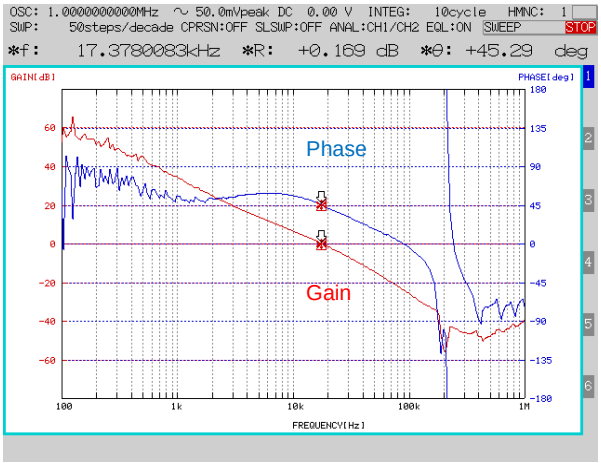

Fig.20 Frequency Response
Io=100mA

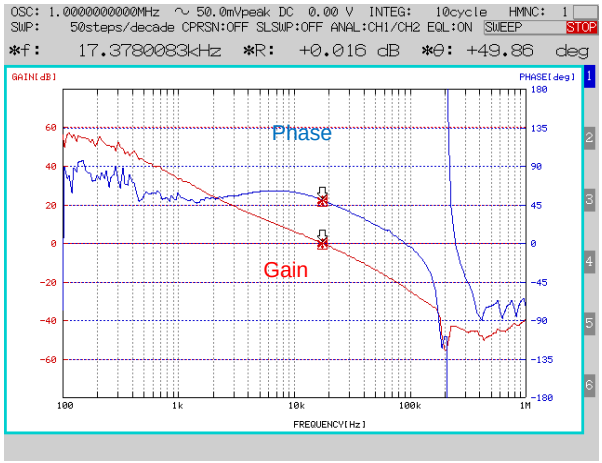

Fig.21 Frequency Response
Io=3.0A

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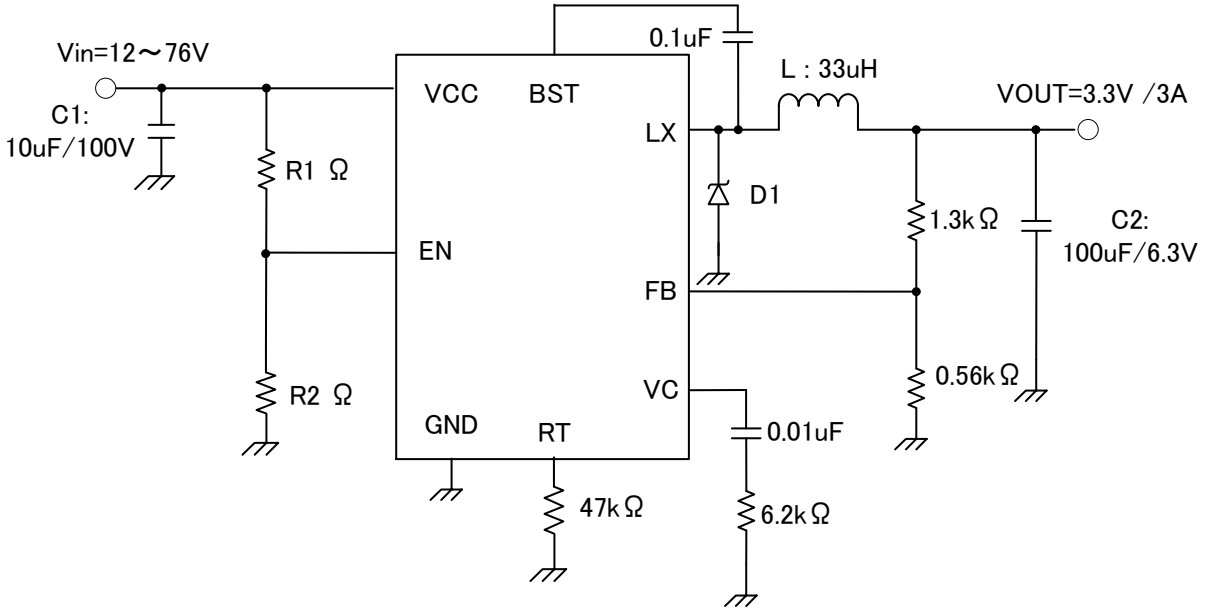
Reference Characteristics of Typical Application Circuits

Vout=3.3V , f=200kHz



Parts :	L	:SUMIDA	CDRH129HF	33μH
	C1	:TDK	C5750X7S2A106K	10μF/100V
	C2	:TDK	C4532X5R0J107M	100μF/6.3V
	D1	:Rohm	RB095B-90	

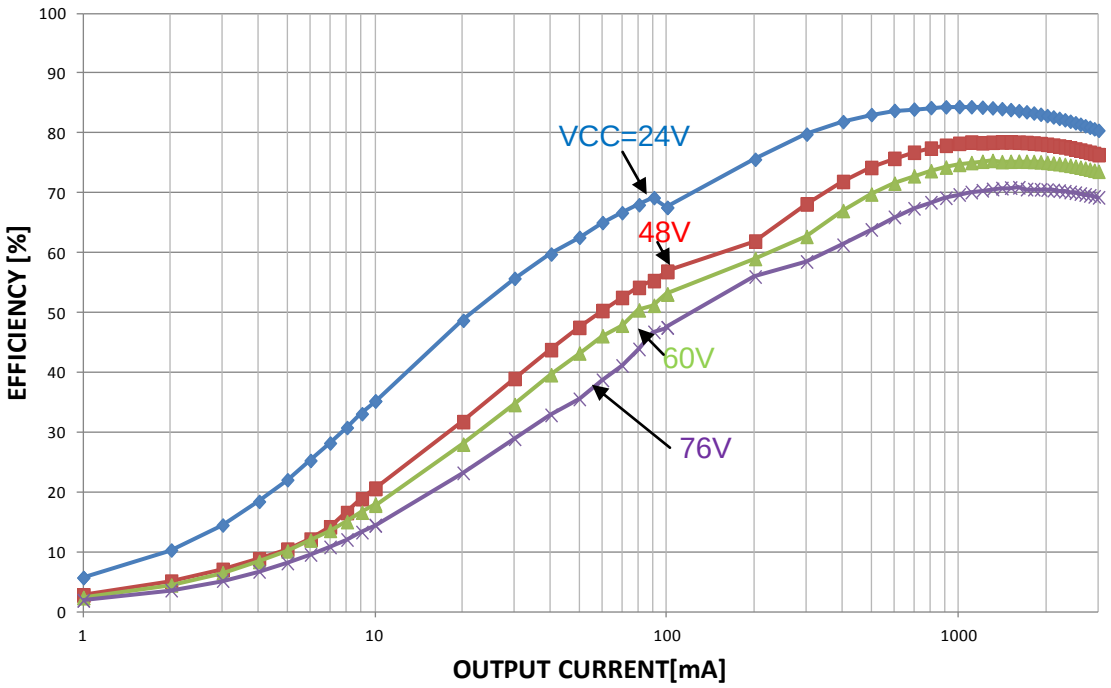


Fig.22 Efficiency – Output Current

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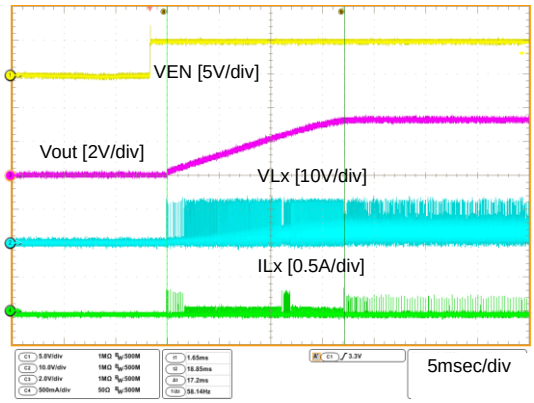

Fig.23 Start-up Characteristics

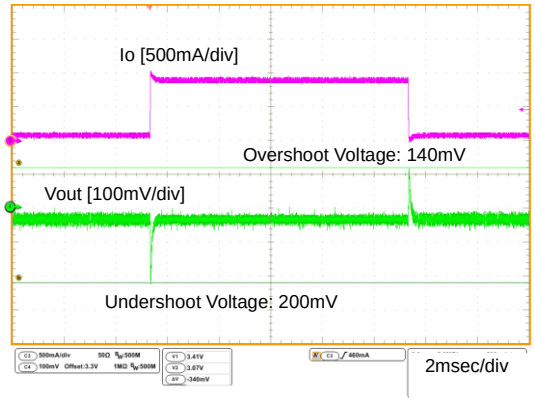

Fig.24 Load Response
Iout:100mA ⇔1A

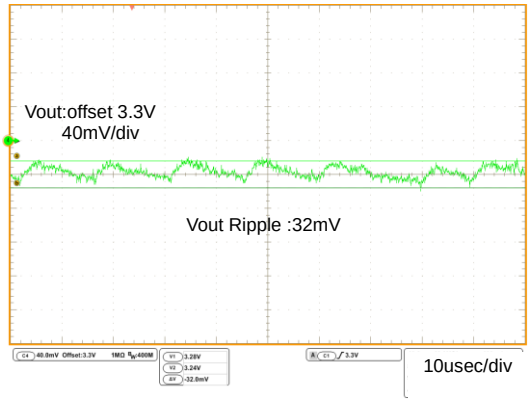

Fig.25 Lx Switching/Vout Ripple
Io = 100mA

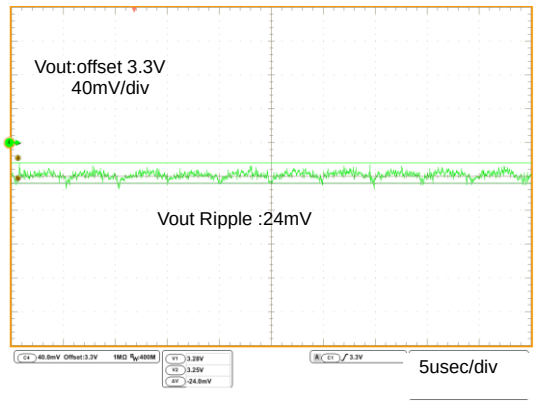

Fig.26 Lx Switching/Vout Ripple
Io=1A

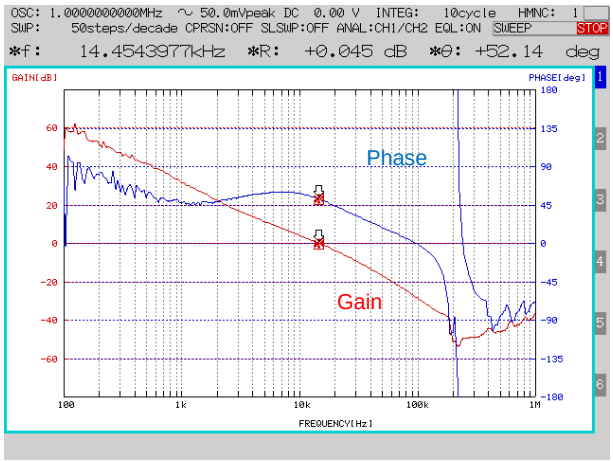

Fig.27 Frequency Response
Io=100mA

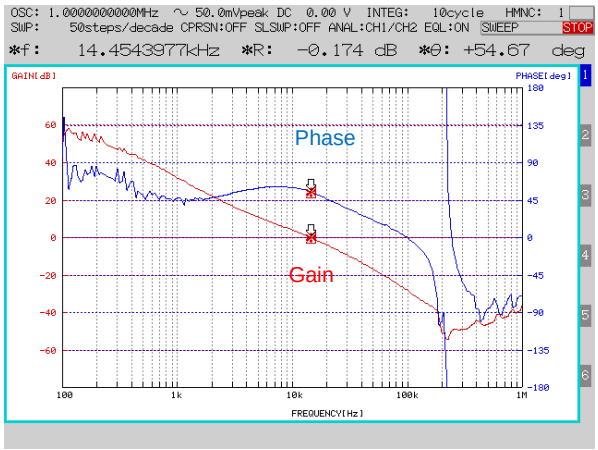

Fig.28 Frequency Response
Io=3A

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Detailed Description

◇Frequency setting

Arbitrary internal oscillator frequency setup is possible by connecting RT resistance. Recommended frequency range is 50 kHz to 750 kHz.

For setting frequency f [Hz] 、RT resistance is looked for using the following formula.

$$RT = \frac{\frac{1}{f} - 400 \times 10^{-9}}{96.48 \times 10^{-12}} [\Omega]$$

If setting frequency is 200kHz, RT is 47kΩ.

RT resistance is related to frequency as shown in Figure 26.

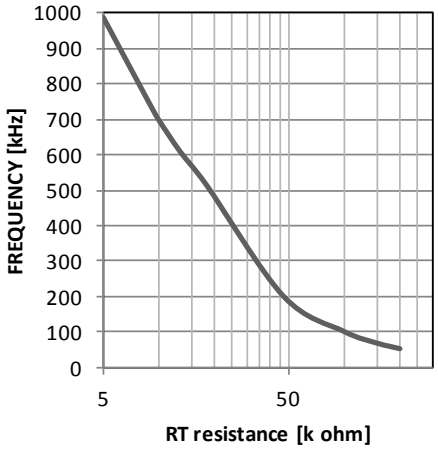

Fig.29 Oscillator Frequency - RT resistance

◇External UVLO threshold

The high precision reset function is built in EN terminal of BD9G341AEFJ, and arbitrary low-voltage malfunction prevention setup is possible by connecting EN pin to resistance division of input voltage.

When you use, please set R1 and R2 to arbitrary voltage of IC turned on (Vuv) and hysteresis (Vuvhys) like below.

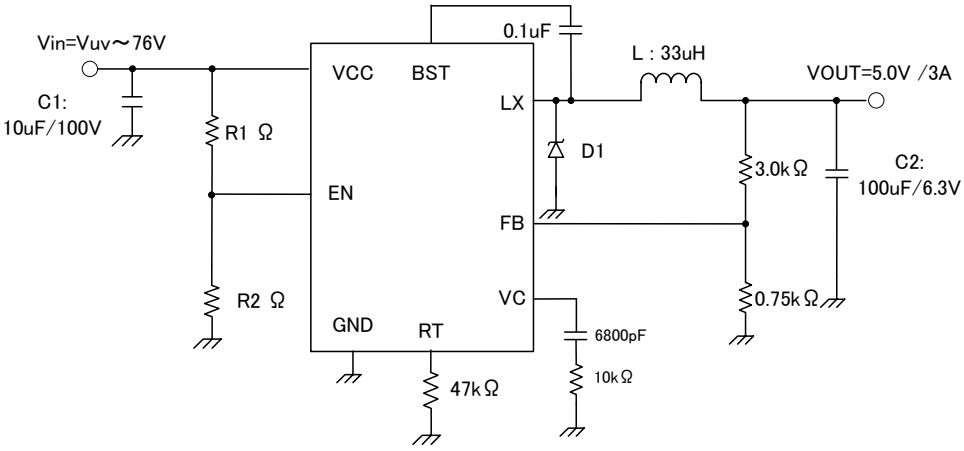

Fig.30 External UVLO setup

$$R1 = \frac{Vuvhys}{IEN} \quad [ohm]$$

$$R2 = \frac{VEN \times R1}{Vuv - VEN} \quad [ohm]$$

IEN:EN pin source current 10uA(typ) VEN: EN pin output on threshold 2.6V(typ)

As an example in typical sample, When Vcc voltage which IC turned on 15V, Hysteresis width 1V, The resistance divider set to R1=100kΩ,R2=20kΩ.

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◇OCP operation

The device has over current protection for protecting the FET from over current.
To detect OCP 2 times sequentially, the device will stop and after 20msec restart.

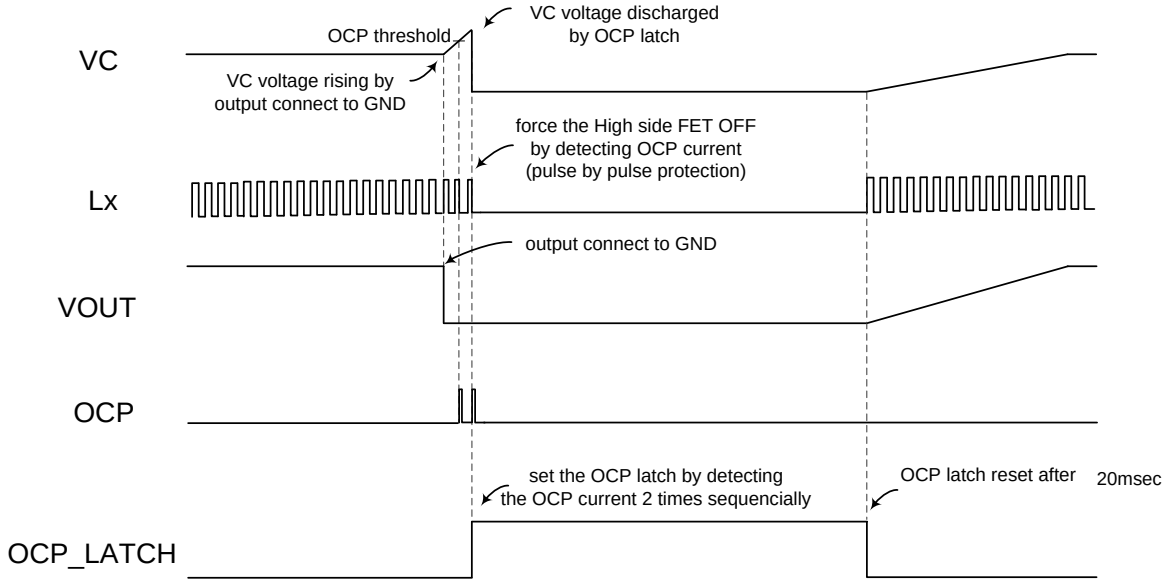

Fig.31 Timing chart at OCP operation

◇start up with output pre-bias voltage

It starts in the state that the voltage remains in the output , in the cases that big capacitor is connected to output ,
IC discharge output voltage min 7.5V by FET ON 300nsec in period to charge bootstrap capacitor between BST to LX.
When it is necessary to make a startup sequence, Please forcibly discharge the output voltage.

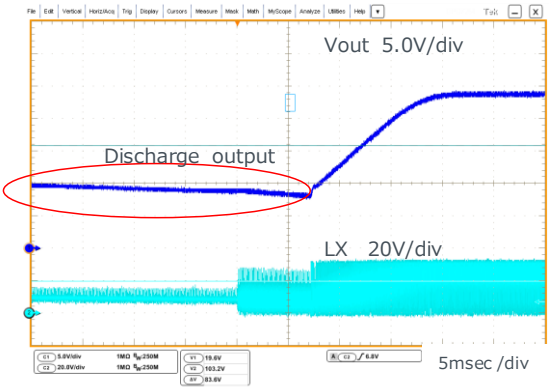

Figure 32. pre-bias start up waveform
VCC=48V Vout=24V

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◇Restriction of output Bias application

The application that output connects to the other power supply is not recommended because the output voltage is not discharged in startup.

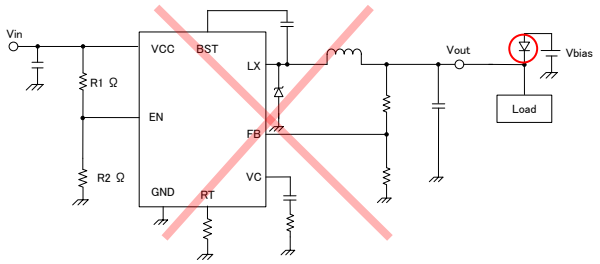

Figure 33. Output Bias NG application

When output connect to voltage supply, Please insert a diode to the IC output side.

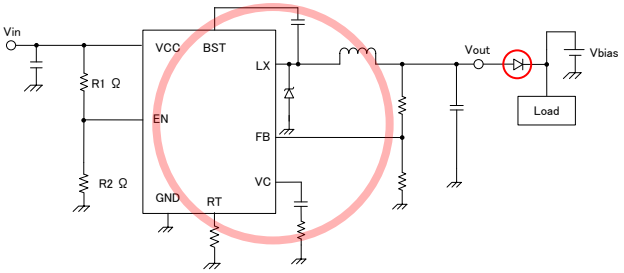

Figure 34. Output Bias OK application

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●Application Components Selection Method

(1) Inductors

Something of the shield type that fulfills the current rating (Current value Ipeak below), with low DCR is recommended. Value of Inductance influences Inductor Ripple Current and becomes the cause of Output Ripple.
In the same way as the formula below, this Ripple Current can be made small for as big as the L value of Coil or as high as the Switching Frequency.

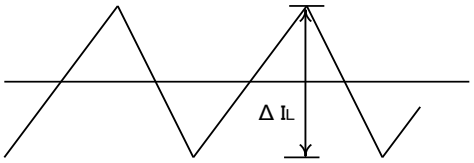

Fig.35 inductor Current

$$Ipeak = IOUT + \frac{\Delta IL}{2} \quad \cdots \quad (1)$$

$$\Delta IL = \frac{VCC - VOUT}{L} \times \frac{VOUT}{VCC} \times \frac{1}{f} \quad \cdots \quad (2)$$

(⊿IL: Output Ripple Current, VCC: Input Voltage, VOUT: Output Voltage, f: Switching Frequency)
For design value of Inductor Ripple Current, please carry out design tentatively with about 20% to 50% of Maximum Input Current.
In the BD9G341AEFJ, it is recommended the below series of 4.7μH to 33μH inductance value.
Recommended Inductor：SUMIDA　CDRH129HF Series

(2) Output Capacitor

In order for capacitor to be used in output to reduce output ripple, Low ceramic capacitor of ESR is recommended.
Also, for capacitor rating, on top of putting into consideration DC Bias characteristics, please use something whose maximum rating has sufficient margin with respect to the Output Voltage.
Output ripple voltage is looked for using the following formula.

$$V_{PP} = \Delta IL \times \frac{1}{2\pi \times f \times COUT} + \Delta IL \times R_{ESR} \quad \cdots \quad (3)$$

Please design in a way that it is held within Capacity Ripple Voltage.
In the BD9G341AEFJ, it is recommended a ceramic capacitor over 10μF.

The maximum value of the output capacitor　is limited by Start up Rush current
The rush current　is expressed by the following

(Rush Current)=（Current of the error amplifier reply delay）+ $\frac{C_{out} \times V_{out}}{T_{softstart_min}}$ +Ripple Current　+Output Current

↑
(Out put Capacitor Charge current)

Current of the error amplifier reply delay depend　on the phase compensation element and output capacitor.
As output　capacitor　big,　Rush Current grows big.
Please verify actual equipments that the Rush Current become　smaller than　OCP Threshold(min3.5A).

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(3) Output voltage setting

The internal reference voltage of ERROR AMP is 1.0V.
Output voltage is determined like (4) types.

$$VOUT = \frac{R1 + R2}{R2} \quad \cdots \quad (4)$$

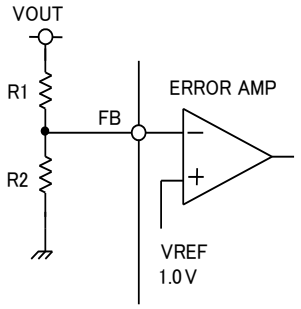

Fig.36 Output voltage setting

(4) Bootstrap Capacitor

Please connect from 0.1uF (Laminate Ceramic Capacitor) between BST Pin and Lx Pins.

(5) Catch Diode

BD9G341AEFJ should be taken to connect external catch diode between Lx Pin and GND Pin. The diode require adherence to absolute maximum Ratings of application. Opposite direction voltage should be higher than maximum voltage of Lx Pin (VCCMAX + 0.5V). The peak current is required to be higher than IOUTMAX +⊿IL.

(6) Input Capacitor
BD9G341AEFJ needs an input decoupling capacitor. It is recommended a low ceramic capacitor ESR over 4.7μF. Additionally, it should be located as close as possible.
Capacitor should be selected by maximum input voltage with input ripple voltage.
Input ripple voltage is calculated by using the following formula.

$$\Delta VCC = \frac{IOUT}{f \times CVCC} \times \frac{VOUT}{VCC} \times \left[1 - \frac{VOUT}{VCC}\right] \cdots \quad (5)$$

CVCC: Input capacitor
RMS ripple current is calculated by using the following formula.

$$I_{CVCC} = IOUT \times \sqrt{\frac{VOUT}{VCC} \times (1 - \frac{VOUT}{VCC})} \quad \cdots \quad (6)$$

If VCC=2VOUT, RMS ripple current is maximum. That is determined by (9) .

$$I_{CVCC_max} = \frac{IOUT}{2} \quad \cdots \quad (7)$$

(7) About Adjustment of DC/DC Comparator Frequency Characteristics
Role of Phase compensation element C1, C2, R3

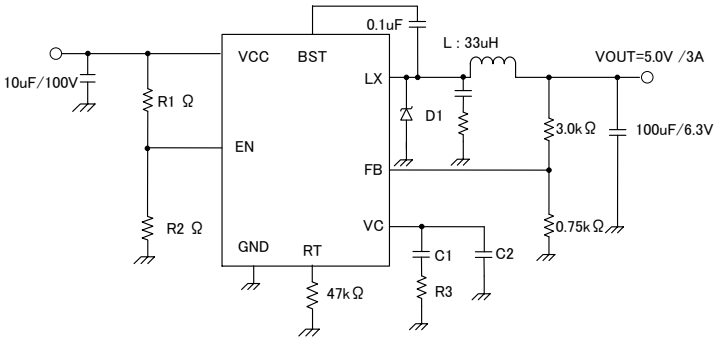

Fig.37 Feedback voltage resistance setting method

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Stability and Responsiveness of Loop are controlled through VC Pin which is the output of Error Amp.
The combination of zero and pole that determines Stability and Responsiveness is adjusted by the combination of resistor and capacitor that are connected in series to the VC Pin.

DC Gain of Voltage Return Loop can be calculated for using the following formula.

$$Adc = Rl \times \mathrm{G_{CS}} \times \mathrm{A_{VEA}} \times \frac{\mathrm{VFB}}{\mathrm{VOUT}} \quad \cdots \quad (8)$$

Here, VFB is Feedback Voltage (1.0V).A_{EA} is Voltage Gain of Error amplifier (typ: 80dB),
Gcs is the Trans-conductance of Current Detect (typ: 10A/V), and Rl is the Output Load Resistance value.

There are 2 important poles in the Control Loop of this DC/DC.
The first occurs with/ through the output resistance of Phase compensation Capacitor (C1) and Error amplifier.
The other one occurs with/through the Output Capacitor and Load Resistor.
These poles appear in the frequency written below.

$$fp1 = \frac{\mathrm{G_{EA}}}{2\pi \times \mathrm{C1} \times \mathrm{A_{VEA}}} \quad \cdots \quad (9)$$

$$fp2 = \frac{1}{2\pi \times \mathrm{COUT} \times Rl} \quad \cdots \quad (10)$$

Here, G_{EA} is the trans-conductance of Error amplifier (typ: 300 µA/V).

Here, in this Control Loop, one zero becomes important. With the zero which occurs because of Phase compensation Capacitor C1 and Phase compensation Resistor R3, the Frequency below appears.

$$fz1 = \frac{1}{2\pi \times \mathrm{C1} \times R3} \quad \cdots \quad (11)$$

Also, if Output Capacitor is big, and that ESR (RESR) is big, in this Control Loop, there are cases when it has an important, separate zero (ESR zero).
This ESR zero occurs due to ESR of Output Capacitor and Capacitance, and exists in the Frequency below.

$$fz_{ESR} = \frac{1}{2\pi \times \mathrm{COUT} \times RESR} \quad \cdots \quad (12)$$

(ESR zero)

In this case, the 3rd pole determined with the 2nd Phase compensation Capacitor (C2) and Phase Correction Resistor (R3) is used in order to correct the ESR zero results in Loop Gain.
This pole exists in the frequency shown below.

$$fp3 = \frac{1}{2\pi \times \mathrm{C2} \times R3} \quad \cdots \quad (13)$$

(Pole that corrects ESR zero)

The target of Phase compensation design is to create a communication function in order to acquire necessary band and Phase margin.

Cross-over Frequency (band) at which Loop gain of Return Loop becomes “0” is important.
When Cross-over Frequency becomes low, Power supply Fluctuation Response, Load Response, etc worsens.
On the other hand, when Cross-over Frequency is too high, instability of the Loop can occur.
Tentatively, Cross-over Frequency is targeted to be made 1/20 or below of Switching Frequency.

Selection method of Phase Compensation constant is shown below.

1. Phase Compensation Resistor (R3) is selected in order to set to the desired Cross-over Frequency.
   Calculation of RC is done using the formula below.

$$R3 = \frac{2\pi \times \mathrm{COUT} \times \mathrm{fc}}{G_{EA} \times \mathrm{G}_{CS}} \times \frac{VOUT}{VFB} \quad \cdots \quad (14)$$

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Here, fc is the desired Cross-over Frequency. It is made about 1/20 and below of the Normal Switching Frequency (fs).

2. Phase compensation Capacitor (C1) is selected in order to achieve the desired phase margin.
In an application that has a representative Inductance value (about several 4.7µH to 33µH), by matching zero of compensation to 1/4 and below of the Cross-over Frequency, sufficient Phase margin can be acquired. C1 can be calculated using the following formula.

$$C1 > \frac{4}{2\pi \times R3 \times fc} \quad \cdots \quad (15)$$

3. Examination whether the second Phase compensation Capacitor C2 is necessary or not is done.
If the ESR zero of Output Capacitor exists in a place that is smaller than half of the Switching Frequency, a second Phase compensation Capacitor is necessary. In other words, it is the case wherein the formula below happens.

$$\frac{1}{2\pi \times COUT \times RESR} < \frac{fs}{2} \quad \cdots \quad (16)$$

In this case, add the second Phase compensation Capacitor C2, and match the frequency of the third pole to the Frequency fp3 of ESR zero.

$$C2 = \frac{COUT \times RESR}{R3} \quad \cdots \quad (17)$$

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PCB Layout

Layout is a critical portion of good power supply design. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VCC pin should be bypassed to ground with a low ESR ceramic bypass capacitor with B dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VCC pin, and the anode of the catch diode. See Fig.28 for a PCB layout example. The GND pin should be tied directly to the thermal pad under the IC and the thermal pad. In order to reduce the influence of the impedance and L of the parasitic, the high current line is thick and short.

Input decoupling capacitor should be located as close to the VCC pins

In order to minimize the parasitic capacitor and impedance of pattern, catch diode and inductance should be located as close to the Lx pin.

The thermal pad should be connected to any internal PCB ground planes using multiple VIAs directly under the IC.

GND feedback resistor, phase compensation element and RT resistor don't give the common impedance resistor against high current line.

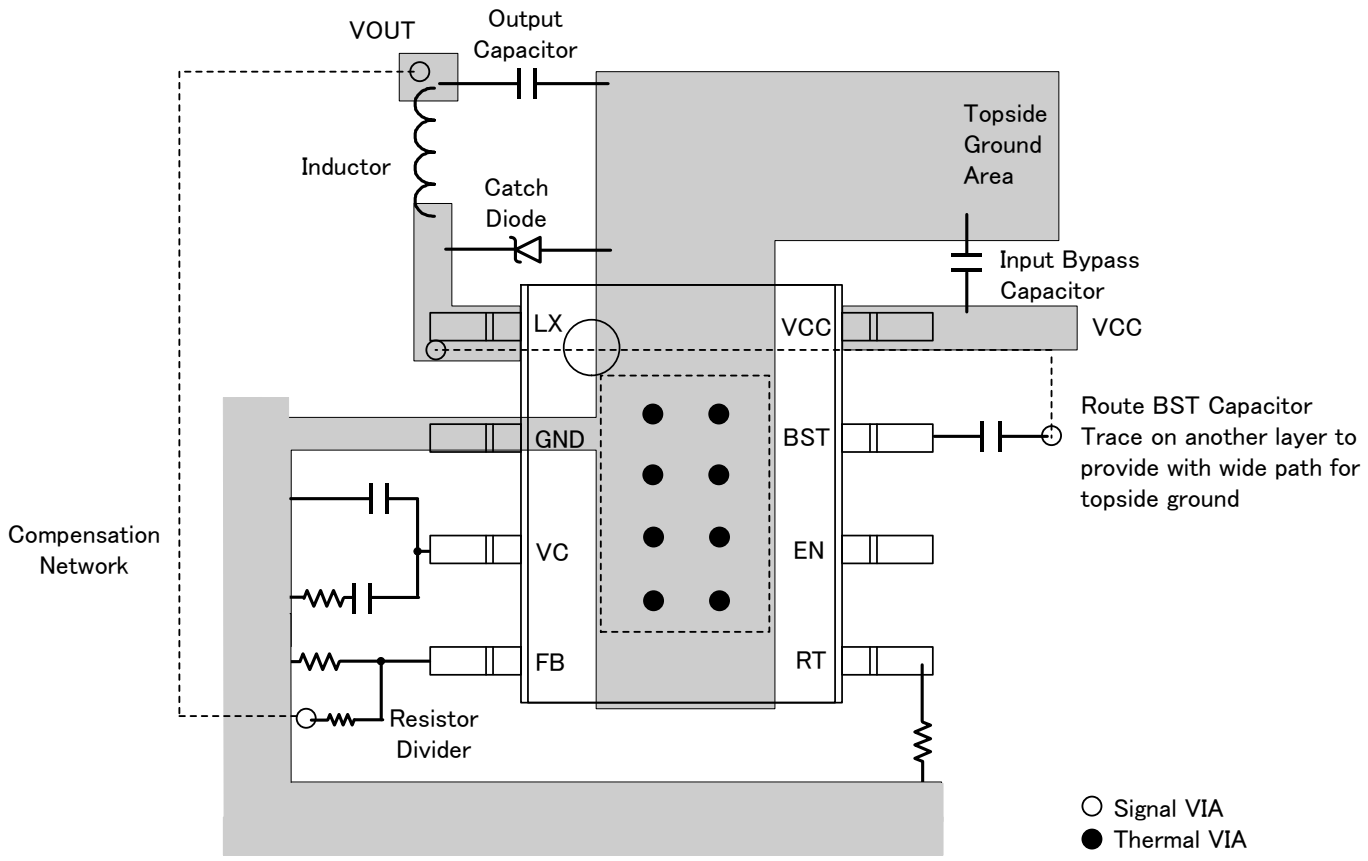

Figure 38. Evaluation Board Pattern

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Power Dissipation

It is shown below reducing characteristics of power dissipation to mount 70mm×70mm×1.6mm^t PCB
Junction temperature must be designed not to exceed 150°C.

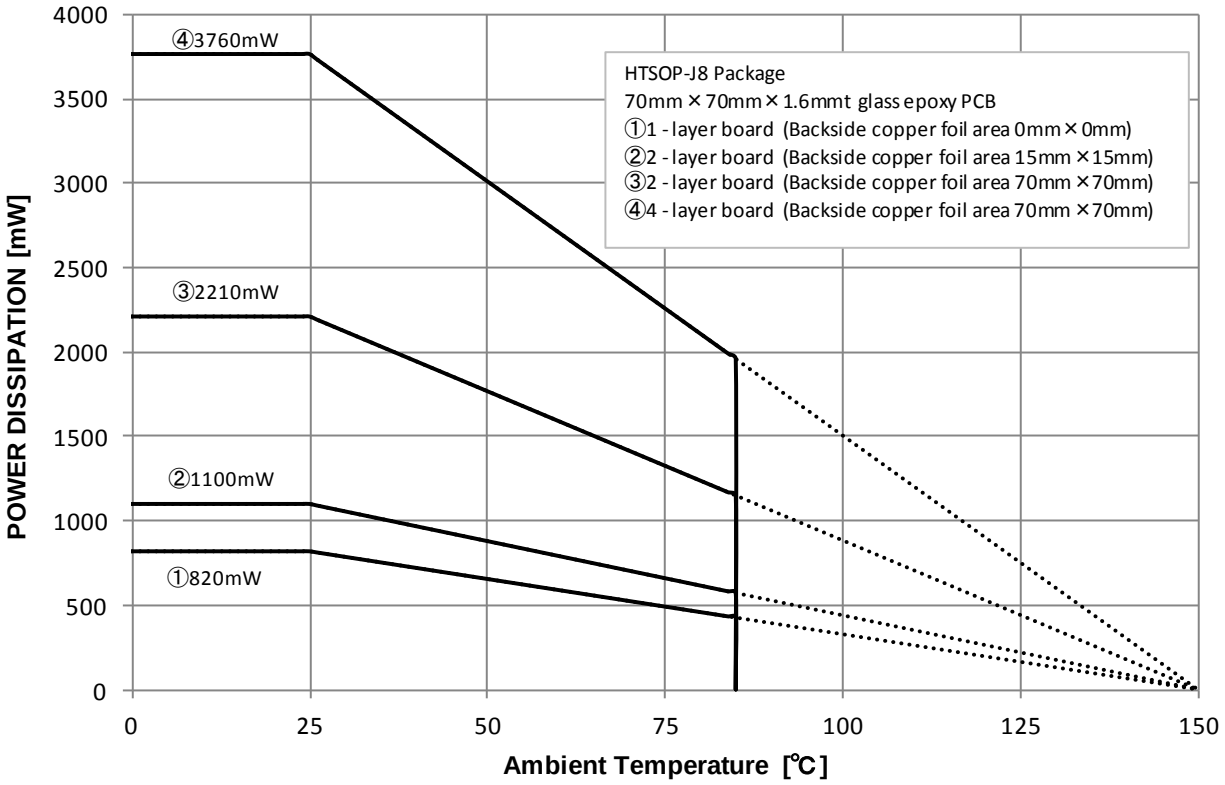

Figure 39.Power Dissipation Characteristic

Power Dissipation Estimate

The following formulas show how to estimate the device power dissipation under continuous mode operations. They should not be used if the device is working in the discontinuous conduction mode.
The device power dissipation includes:

1) Conduction loss：$Pcon = IOUT^2 \times RonH \times VOUT/VCC$
2) Switching loss： $Psw = 16n \times VCC \times IOUT \times fsw$
3) Gate charge loss：$Pgc = 500p \times 7 \times 7 \times fsw$
4) Quiescent current loss：$Pq = 1.5m \times VCC$

Where:
IOUT is the output current (A)，RonH is the on-resistance of the high-side MOSFET（Ω），VOUT is the output voltage (V).
VCC is the input voltage (V) fsw is the switching frequency (Hz).
Therefore
Power dissipation of IC is the sum of above dissipation.
$Pd = Pcon + Psw + Pgc + Pq$
For given Tj, $Tj = Ta + \theta ja \times Pd$
Where:
Pd is the total device power dissipation (W), Ta is the ambient temperature (°C)
Tj is the junction temperature (°C), θja is the thermal resistance of the package (°C)

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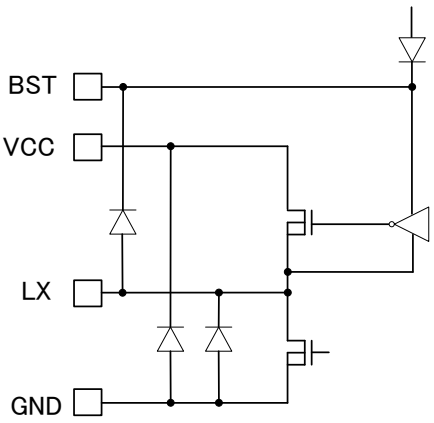
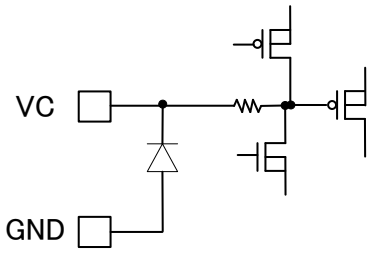
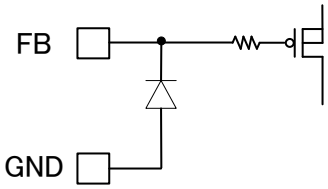
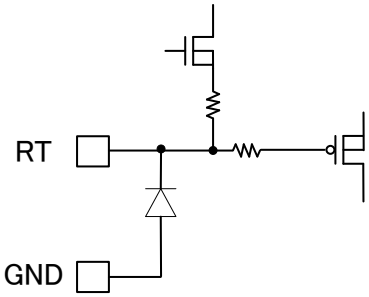
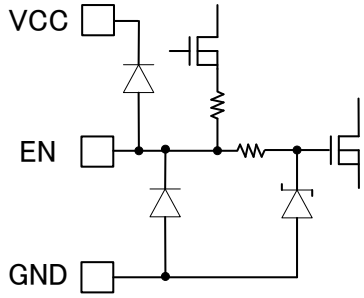
I/O Equivalent Schematic

Pin. No	Pin. Name	Pin Equivalent Schematic
1 2 7 8	Lx GND BST VCC	
3	VC	
4	FB	

Pin. No	Pin. Name	Pin Equivalent Schematic
5	RT	
6	EN	

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.
   OR

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

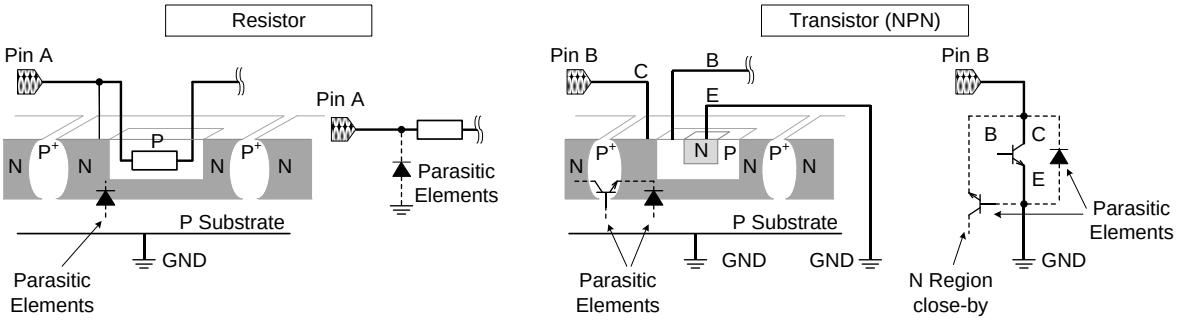

Figure 40. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

Operational Notes – continued

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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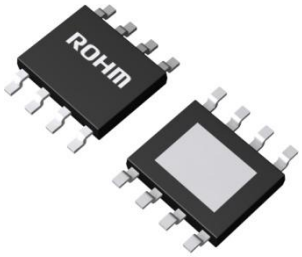
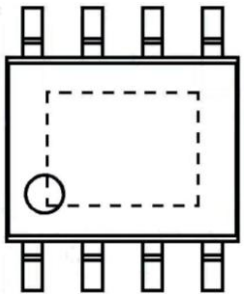
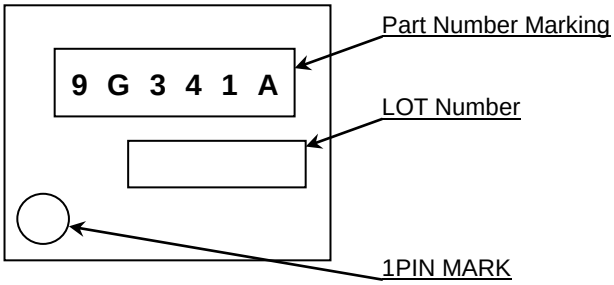
Ordering Information

B D 9 G 3 4 1 A E F J - E2

- Part Number
- Package
  EFJ: HTSOP-J8
- Packaging and forming specification :
  Embossed tape and reel

Marking Diagrams

HTSOP-J8		
4.90mm x 6.00mm x 1.00mm		
	HTSOP-J8 (TOP VIEW) 	HTSOP-J8(TOP VIEW) 

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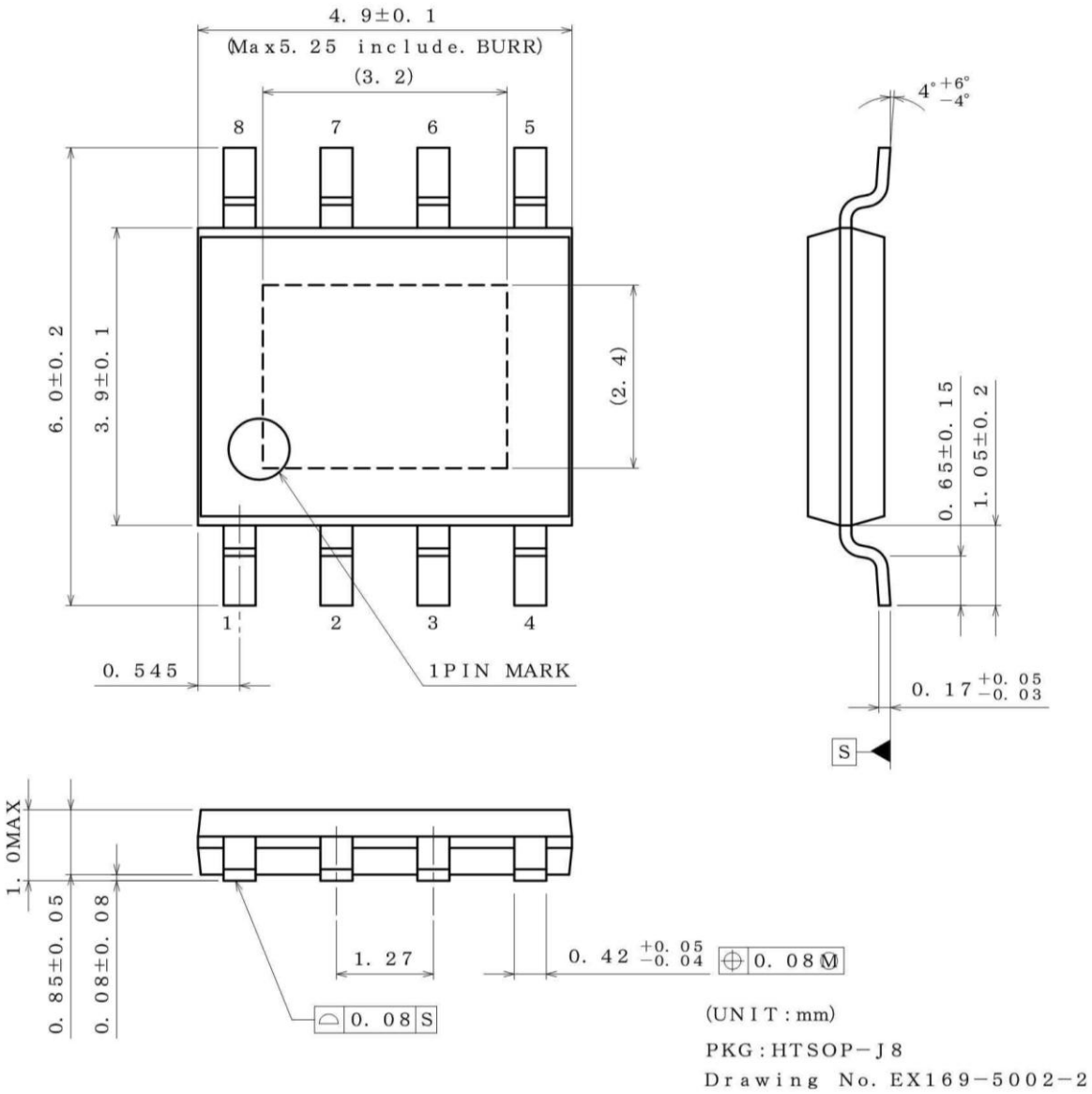
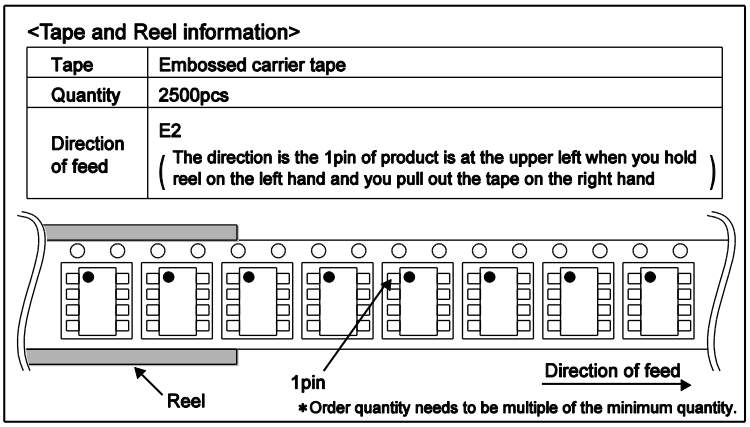
Physical Dimension, Tape and Reel Information

Package Name	HTSOP-J8





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Revision History

Date	Revision	Changes
15.Jun.2015	001	New Release
06.Oct.2015	002	P16 Correct error in writing
16.Dec.2015	003	P13 start up with output pre-bias voltage P14 Restriction of output Bias application P15 Output Capacitor maximum value
28.Sep.2016	004	Correct error in writing P20 Fig39 P20 calculation of Gate charge loss Pgc = 500p × 7 × fsw ⇒Pgc = 500p × 7 × 7 × fsw

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Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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