AIE Adaptive Image Enhancer Series

Video Encoders built-in Image Correction

BU6520KV,BU6521KV

No.10060ECT03

●Description

BU6520KV, BU6521KV are video encoders with built-in AIE image correcting function. Also, BU6521KV has the image correcting function of the fog reduction, too.
Fog Reduction, the brightness correction, the backlight correction and the chroma emphasis can improve the visibility of the input image of the camera.

* AIE and Fog Reduction function are image processing technology by ROHM's hardware.

●Features

1) Format of video output is compatible with NTSC/PAL composite video format (CVBS).
   Built-in DAC with direct 75Ω drive capability.
2) Built-in Fog Reduction function[*1], dynamic range correction, edge-emphasizing filter and gamma filter.
3) Input/output data format is compatible with ITU-R BT.656 and YCbCr=4:2:2 with synchronization signal.
4) Compatible with NTSC (27MHz, 28.63636MHz and 19.06993MHz)/
   PAL(27MHz, 28.375MHz, 35.46895MHz and 18.9375MHz) [*2].
5) Registers can be set up with a 2-line serial interface.
6) Registers can be automatically set up by reading from external EEPROM, when after resetting or changing mode.

*1 As for the Fog Reduction feature, it loads only BU6521KV.
*2 NTSC 19,06993 MHz and PAL 18,9375 MHz support only BU6521KV.

●Applications

Security camera, camera for automotive, drive recorder etc.

●Line up matrix

Part No.	Power Sopply Voltage(V)	Image size	Input Interface	Control Interface	Output Interface	Feature	Temperature Operating Range(°C)	Package
BU6520KV	1.4 to 1.6 (V_{DD}Core) 2.7 to 3.6 (V_{DD}I/O, AV_{DD})	720x480, SD size	8bit, YUV=4:2:2, ITU-R BT.656	I^2C, Serial EEPROM interface	8bit, YUV=4:2:2, ITU-R BT.656	AIE, Video output	-40 ~ +85	VQFP48C
BU6521KV	1.4 to 1.6 (V_{DD}Core) 2.7 to 3.6 (V_{DD}I/O, AV_{DD})	720x480, SD size	8bit, YUV=4:2:2, ITU-R BT.656	I^2C, Serial EEPROM interface	8bit, YUV=4:2:2, ITU-R BT.656	AIE, Fog reduction, Video output	-40 ~ +85	VQFP48C

I^2C BUS is a registered trademark of Philips

●Absolute maximum ratings

Parameter	Symbol	Rating	Unit
Supply voltage1 (IO)	VDDIO	-0.3～+4.2	V
Supply voltage2 (IO)	VDDI2C	-0.3～+4.2	V
Supply voltage3 (DAC)	AVDD	-0.3～+4.2	V
Supply voltage4 (CORE)	VDD	-0.3～+2.1	V
Input voltage range	VIN	-0.3～IO_LVL+0.3 *1	V
Storage temperature range	Tstg	-40～+125	℃
Power dissipation	PD	400 *2, 900 *3	mW

*1 IO_LVL is a generic name of VDDIO, VDDI2C, and AVDD.
*2 IC only. In the case exceeding 25ºC, 4.0mW should be reduced at the rating 1ºC.
*3 When packaging a glass epoxy board of 70x70x1.6mm. If exceeding 25ºC, 9.0mW should be reduced at the rating 1ºC.
* Has not been designed to withstand radiation.
* Operation is not guaranteed at absolute maximum ratings.

●Operating conditions

Parameter	Symbol	Ratings	Unit
Supply voltage 1 (IO)	VDDIO	2.70 ~ 3.60 (Typ.: 3.30)	V
Supply voltage 2 (IO)	VDDI2C	2.70 ~ 3.60 (Typ.: 3.30)	V
Supply voltage 3 (DAC)	AVDD	2.70 ~ 3.60 (Typ.: 3.30)	V
Supply voltage 4 (CORE)	VDD	1.40 ~ 1.60 (Typ.: 1.50)	V
Input voltage range	VIN	0.00 ~ IO_LVL *1	V
Operating temperature range	Topr	-40 ~ +85	ºC

*1 IO_LVL is a generic name of VDDIO, VDDI2C, and AVDD.
* Please supply power source in order of VDD→(VDDIO, VDDI2C, and AVDD).

●Block Diagram

[BU6520KV]

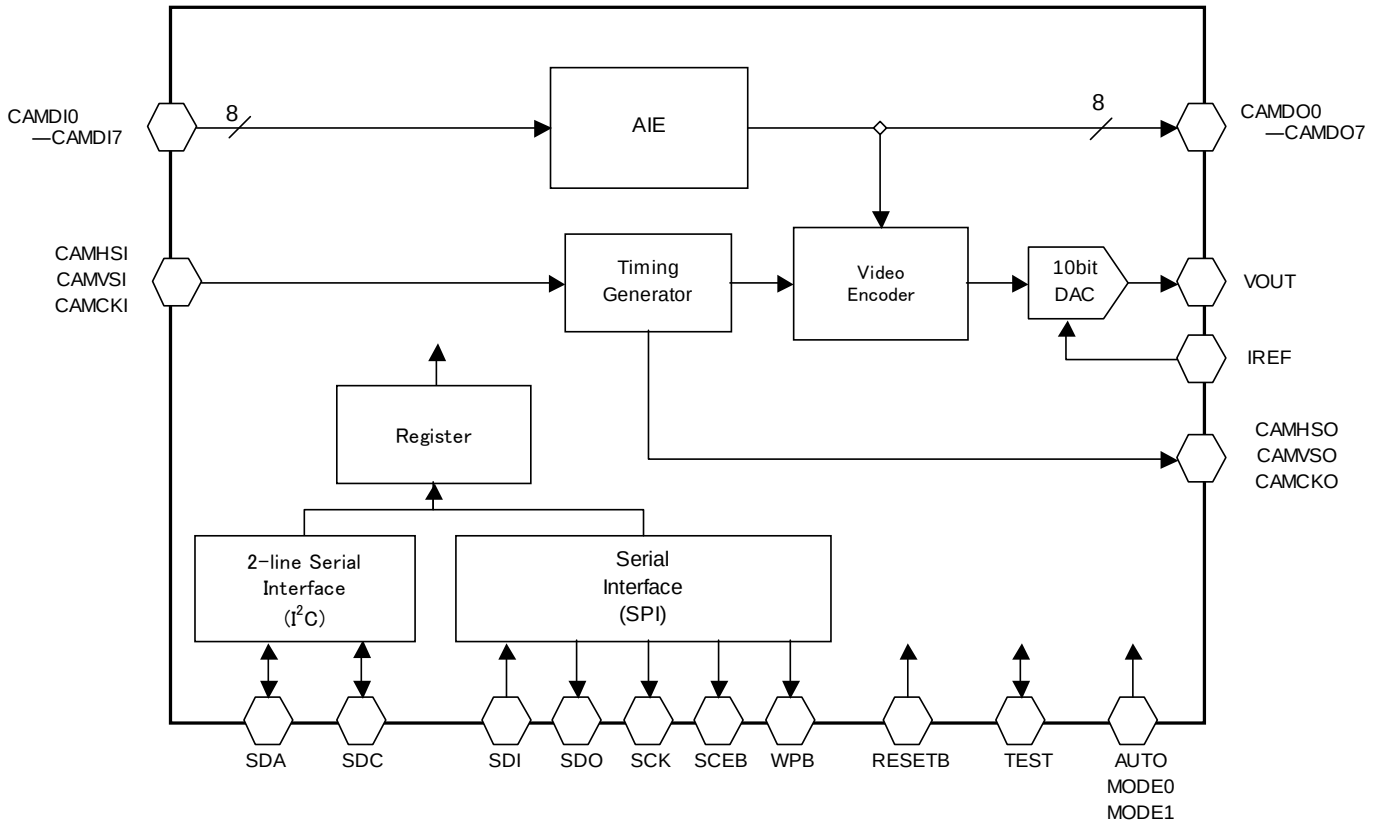


Fig.1 BU6520KV Block Diagram

[BU6521KV]

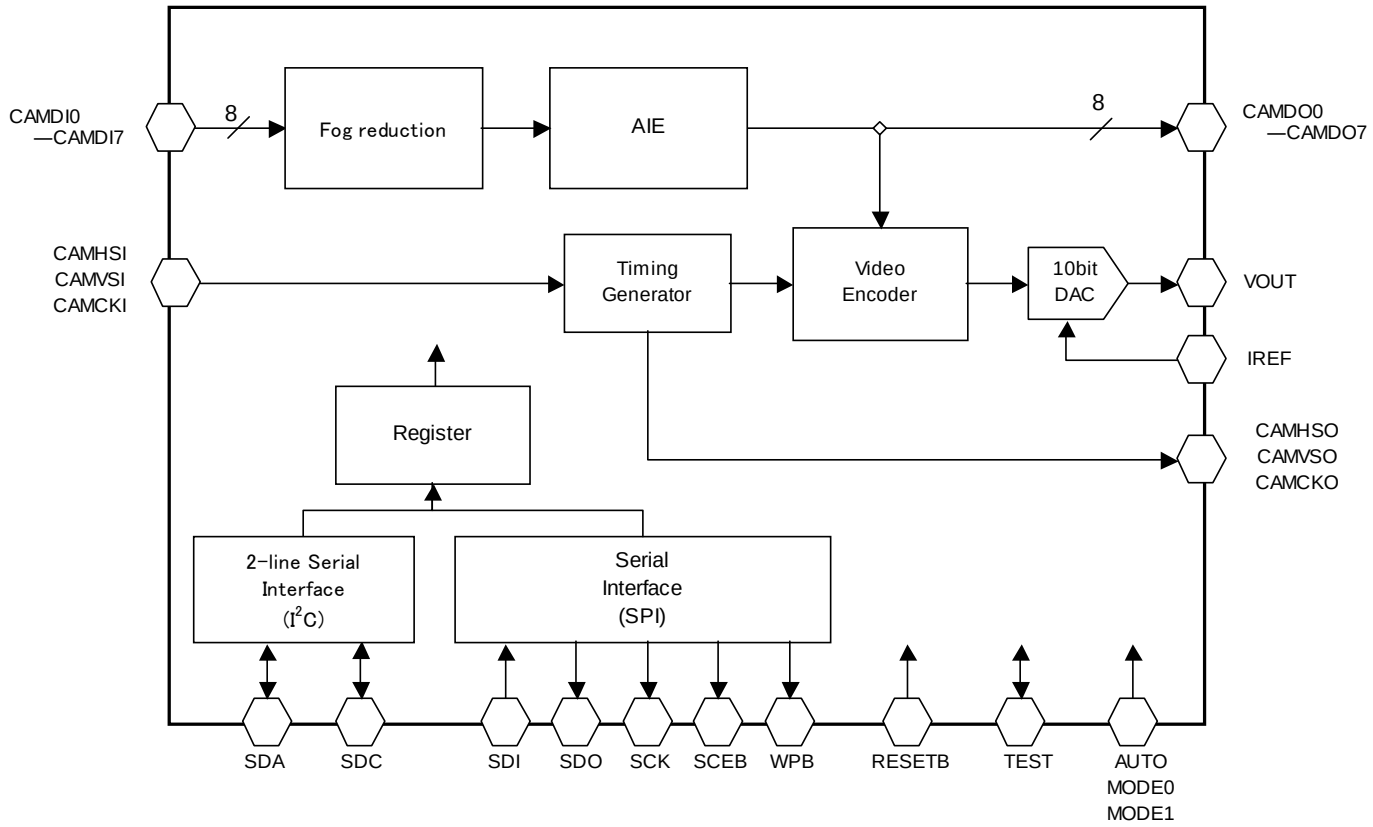


Fig.2 BU6521KV Block Diagram

●Pin functional descriptions・Equivalent circuit

PIN No.	PIN Name	In/Out	Active Level	Init	Function explanation	Power Source System	I/O type*1
1	SDI	In	DATA	-	SPI-bus data input	1	A
2	CAMDI7	In	DATA	-	Data input bit 7	1	C
3	CAMDI6	In	DATA	-	Data input bit 6	1	C
4	CAMDI5	In	DATA	-	Data input bit 5	1	C
5	CAMDI4	In	DATA	-	Data input bit 4	1	C
6	GND	-	GND	-	Common GROUND	1,2,4	-
7	VDD	-	PWR	-	CORE power source	4	-
8	CAMDI3	In	DATA	-	Data input bit 3	1	C
9	CAMDI2	In	DATA	-	Data input bit 2	1	C
10	CAMDI1	In	DATA	-	Data input bit 1	1	C
11	CAMDI0	In	DATA	-	Data input bit 0	1	C
12	CAMHSI	In	*	-	Horizontal timing input	1	C
13	CAMVSI	In	*	-	Vertical timing input	1	C
14	CAMCKI	In	CLK	-	Clock input	1	E
15	GND	-	GND	-	Common GROUND	1,2,4	-
16	VDDIO	-	PWR	-	Digital IO power source	1	-
17	CAMDO0	Out	DATA	Low	Data output bit 0	1	F
18	CAMDO1	Out	DATA	Low	Data output bit 1	1	F
19	CAMDO2	Out	DATA	Low	Data output bit 2	1	F
20	CAMDO3	Out	DATA	Low	Data output bit 3	1	F
21	CAMDO4	Out	DATA	Low	Data output bit 4	1	F
22	CAMDO5	Out	DATA	Low	Data output bit 5	1	F
23	CAMDO6	Out	DATA	Low	Data output bit 6	1	F
24	CAMDO7	Out	DATA	Low	Data output bit 7	1	F

※ " * " in the Active Level column indicates that it may be changed during set-up of the register.
※ Init column indicates pin status when released from reset.
※ In the power system column, " 1 " stands for VDDIO, " 2 " stands for VDDI2C, " 3 " stands for AVDD, " 4 " stands for VDD.
*1 Fig.3 Equivalent Circuit Structures of input / output pins reference

PIN No.	PIN Name	In/Out	Active Level	Init	Function explanation	Power Source System	I/O type*1
25	CAMHSO	Out	*	Low	Horizontal timing output	1	F
26	CAMVSO	Out	*	Low	Vertical timing output	1	F
27	CAMCKO	Out	CLK	Low	Clock output	1	F
28	GND	-	GND	-	Common GROUND	1,2,4	-
29	VDD	-	PWR	-	CORE power source	4	-
30	AUTO	In	High	PD *2	Auto register setting enable signal	1	D
31	MODE0	In	DATA	PD *2	Auto register setting mode select bit 0	1	D
32	MODE1	In	DATA	PD *2	Auto register setting mode select bit 1	1	D
33	VOUT	Out	Analog	-	Analog composite output	3	H
34	AVSS	-	GND	-	Analog GROUND for DAC	3	-
35	IREF	Out	Analog	-	Reference voltage for DAC	3	I
36	AVDD	-	PWR	-	Analog power source for DAC	3	-
37	GND	-	GND	-	Common GROUND	1,2,4	-
38	VDDI2C	-	PWR	-	Digital IO power source (For 2-line serial interface input/output)	2	-
39	SDA	In/Out	DATA	In	2-line serial interface data input/output	2	G
40	SDC	In/Out	CLK	In	2-line serial interface clock input	2	G
41	RESETB	In	Low	-	System reset signal	1	B
42	TEST	In	High	PD *2	Test mode terminal (Connect to GND)	1	D
43	GND	-	GND	-	Common GROUND	1,2,4	-
44	VDDIO	-	PWR	-	Digital IO power source	1	-
45	WPB	Out	Low	Low	Write protect signal to EEPROM	1	F
46	SCEB	Out	Low	High	Chip select signal to EEPROM	1	F
47	SCK	Out	CLK	Low	SPI-bus clock	1	F
48	SDO	Out	DATA	Low	SPI-bus data output	1	F

※ " * " in the Active Level column indicates that it may be changed during set-up of the register.
※ Init column indicates pin status when released from reset.
※ In the power system column, " 1 " stands for VDDIO, " 2 " stands for VDDI2C, " 3 " stands for AVDD, " 4 " stands for VDD.
*1 Fig.3 Equivalent Circuit Structures of input / output pins reference
*2 Pull-down status.

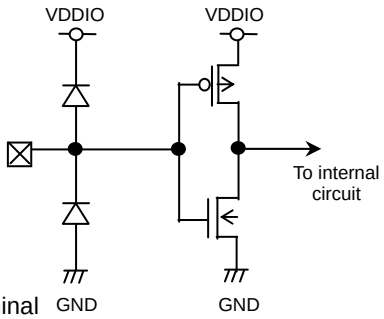
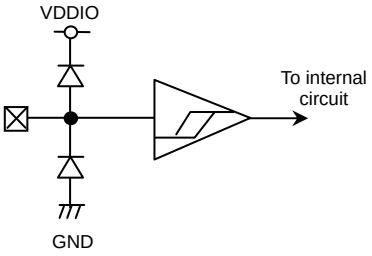
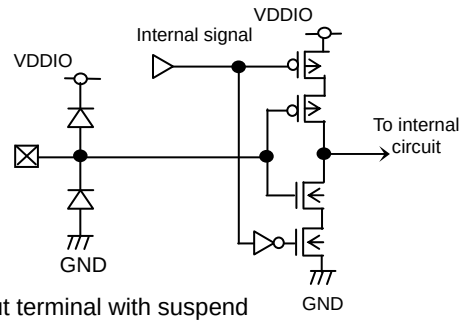
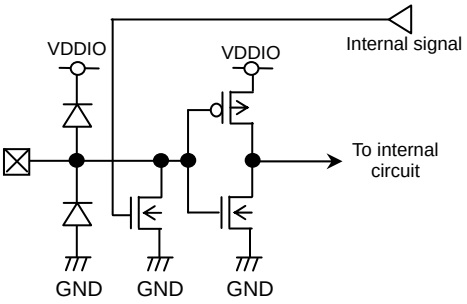
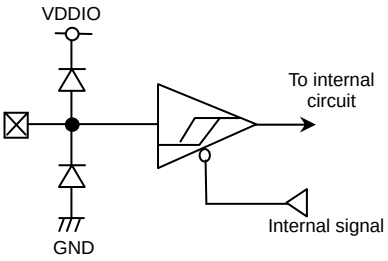
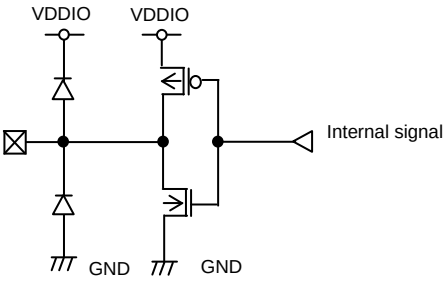
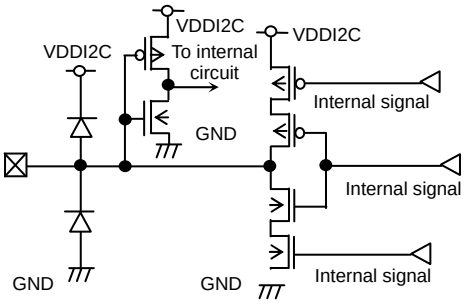
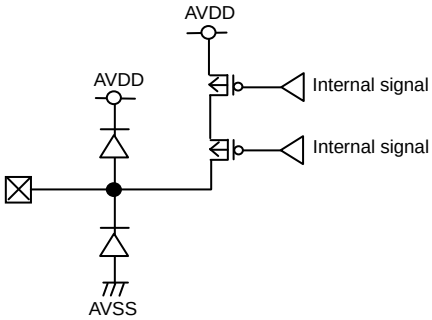
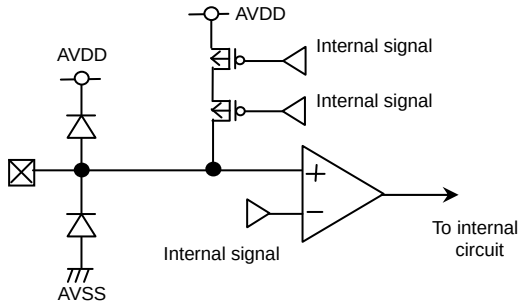
Type	Equivalent circuit configuration	Typ	Equivalent circuit configuration
A	 Input terminal	B	 Input terminal with hysteresis
C	 Input terminal with suspend	D	 Input terminal with pull down
E	 Input terminal with hysteresis and suspend	F	 Output terminal
G	 Input/Output terminal	H	 VOUT
I	 IREF		

Fig.3 Equivalent Circuit Structures of input / output pins

●Pin configrations

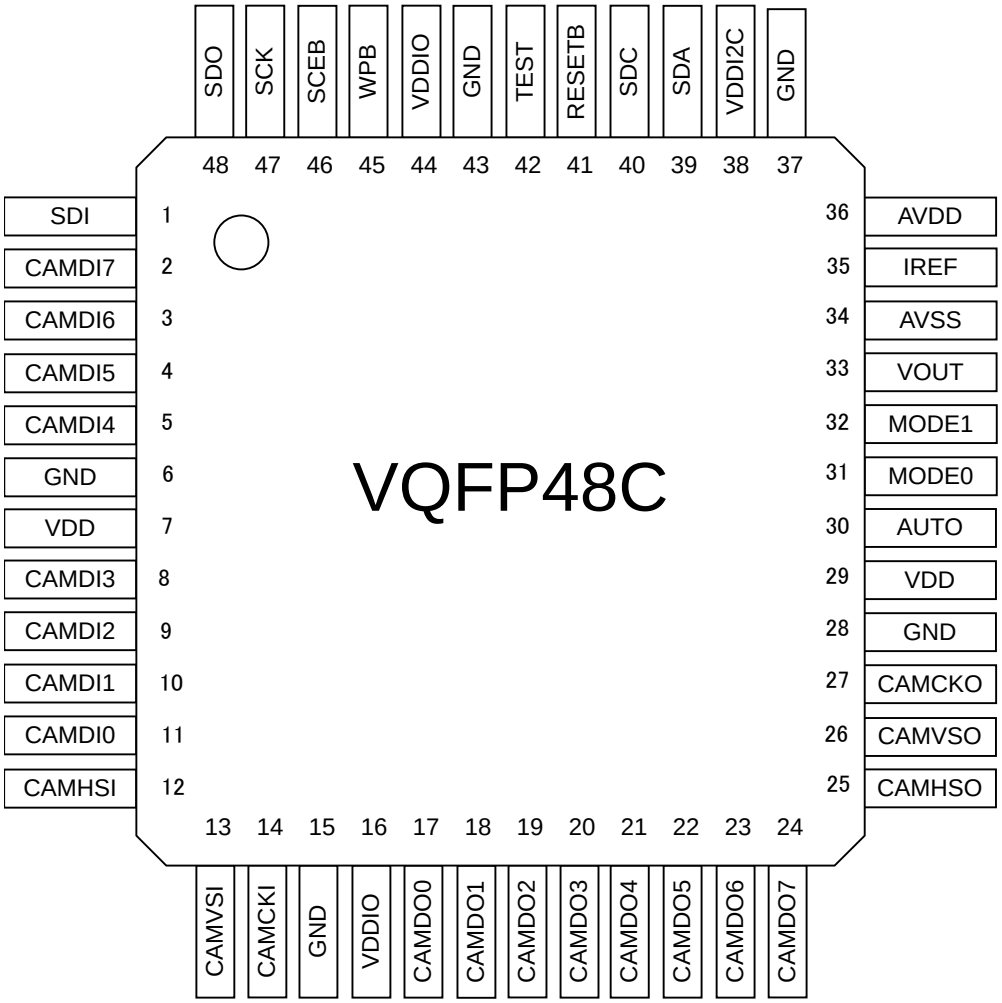


Fig.4 Pin configrations

●Electrical characteristics(common)

(Unless otherwise specified VDD=1.50V, VDDIO=3.3V, VDDI2C=3.3V, AVDD=3.3V, GND=0.0V, Ta=25℃,f_{IN}=35.5MHz)

Parameter		Symbol	Limits			Unit	Condition
			MIN.	TYP.	MAX.		
Input frequency		f_{IN}	2	-	35.5	MHz	CAMCKI(DUTY45%～55%)
Supply current (CORE)	BU6520KV	IDD1	-	30	-	mA	35.5MHz operational setting*1
	BU6521KV	IDD1	-	40	62	mA	35.5MHz operational setting*2
Leakage current (CORE)		IDDst1	-	-	50	μA	At sleep mode setting, input terminal = GND setting
Supply current (DAC)	BU6520KV	IDD2	-	38	-	mA	RL=37.5Ω, RIREF=2.4kΩ
	BU6521KV	IDD2	-	38	56	mA	RL=37.5Ω, RIREF=2.4kΩ
Leakage current (DAC)		IDDst2	-	-	5	μA	input terminal=GND and DAC power down mode setting

*1 Supply current(Total value of current of VDD, VDDIO, and VDDI2C) at color-bar image input in AIE enable and Digital output disable settings.
*2 Supply current(VDD) at color-bar image input in Fog-Reduction enable, AIE enable and Digital output disable settings.

●Electrical characteristics(DC characteristics)

1. DC characteristics (IO)

(Unless otherwise specified VDD=1.50V, VDDIO=3.3V, VDDI2C=3.3V, AVDD=3.3V, GND=0.0V, Ta=25℃)

Parameter	Symbol	Limits			Unit	Condition
		MIN.	TYP.	MAX.		
Input ”H” current	IIH	-10	-	10	μA	VIH=IO_LVL
Input ”L” current	IIL	-10	-	10	μA	VIL=GND
Pull-down current	IPD	25	50	100	μA	VIH=IO_LVL
Input ”H” voltage 1	VIH1	IO_LVL x0.8	-	IO_LVL +0.3	V	Normal input (Including input mode of I/O terminal)
Input ”L” voltage 1	VIL1	-0.3	-	IO_LVL x0.2	V	Normal input (Including input mode of I/O terminal)
Input ”H” voltage 2	VIH2	IO_LVL x0.85	-	IO_LVL +0.3	V	Hysteresis input (RESETB,CAMCKI,AUTO,MODE0,MODE1)
Input ”L” voltage 2	VIL2	-0.3	-	IO_LVL x0.15	V	Hysteresis input (RESETB,CAMCKI,AUTO,MODE0,MODE1)
Output ”H” voltage	VOH	IO_LVL -0.4	-	IO_LVL	V	IOH=-1.0mA(DC) (including output mode of I/O terminal)
Output ”L” voltage	VOL	0.0	-	0.4	V	IOL=1.0mA(DC) (including output mode of I/O terminal)

* IO_LVL is a generic name of VDDIO, VDDI2C and AVDD.

2. DC characteristics (DAC)

(Unless otherwise specified VDD=1.50V, VDDIO=3.3V, VDDI2C=3.3V, AVDD=3.3V, GND=0.0V, Ta=25℃)

Parameter	Symbol	Limits			Unit	Condition
		MIN.	TYP.	MAX.		
Integral Non-linearity	INL	-	±4.0	±8.0	LSB	RL=37.5Ω, RIREF=2.4kΩ, DAC resolution=10bit
Differential Non-linearity	DNL	-	±1.0	±2.0	LSB	RL=37.5Ω, RIREF=2.4kΩ, DAC resolution=10bit
Output Voltage (full scale)	VFS	1.1	1.25	1.4	V	RL=37.5Ω, RIREF=2.4kΩ, DAC resolution=10bit

●Electrical characteristics(AC characteristics)

1. Data Input Interface Timing

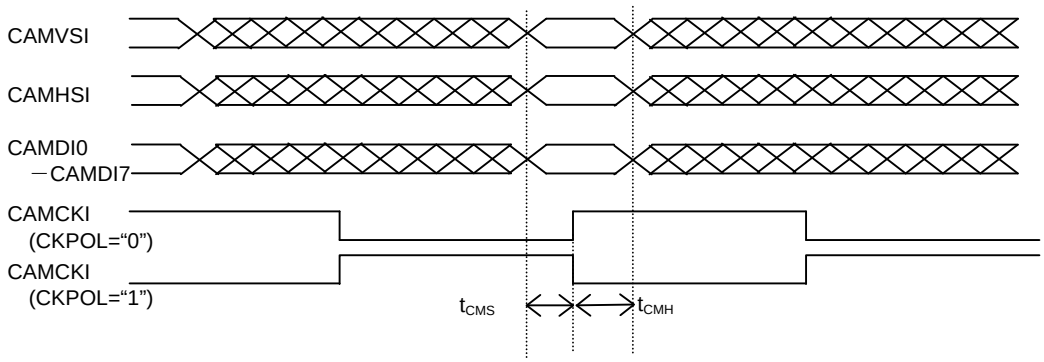


Fig.5 Data Input Interface Timing

Symbol	Description		MIN	TYP	MAX	Unit
t_{CAMCKI}	CAMCKI Clock Cycle		27.8	-	-	ns
d_{CAMCKI}	CAMCKI Clock Duty		45	50	55	%
t_{CMS}	CAMCKI Rise / Fall Camera Setup Time		8	-	-	ns
t_{CMH}	CAMCKI Rise / Fall Camera Hold Time	BU6520KV	6	-	-	ns
		BU6521KV	5	-	-	ns

* CKPOL selects the CAMCKI polarity. (CKPOL is register at BU6520KV/BU6521KV)

2. Data Output Interface Timing

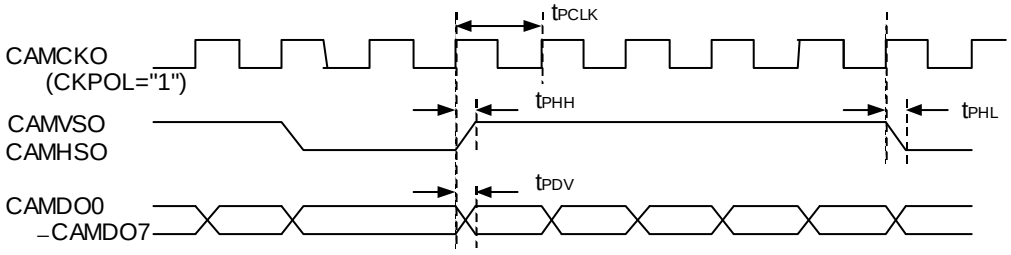


Fig.6 Data Output Interface Timing

Symbol	Description	MIN	TYP	MAX	Unit
t_{PCLK}	CAMCKO Clock Cycle	27.8	-	-	ns
d_{PCLK}	CAMCKO Clock Duty	40	50	60	%
t_{PDV}	Decision of CAMDO from CAMCKO	-	-	7	ns
t_{PHL}, t_{PHH}	Decision of CAMVSO or CAMHSO from CAMCKO	-	-	7	ns

* This figure shows CKPOL setting is ” 1 ” In case of CKPOL= ” 0 ”, CAMVSO, CAMHSO and CAMDO0-CAMCO7 change based on CAMCKO fall edge.

3. 2-line Serial Interface Timing

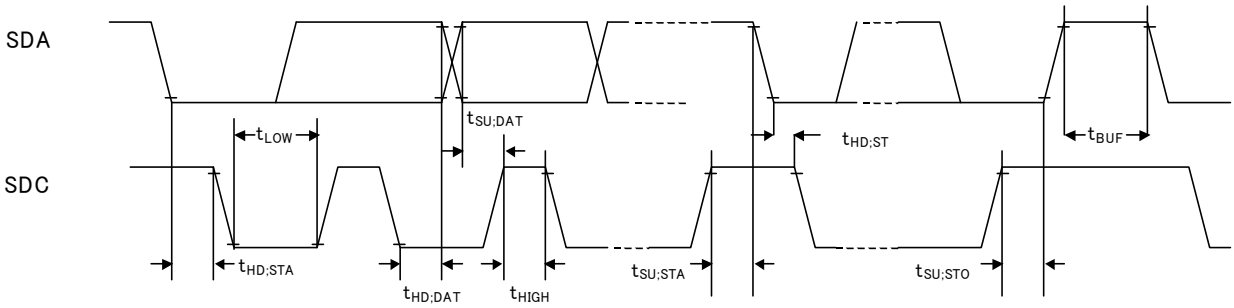


Fig.7 2-line Serial Interface Timing

Symbol	Description	MIN	TYP	MAX	Unit
f_{SCL}	SDC Clock Frequency	0	-	400	kHz
$t_{HD;STA}$	Hold Time (repetition) ”START” conditions. The first clock pulse is generated after this period.	0.6	-	-	µs
f_{LOW}	The ”L” period of SDC clock	1.3	-	-	µs
t_{HIGH}	The ”H” period of SDC clock	0.6	-	-	µs
$t_{SU;STA}$	Setup Time of repetitive ”START” conditions	0.6	-	-	µs
$t_{HD;DAT}$	Data Hold Time	0			µs
$t_{SU;DAT}$	Data Setup Time	100	-	-	ns
$t_{SU;STO}$	Setup Time of the ”STOP” conditions	0.6	-	-	µs
t_{BUF}	Bus free Time between ”STOP” conditions and the ”START” conditions	1.3	-	-	µs

4. SPI-bus Interface Timing

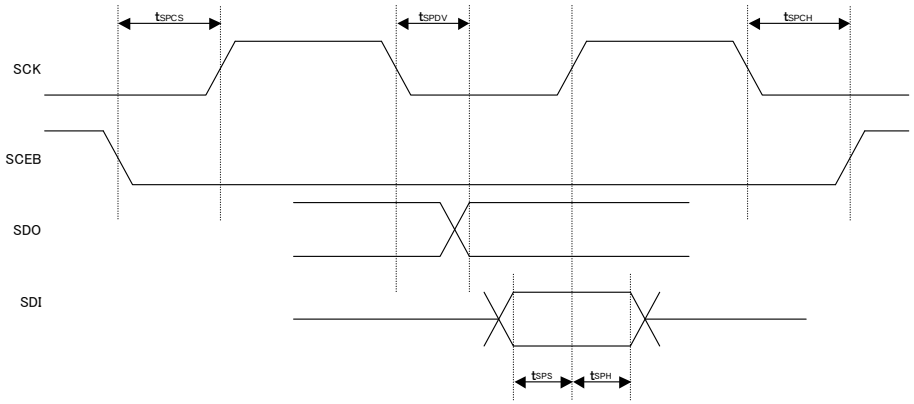


Fig.8 SPI-bus Interface Timing

Symbol	Description	MIN	TYP	MAX	Unit
t_{SPCLK}	Clock Cycle	2	736*1	8192	t_{CAMCKI}
d_{SPCLK}	Clock Duty	45	50	55	%
t_{SPCS}	SCK Rise SCEB Setup Time	4	738～1105*1	12289	t_{CAMCKI}
t_{SPCH}	SCEB Rise after SCK Rise Time	2	751*1	8319	t_{CAMCKI}
t_{SPDV}	Decision of SDO from SCK Fall	-	-	28	ns
t_{SPS}	SCK Rise SDI Setup Time	-	-	28	ns
t_{SPH}	SCK Rise SDI Hold Time	-	-	28	ns

*1 Default status right after reset

When the automatic reading function with the AUTO pin is used, it becomes timing of SCEB to SCK as above.
It is possible to access from the register of BU6520KV/BU6521KV to EEPROM.In that case, SCEB is controlled by the register.
After the value is set to the register, the SCEB pin is changed into the logic set at once.

●Functional descriptions

1. Analog Composite Output Waveform

1.1. Output waveform in NTSC

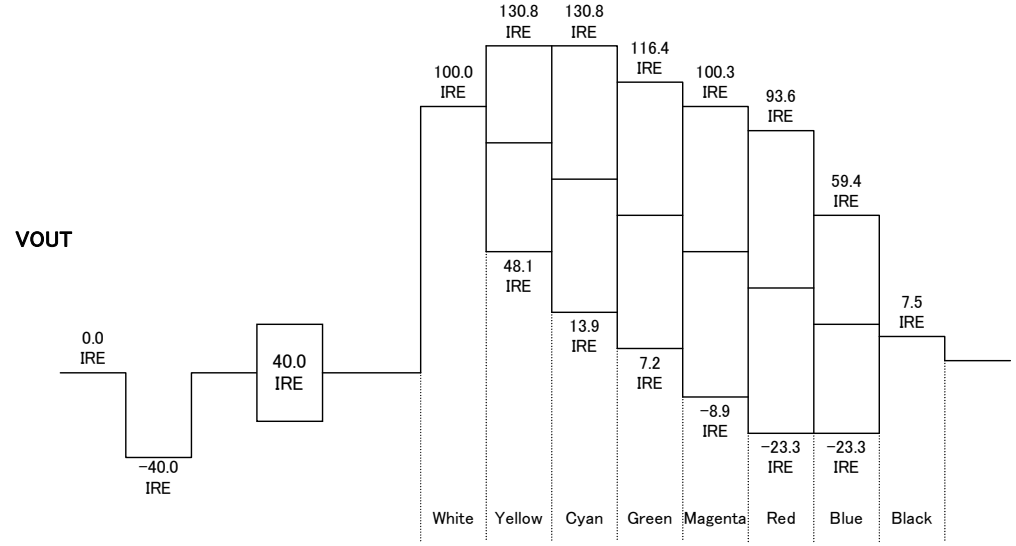


Fig.9 Color-bar corrugation in NTSC setting

1.2. Output waveform in PAL

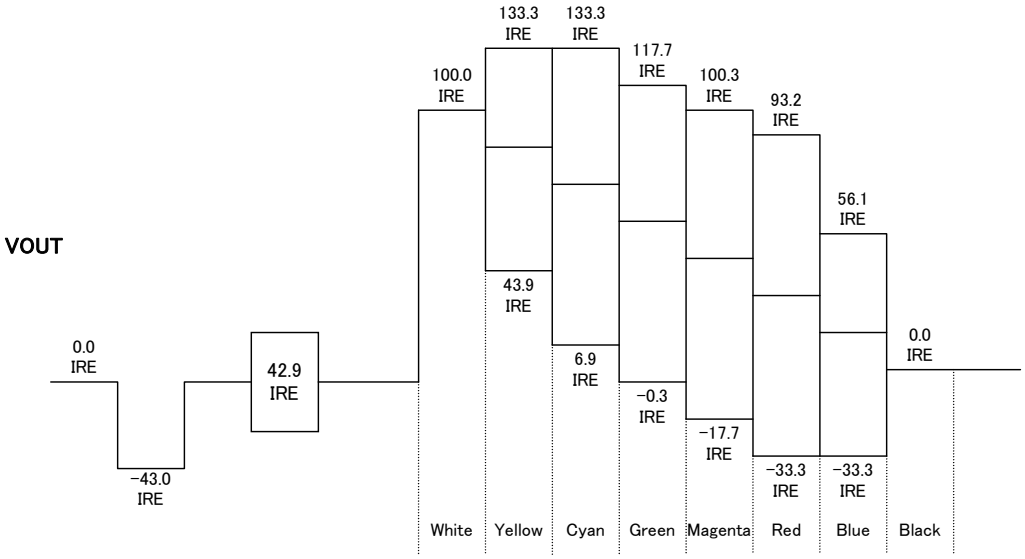


Fig.10 Color-bar corrugation in PAL setting

2. The 2 line formula serial interface format
   Slave address is 70h.
   The sub-address is incremented automatically when accessing it (read / write) continuously 2 times or more.

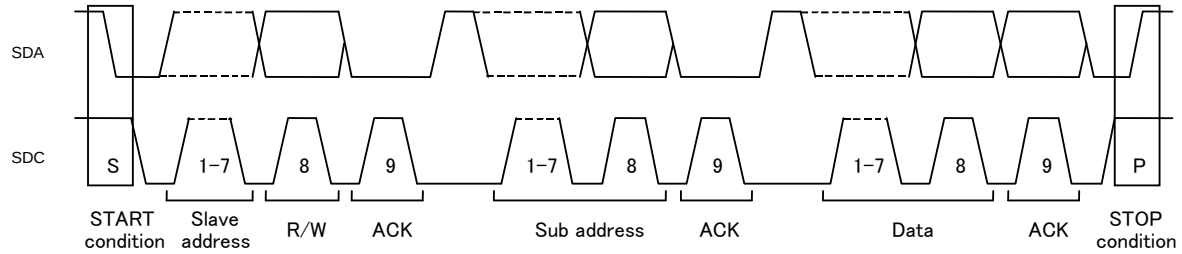


Fig.11 Waveform of date transmission part

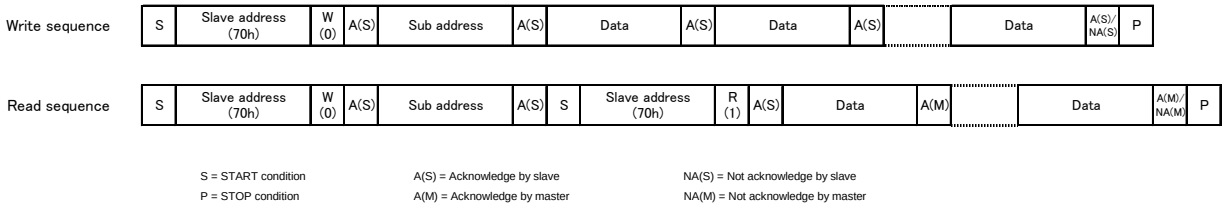


Fig.12 2-line serial interface format

3. SPI-bus format

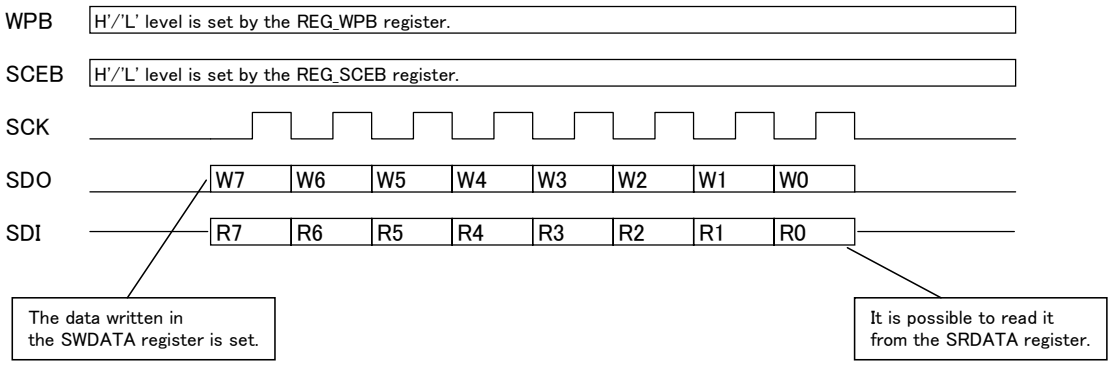


Fig.13 SPI-bus interface wave form

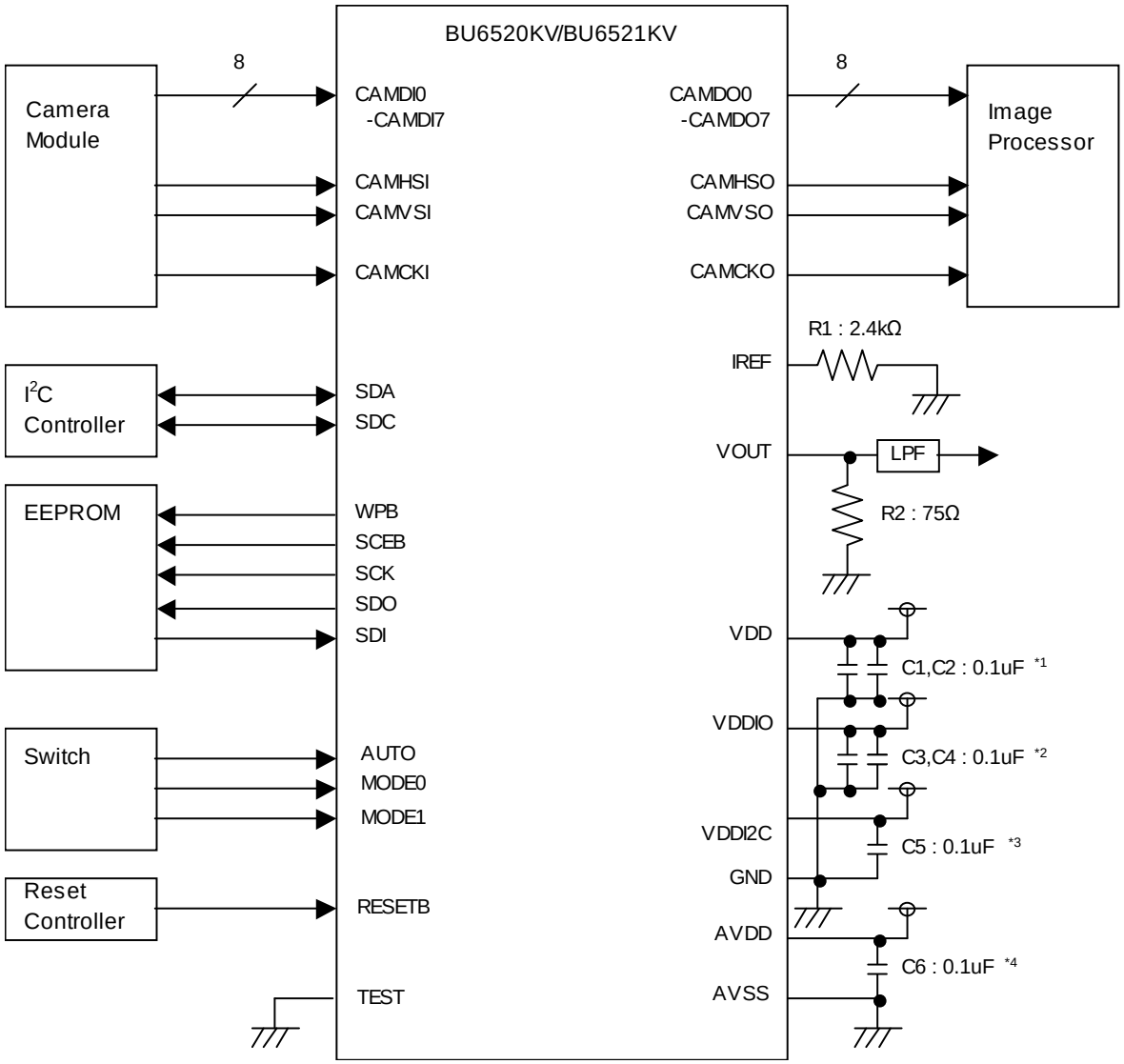
* REG_WPB, REG_SCEB, SWDATA, and SRDATA in figure are the register names, and the each function is as follows.
  REG_WPB : Set WP Terminal logic. Register value is output directly.
  REG_SCEB : Set SCEB Terminal logic. Register value is output directly.
  SWDATA[7:0] : Write data to EEPROM. Transfers MSB the first.
  SRDATA[7:0] : Read data from EEPROM. Converts MSB the first.

The SCK clock frequency is as follows.
SCK frequency = CAMCKI frequency ÷ $2^{(SPIPREDIV+1)}$ ÷ (SPIDIV+1)

Register range : SPIPREDIV = 0 to 7, SPIDIV = 0 to 31
When CAMCKI is 27MHz, SCK becomes 3.3 kHz from 13.5 MHz.

●Application example

<When registers are controlled by both of the automatic reading from EEPROM and the I^2C controller >

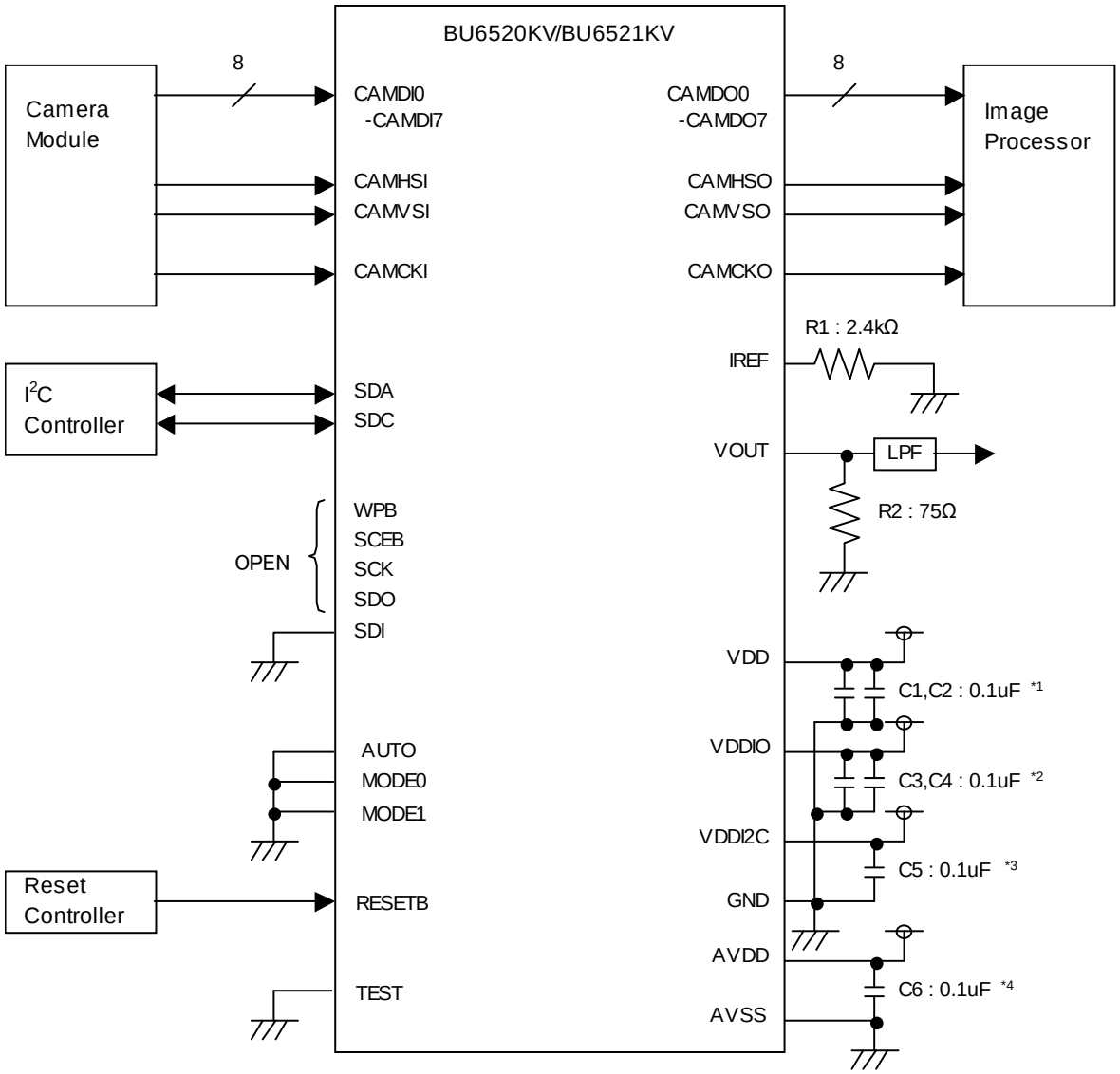


*1 Please arrange a capacitor each near two VDD pin.
*2 Please arrange a capacitor each near two VDDIO pin.
*3 Please arrange a capacitor near VDDI2C pin.
*4 Please arrange a capacitor near AVDD pin.

Fig.14 Application example 1

Fig.14 is a reference example when the system is connected, and the operation is not guaranteed.

<When registers are controlled only by the I²C controller>

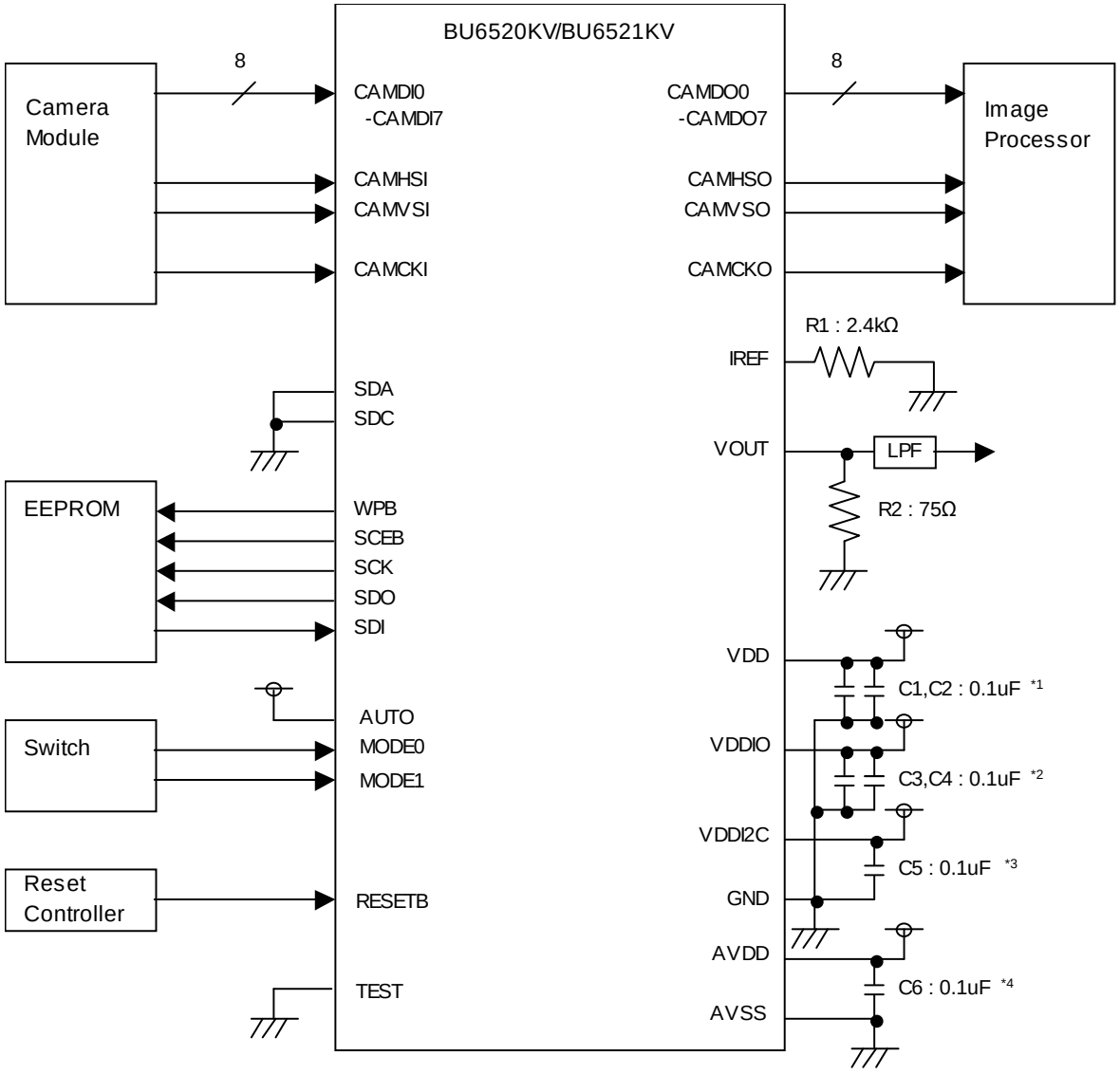


*1 Please arrange a capacitor each near two VDD pin.
*2 Please arrange a capacitor each near two VDDIO pin.
*3 Please arrange a capacitor near VDDI2C pin.
*4 Please arrange a capacitor near AVDD pin.

Fig.15 Application example 2

Fig.15 is a reference example when the system is connected, and the operation is not guaranteed.

<When registers are controlled only by the automatic reading from EEPROM >



*1 Please arrange a capacitor each near two VDD pin.
*2 Please arrange a capacitor each near two VDDIO pin.
*3 Please arrange a capacitor near VDDI2C pin.
*4 Please arrange a capacitor near AVDD pin.

Fig.16 Application example 3

Fig.16 is a reference example when the system is connected, and the operation is not guaranteed.

●Note for use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.
In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals}

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) Rush current

For ICs with more than one power supply, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of wiring.

●Ordering part number

B	U	6	5	2	0	K	V	-	E	2

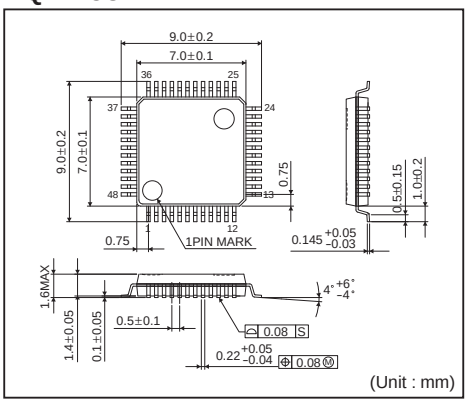
Part No.

Part No.
6520
6521

Package
KV:VQFP48C

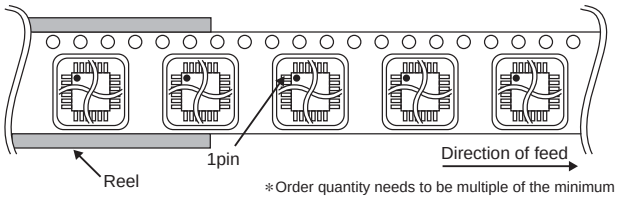
Packaging and forming specification
E2: Embossed tape and reel

VQFP48C



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

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