Regulator IC Series for Automotive

Termination Regulator for DDR-SDRAMs

BD35395FJ-M

General Description

BD35395FJ-M is a termination regulator compatible with JEDEC DDR1/2/3/3L-SDRAM, which functions as a linear power supply incorporating an N-channel MOSFET and provides a sink/source current capability up to 1A respectively. A built-in high-speed OP-AMP specially designed offers an excellent transient response. Requires 3.3 volts or 5.0 volts as a bias power supply to drive the N-channel MOSFET. Has an independent reference voltage input pin (VDDQ) and an independent feedback pin (VTTS) to maintain the accuracy in voltage required by JEDEC, and offers an excellent output voltage accuracy and load regulation.

Features

- Incorporates a push-pull power supply for termination (VTT).
- Incorporates an enabler.
- Incorporates an under voltage lockout (UVLO).
- Employs SOP-J8 package : 4.9×6.0×1.65(mm).
- Incorporates a thermal shutdown protector (TSD).
- Operates with input voltage from 2.7 to 5.5 volts.
- Compatible with Dual Channel (DDR1,DDR2,DDR3/DDR3L)
- Incorporates PGOOD function.

Applications

- Power supply for DDR1/2/3/3L SDRAM

Key Specifications

- Input Voltage Range: 2.7V to 5.5V
- Termination Input Voltage: 1.0V to 5.5V
- VDDQ Reference Voltage: 1.0V to 2.75V
- Output Current: -1.0～1.0A(Max)
- Upper Side ON Resistance: 0.35Ω(Typ)
- Lower Side ON Resistance: 0.35Ω(Typ)
- Standby Current: 0.5mA (Typ)
- Operating Temperature Range: -40°C to +105°C

Package(s)	W(Typ) x D(Typ) x H(Max)
SOP-J8	4.90mm x 6.00mm x 1.65mm

SOP-J8

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

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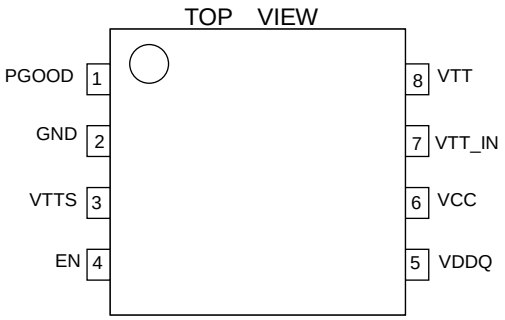
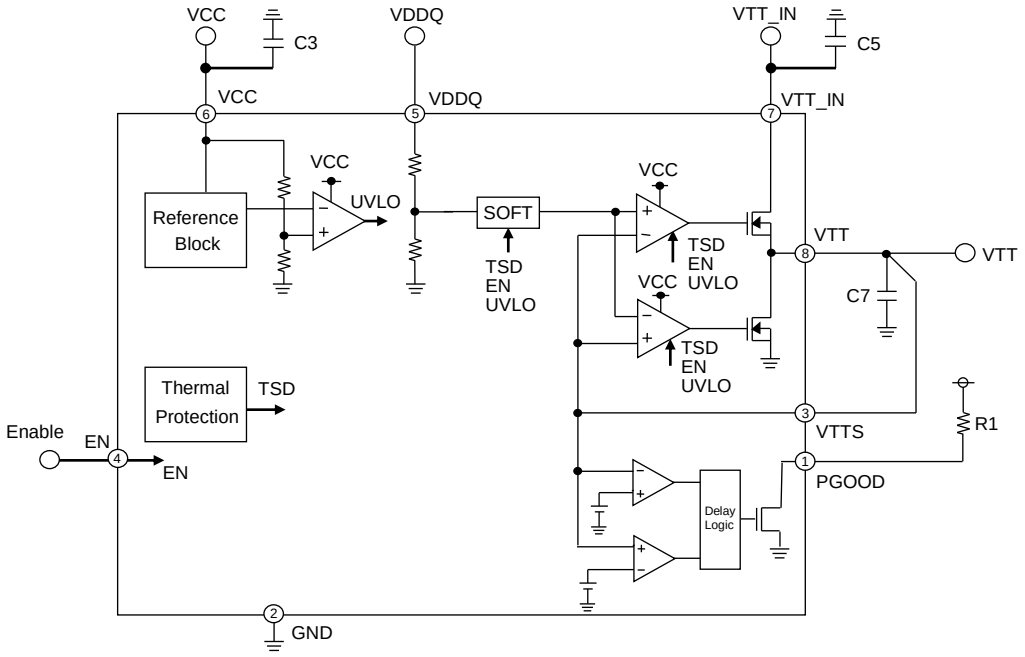
Pin Configuration(s)



Pin Description(s)

Pin No.	Pin Name	Function
1	PGOOD	PGOOD output pin
2	GND	GND
3	VTTS	Detector Pin for Termination Voltage
4	EN	ENABLE input pin
5	VDDQ	Reference Voltage Input Pin
6	VCC	VCC Pin
7	VTT_IN	Termination power supply Pin
8	VTT	Termination Output Pin

Block Diagram



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Description of Block(s)

・VCC

In BD35395FJ-M, an independent power input pin is provided for an internal circuit operation of the IC. This is used to drive the amplifier circuit of the IC, and its maximum current rating is 4mA. The power supply voltage is 2.7 to 5.5 volts. It is recommended to connect a bypass capacitor of 1μF or so to VCC.

・VDDQ

Reference input pin for the output voltage that may be used to satisfy the JEDEC requirement for DDR1/2/3/3L-SDRAM (VTT = 1/2VDDQ) by dividing the voltage inside the IC with two 100kΩ voltage-divider resistors.
For BD35395FJ-M, care must be taken to an input noise to VDDQ pin because this IC also cuts such noise input into half and provides it with the voltage output divided in half. Such noise may be reduced with an RC filter consisting of such resistance and capacitance (220Ω and 2.2μF, for instance) that may not give significant effect to voltage dividing inside the IC.

・VTT_IN

VTT_IN is a power supply input pin for VTT output. Voltage in the range between 1.0 and 5.5 volts may be supplied to this VTT_IN terminal, but care must be taken to the current limitation due to on-resistance of the IC and the change in allowable loss due to input/output voltage difference.
Generally, the following voltages are supplied:

- ・DDR1 VTT_IN=2.5V
- ・DDR2 VTT_IN=1.8V
- ・DDR3 VTT_IN=1.5V
- ・DDR3L VTT_IN=1.35V

Higher impedance of the voltage input at VTT_IN may result in oscillation or degradation in ripple rejection, which must be noted. To VTT_IN terminal, it is recommended to use a 10μF capacitor characterized with less change in capacitance. But it may depend on the characteristics of the power supply input and the impedance of the pc board wiring, which must be carefully checked before use.

・PGOOD

PGOOD pin is power good output pin. This is the open drain pin, so pull up resistor is connected via other power supply If VTT voltage becomes over 1/2 ×VDDQ+30mV,or under 1/2 ×VDDQ+30mV, it outputs High voltage.

・VTTS

An isolated pin provided to improve load regulation of VTT output. In case that longer wiring is needed to the load at VTT output, connecting VTTS from the load side may improve the load regulation.

・VTT

A DDR memory termination output pin. BD35395FJ-M has a sink/source current capability of ±1.0A respectively. The output voltage tracks the voltage divided in half at VDDQ pin. VTT output is turned to OFF when VCC UVLO or thermal shutdown protector is activated with EN pin level turned to “Low”. Do not fail to connect a capacitor to VTT output pin for a loop gain phase compensation and a reduction in output voltage variation in the event of sudden change in load. Insufficient capacitance may cause an oscillation. High ESR (Equivalent Series Resistance) of the capacitor may result in increase in output voltage variation in the event of sudden change in load. It is recommended to use a 10μF or so ceramic capacitor, though it depends on ambient temperature and other conditions.

・EN

With an input of 2.3 volts or higher, the level at EN pin turns to “High” to provide VTT output. If the input is lowered to 0.8 volts or less, the level at EN pin turns to “Low” and VTT status turns to Hi-Z.

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Absolute Maximum Ratings(Ta = 25°C)

Parameter	Symbol	Limit	Unit
Input Voltage	VCC	7 (Note1) (Note2)	V
Enable Input Voltage	VEN	7 (Note1) (Note2)	V
Termination Input Voltage	VTT_IN	7 (Note1) (Note2)	V
VDDQ Reference Voltage	VDDQ	7 (Note1) (Note2)	V
Output Current (when pulse is active(Note1 3))	ITT	1(Note1)	A
Power Dissipation1	Pd1	563(Note4)	mW
Power Dissipation2	Pd2	675(Note5)	mW
Operating Temperature Range	Topr	-40～+105	℃
Storage Temperature Range	Tstg	-55～+150	℃
Maximum Junction Temperature	Tjmax	+150	℃

(Note 1) Should not exceed Pd.
(Note 2) Instantaneous surge voltage, back electromotive force and voltage under less than 10% duty cycle.
(Note 3) Voltage under less than 10u sec.
(Note 4) Reduced by 4.50℃/W for each increase in Ta of 1℃ over 25℃ (when don't mounted on a heat radiation board)
(Note 5) Reduced by 5.40℃/W for each increase in Ta of 1℃ over 25℃ (when mounted on a 70mm×70mm×1.6mm glass epoxy board)

Recommended Operating Conditions(Ta= 25°C)

Parameter	Symbol	Limit		Unit
		MIN	MAX	
Input Voltage	VCC	2.7	5.5	V
Termination Input Voltage	VTT_IN	1.0	5.5	V
VDDQ Reference Voltage	VDDQ	1.0	2.75	V
Enable Input Voltage	VEN	-0.3	5.5	V

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Electrical Characteristics(Unless otherwise specified Ta=25℃, VCC=3.3V, VEN=3V, VDDQ=1.8V, VTT_IN=1.8V)

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
Standby Current	IST	-	0.5	1.0	mA	VEN=0V
Bias Current	ICC	-	2	4	mA	VEN=3V
[Enable]						
High Level Enable Input Voltage	VENHIGH	2.3	-	5.5	V	
Low Level Enable Input Voltage	VENLOW	-0.3	-	0.8	V	
Enable Pin Input Current	IEN	-	7	10	µA	VEN=3V
[Termination]						
Termination Output Voltage (DDR2)	VTT2	1/2×VDDQ -30m	1/2×VDDQ	1/2×VDDQ +30m	V	ITT=-1.0A to 1.0A Ta=-40℃ to 105℃
Termination Output Voltage (DDR1)	VTT1	1/2×VDDQ -30m	1/2×VDDQ	1/2×VDDQ +30m	V	VCC = 5.3V, VDDQ = 2.5V VTT_IN = 2.5V ITT=-1.0A to 1.0A Ta=-40℃ to 105℃
Termination Output Voltage (DDR3)	VTT3	1/2×VDDQ -15m	1/2×VDDQ	1/2×VDDQ +15m	V	VCC = 3.3V, VDDQ =1.5V VTT_IN =1.5V ITT=-1.0A to 1.0A Ta=-40℃ to 105℃
Termination Output Voltage (DDR3L)	VTT3L	1/2×VDDQ -13.5m	1/2×VDDQ	1/2×VDDQ +13.5m	V	VCC=3.3V, VDDQ=1.35V, VTT_IN=1.35V ITT=-1.0A to 1.0A Ta=-40℃ to 105℃
Source current	ITT+	1.0	-	-	A	
Sink current	ITT-	-	-	-1.0	A	
Load Regulation	⊿VTT	-	-	50	mV	ITT=-1.0A to 1.0A
Upper Side ON Resistance	HRON	-	0.35	0.65	Ω	
Lower Side ON Resistance	LRON	-	0.35	0.65	Ω	
[VREF]						
Input Impedance	ZVDDQ	140	200	260	kΩ	
[PGOOD]						
VTT PGOOD Low Threshold voltage	PGDLow	-	1/2×VDDQ -30m	-	V	
VTT PGOOD High Threshold Voltage	PGDHigh	-	1/2×VDDQ +30m	-	V	
PGOOD output ON resistor	PGDRon	-	10	20	Ω	
PGOOD output leakage current	PGDleak	-	-	1	µA	PGOOD=6V
PGOOD delay time	PGDdelay	1	2	4	Ms	
[UVLO]						
Threshold Voltage	VUVLO	2.35	2.50	2.65	V	VCC : sweep up
Hysteresis Voltage	⊿VUVLO	120	180	240	mV	VCC : sweep down

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Typical Performance Curves

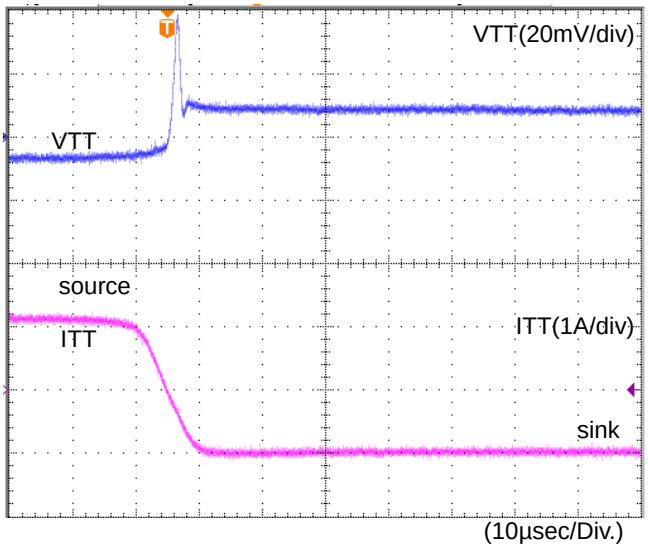

Figure 1. DDR3 (-1A→1A)

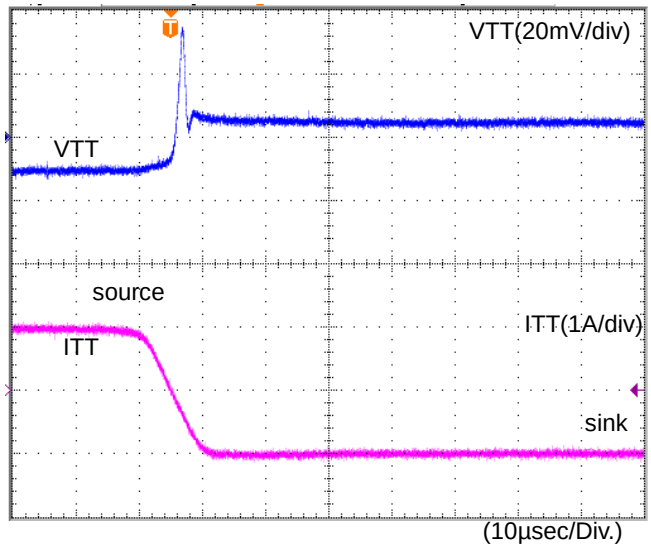

Figure 2. DDR2 (-1A→1A)

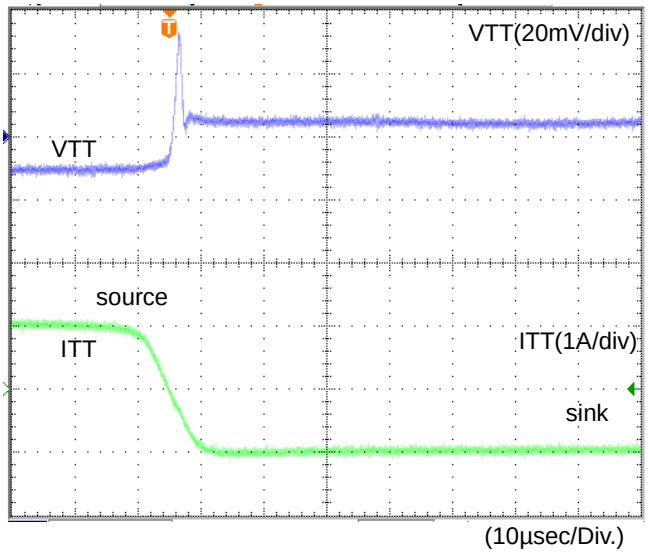

Figure 3. DDR1 (-1A→1A)

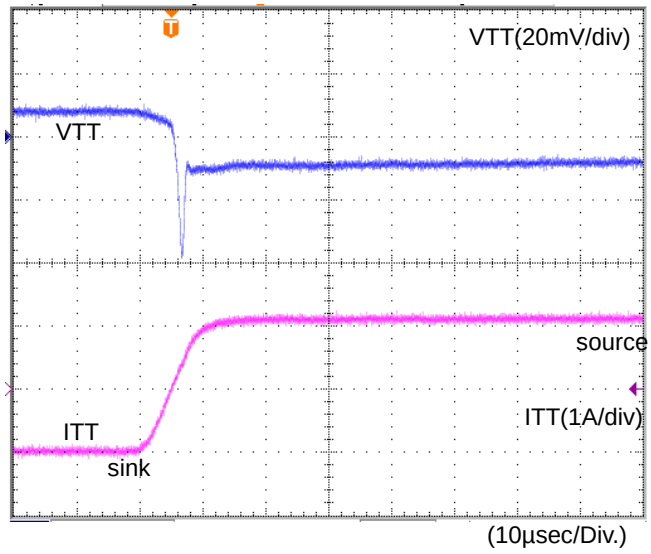

Figure 4. DDR3 (1A→-1A)

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Typical Performance Curves - continued

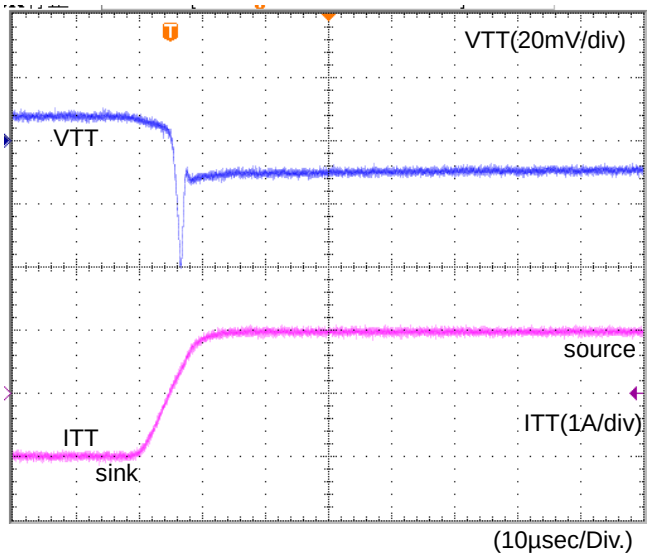

Figure 5. DDR2 (1A→-1A)

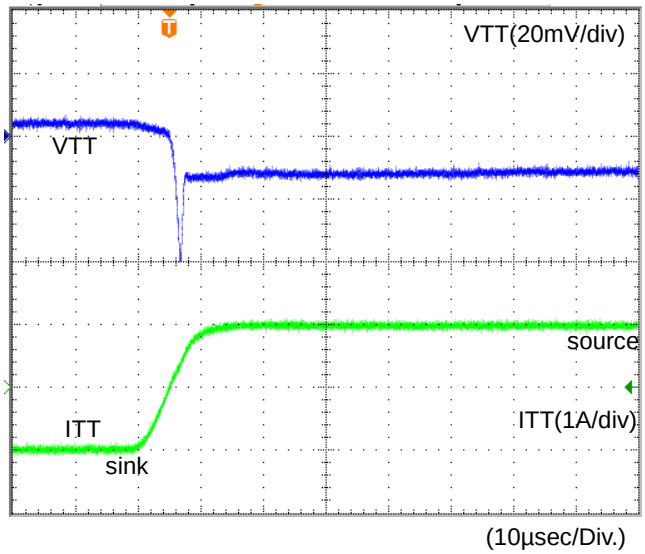

Figure 6. DDR1 (1A→-1A)

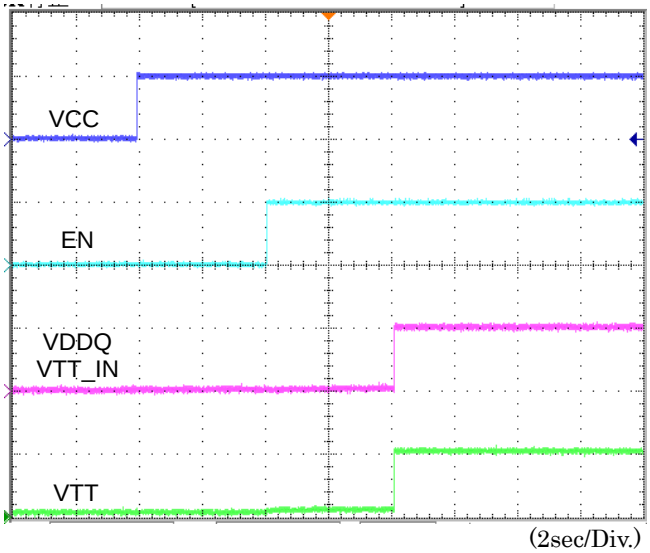

Figure 7. Input sequence1

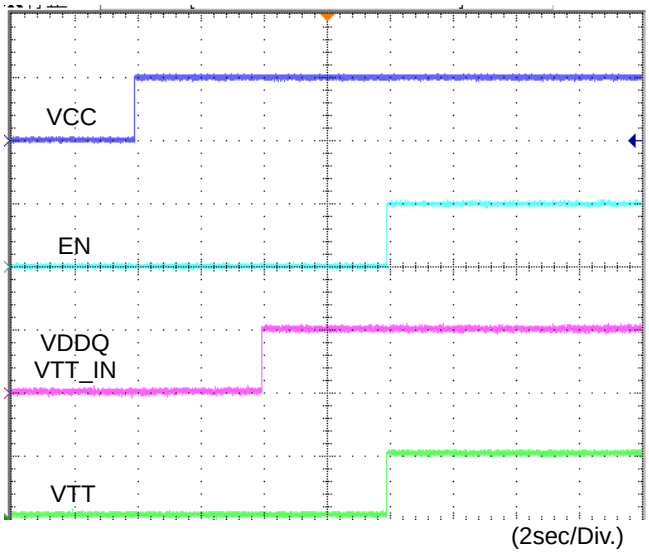

Figure 8. Input sequence2

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Typical Performance Curves - continued

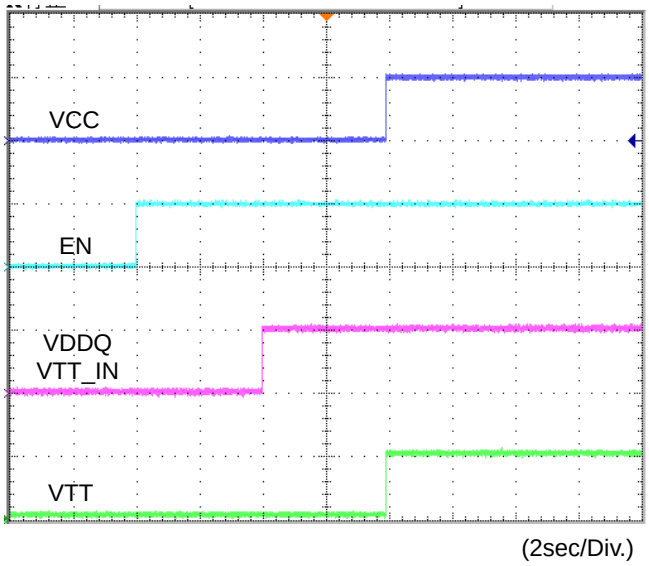

Figure 9. Input sequence3

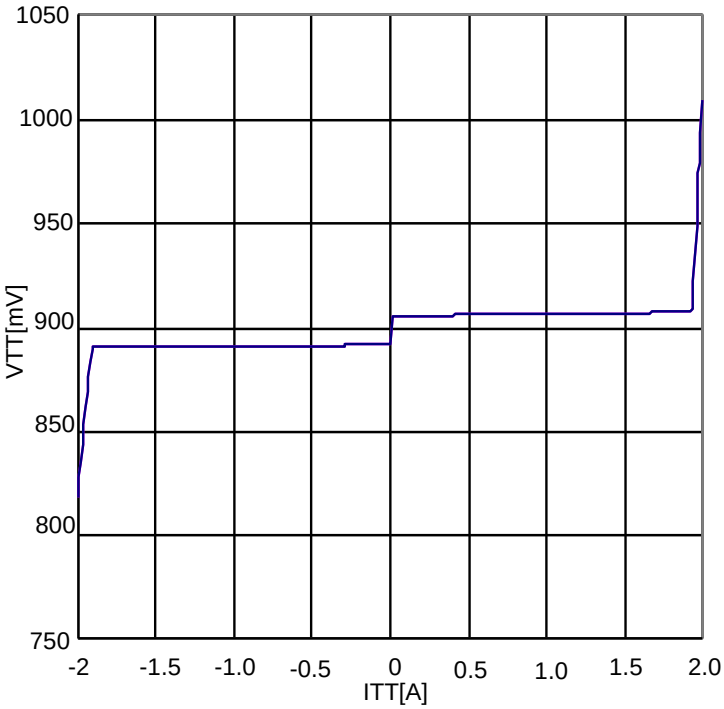

Figure.10 ITT-VTT(DDR2)

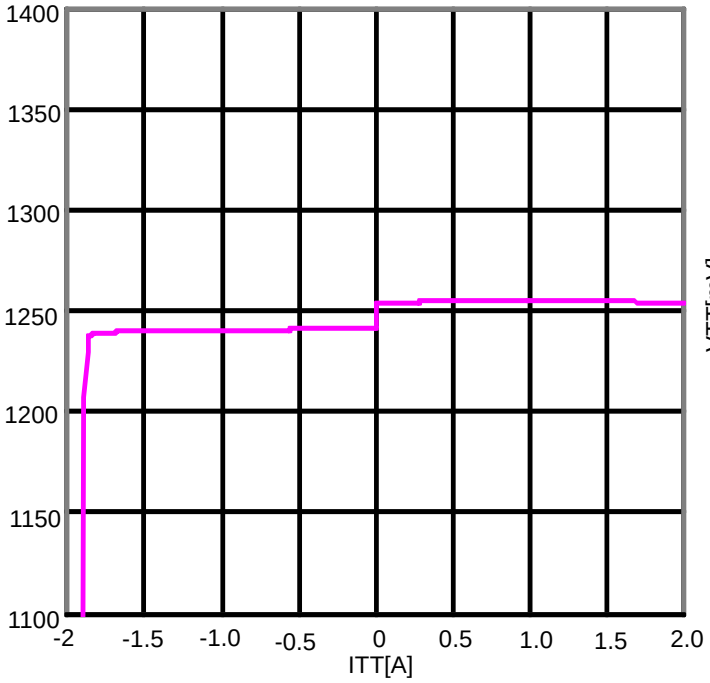

Figure.11 ITT-VTT(DDR1)

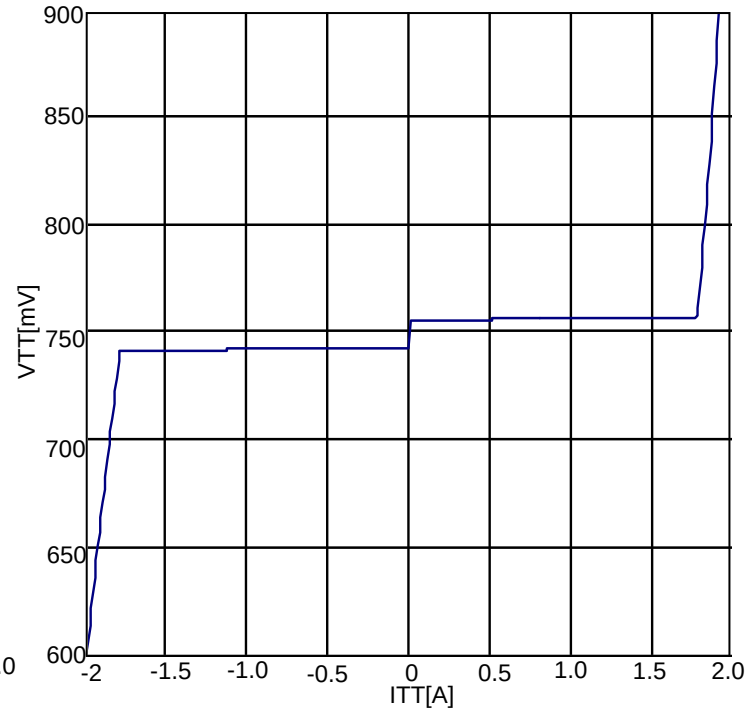

Figure.12 ITT-VTT(DDR3)

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Typical Performance Curves - continued

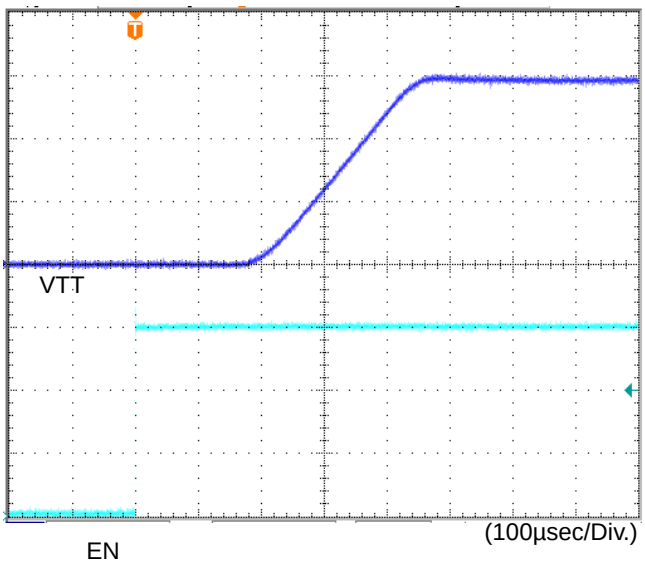

Fig.13 EN soft start
(DDR2)

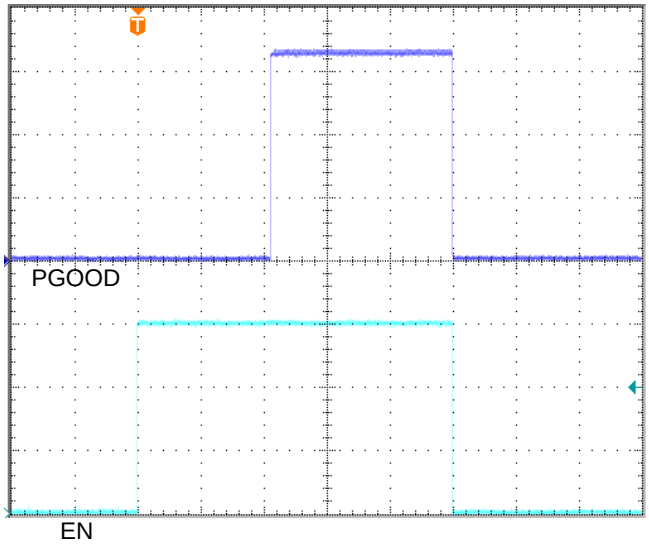

Figure.14 PGOOD Delay
(Start up-Shut down)

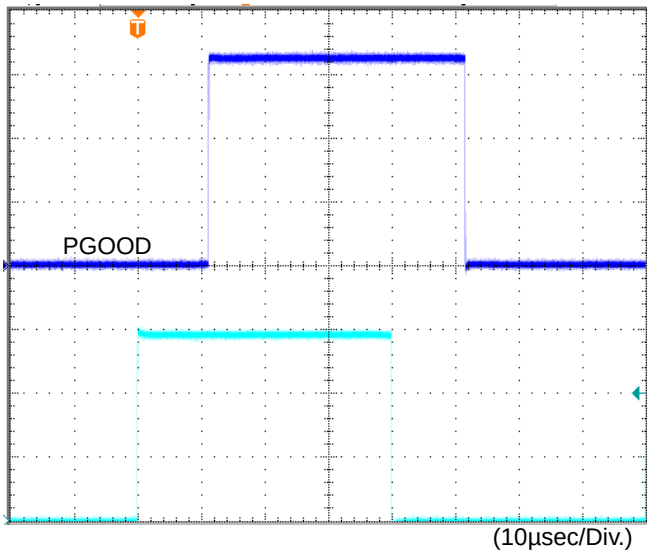

Fig.15 PGOOD Delay
(TSD OFF-TSD ON)

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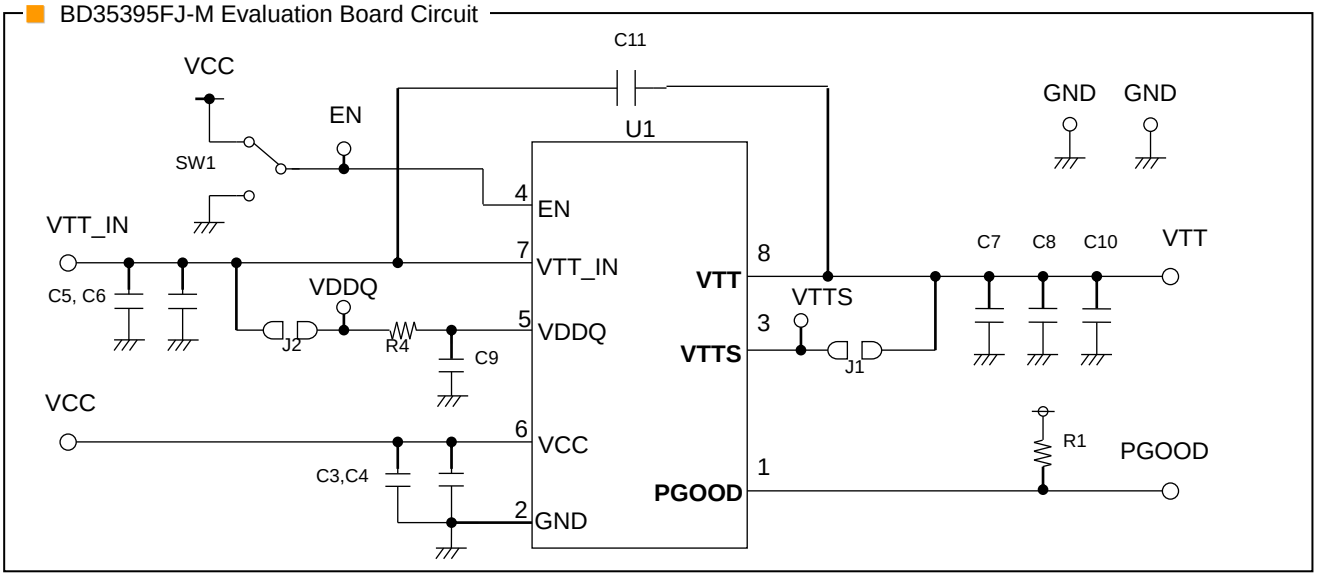
Application Example

■ BD35395FJ-M Evaluation Board Circuit



■ BD35395FJ-M Evaluation Board Application Components

Designation	Value	Company	Part No.
U1	-	ROHM	BD35395FJ-M
R1	10kΩ	ROHM	MCR031002
R4	220Ω	ROHM	MCR032200
J1	0Ω	-	-
J2	0Ω	-	-
C3	1µF	KYOCERA	CM105B105K06A
C4	-	-	-

Designation	Value	Company	Part No.
C5	10µF	KYOCERA	CM21B106M06A
C6	-	-	-
C7	10µF	KYOCERA	CM21B106M06A
C8	-	-	-
C9	2.2µF	KYOCERA	CM105B225K06A
C10	-	-	-
C11	-	-	-

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Power Dissipation

Thermal design must be conducted with the operation under the conditions listed below (which are the guaranteed temperature range requiring consideration on appropriate margins etc);

1: Ambient temperature Ta: 105℃ or lower

2:Chip junction temperature Tj: 150℃ or lower

The chip junction temperature Tj can be considered as follows:

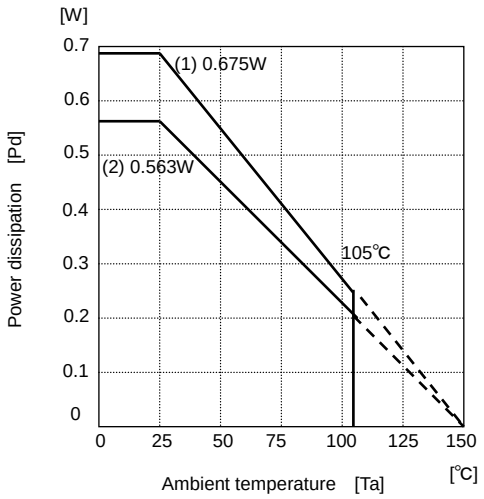
Most of heat loss in BD35395FJ-M occurs at the output N-channel FET. The power lost is determined by multiplying the voltage between VIN and Vo by the output current. As this IC employs the power PKG, the thermal derating characteristics significantly depends on the pc board conditions. When designing, care must be taken to the size of a pc board to be used.

Power consumption (W) = Input voltage (V_{TT_IN})-Output voltage (V_{TT}≒1/2VDDQ) ×Io(Ave)

Example) Where V_{TT_IN} =1.8V, VDDQ=1.8V, Io(Ave)= 0.5A

Power consumption(W) = {1.8(V)-0.9(V)} ×0.5(A)
= 0.45(W)

Heat dissipation characteristics



(1) mounted on 70mm×70mm×1.6mm glass-epoxy board
θj-c=185.2℃/W
(2) With no heat sink
θj-a=222.2℃/W

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.
   OR

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

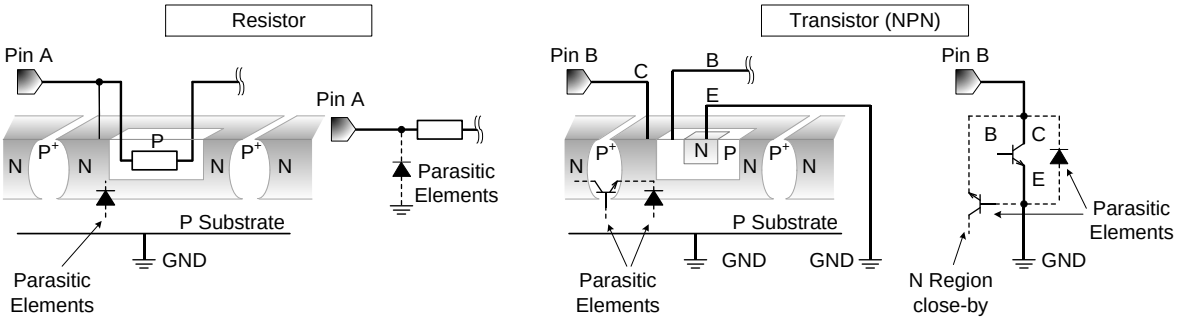

Figure xx. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

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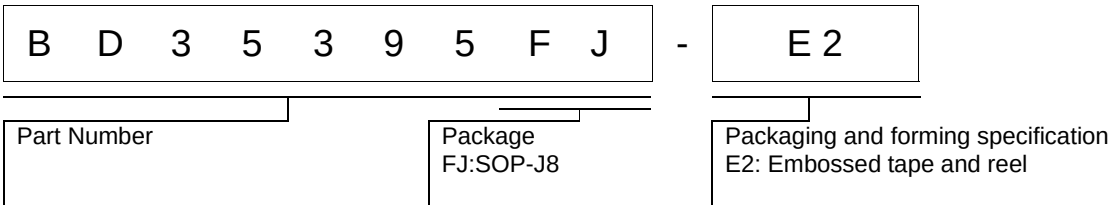
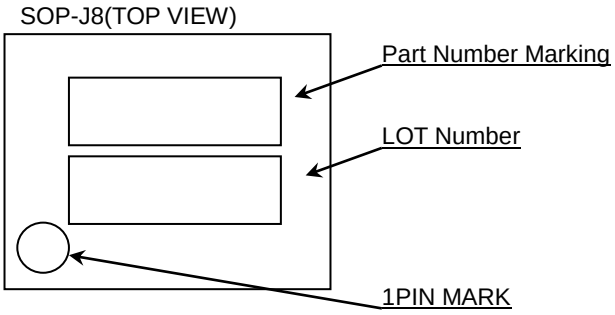
Ordering Information



Marking Diagrams



Part Number Marking	Package	Orderable Part Number
35395	SOP-J8	BD35395FJ-ME2

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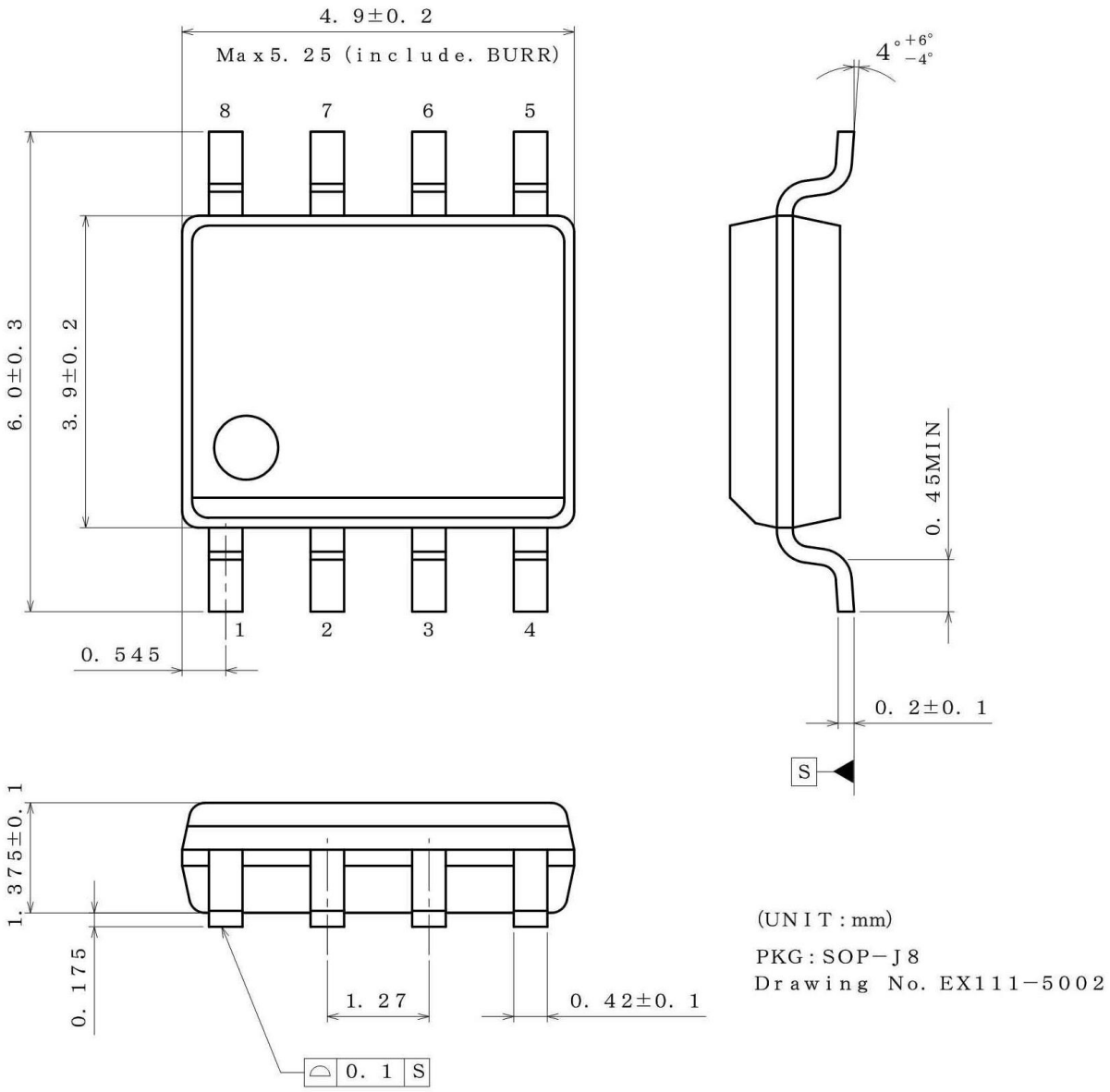
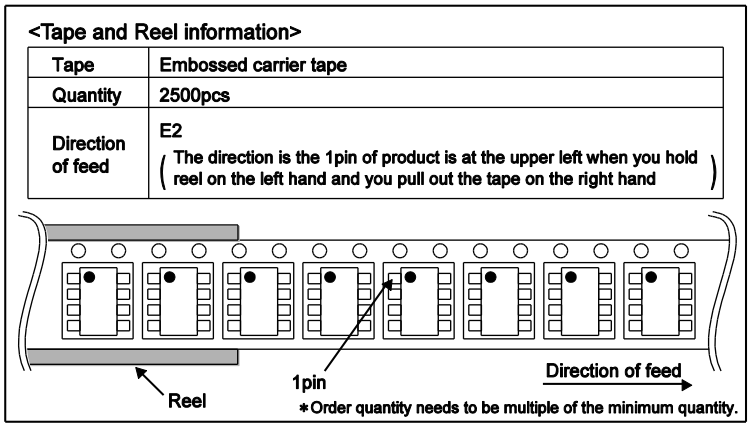
Physical Dimension, Tape and Reel Information

Package Name	SOP-J8





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Revision History

Date	Revision	Changes
26.Feb.2014	001	New Release
5.Jun.2014	002	The specification is added for DDR3L. (P.5)
30.Nov.2017	003	The item of “16. Over Current Protection Circuit (OCP)” in “Operational Notes” is deleted. (P.13)

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Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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