4.5V to 18V Input, 4.0A Integrated MOSFET Single Synchronous Buck DC/DC Converter

BD9C401EFJ

General Description

BD9C401EFJ is a synchronous buck switching regulator with built-in low on-resistance power MOSFETs. With wide input voltage range, It is capable of providing current of up to 4A. It is a current mode control DC/DC converter and features high-speed transient response. Phase compensation can also be set easily.

Key Specifications

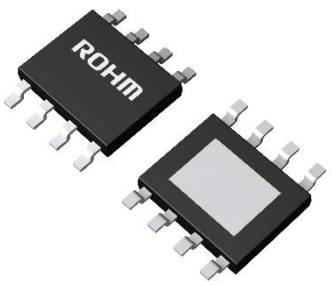
- Input Voltage Range: 4.5V to 18.0V
- Reference Voltage: 0.8V ± 1%
- Maximum Output Current: 4A(Max)
- Switching Frequency: 500kHz(Typ)
- Pch MOSFET On Resistance: 65mΩ(Typ)
- Nch MOSFET On Resistance: 35mΩ(Typ)
- Standby Current: 1μA (Typ)
- Operating Temperature Range: -40°C to +85°C

Features

- Synchronous Single DC/DC Converter
- Over Current Protection
- Thermal Shutdown Protection
- Under Voltage Lockout Protection
- Short Circuit Protection
- Fixed Soft Start Function

Package

	W(Typ) x D(Typ) x H(Max)
HTSOP-J8	4.90mm x 6.00mm x 1.00mm



HTSOP-J8

Applications

- LCD TVs
- Set-top Boxes
- DVD/Blu-ray Disc Players/Recorders
- Broadband Network and Communication Interface
- Entertainment Devices

Typical Application Circuit

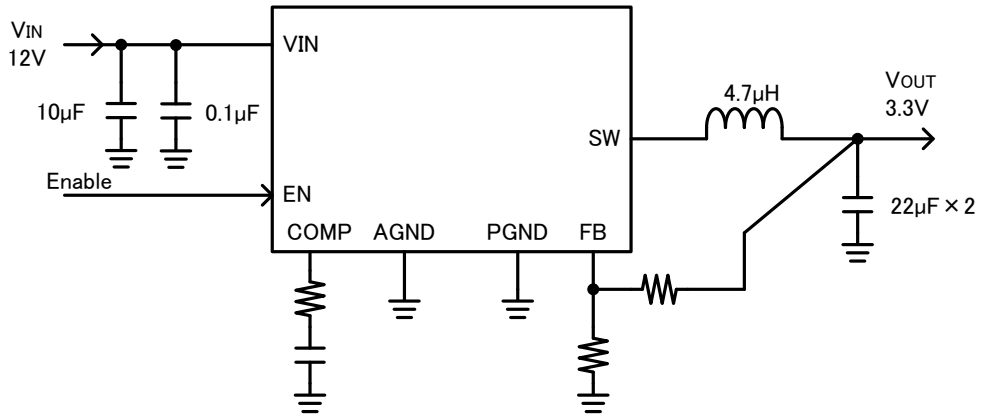


Figure 1. Application Circuit

○Product structure: silicon monolithic integrated circuit ○This product has no protection against radioactive rays

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Pin Configuration

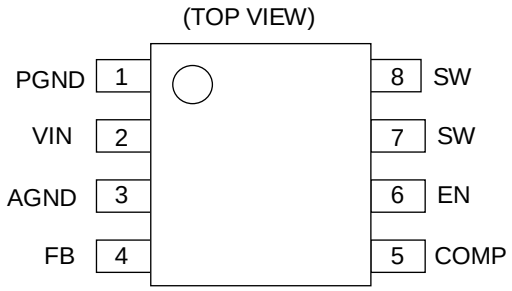

Figure 2. Pin Assignment

Pin Descriptions

Pin No.	Pin Name	Function
1	PGND	Ground pins for the output stage of the switching regulator.
2	VIN	This pins supply power to the control circuit and the output stage of the switching regulator. Connecting a 10 µF and a 0.1µF ceramic capacitor is recommended.
3	AGND	Ground pin for the control circuit.
4	FB	An inverting input node for the gm error amplifier. See page 14 for how to calculate the resistance of the output voltage setting.
5	COMP	An input pin for the switch current comparator and an output pin for the gm error amplifier. Connect a frequency phase compensation component to this pin. See page 14 for how to calculate the resistance and capacitance for phase compensation.
6	EN	Turning this pin signal low (0.8 V or lower) forces the device to enter the shutdown mode. Turning this pin signal high (2.0 V or higher) enables the device. This pin must be terminated.
7	SW	Switch nodes. These pins are connected to the drain of Pch MOSFET and the drain of Nch MOSFET.
8		
-	E-Pad	A backside heat dissipation pad. Connecting to the internal PCB ground plane by using multiple vias provides excellent heat dissipation characteristics.

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Block Diagram

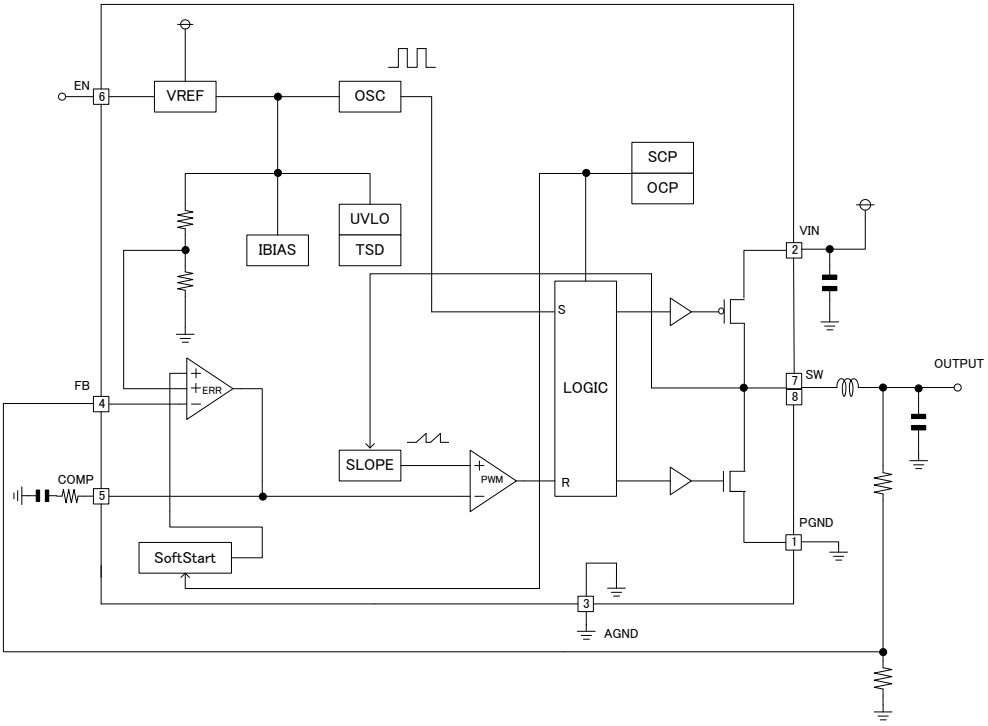

Figure 3. Block Diagram

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit	Conditions
Supply Voltage	V_{IN}	20	V	
SW Pin Voltage	V_{SW}	20	V	
EN Pin Voltage	V_{EN}	20	V	
Power Dissipation (Note 1)	Pd	3.76	W	When mounted on a 70 mm x 70 mm x 1.6 mm 4-layer glass epoxy board
Operating Temperature Range	Topr	-40 to +85	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	
Maximum Junction Temperature	Tjmax	150	°C	
FB, COMP Pin Voltage	V_{LVPINS}	7	V	

(Note1) Derate by 30.08 mW when operating above 25°C.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Range (Ta= -40°C to +85°C)

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Supply Voltage	V_{IN}	4.5	-	18.0	V
Output Current	I_{OUT}	-	-	4.0	A
Output Voltage Setting Range	V_{RANGE}	$V_{IN} \times 0.125$ (Note 1)	-	$V_{IN} \times 0.7$	V

(Note 1) $V_{IN} \times 0.125 \geq 0.8$ [V]

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Electrical Characteristics
(Ta = 25°C, V_{IN} = 12 V, V_{EN} = 5 V unless otherwise specified)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Circuit Current in Active	I_{Q_active}	-	1.5	2.5	mA	V_{FB}= 0.75V, V_{EN}= 5V
Circuit Current in Standby	I_{Q_stby}	-	1.0	10.0	μA	V_{EN} = 0V
FB Pin Voltage	V_{FB}	0.792	0.800	0.808	V	FB-COMP Short (Voltage follower)
FB Input Current	I_{FB}	-	0	2	μA	
Switching Frequency	f_{OSC}	450	500	550	kHz	
High Side FET On Resistance	R_{ONH}	-	65	-	mΩ	V_{IN}= 12V , I_{SW} = -1A
Low Side FET On Resistance	R_{ONL}	-	35	-	mΩ	V_{IN}= 12V , I_{SW} = -1A
Power MOS Leakage Current	I_{LSW}	-	0	5	μA	V_{IN}= 18V , V_{SW} = 18V
Current Limit	I_{LIMIT}	4.5	-	-	A	
Minimum Duty Ratio	Min_duty	-	-	12.5	%	
UVLO Threshold	V_{UVLO}	3.75	4.0	4.25	V	V_{IN} Sweep up
UVLO Hysteresis Voltage	$V_{UVLOHYS}$	-	0.2	-	V	
EN High-Level Input Voltage	V_{ENH}	2.0	-	-	V	
EN Low-Level Input Voltage	V_{ENL}	-	-	0.8	V	
Soft Start Time	T_{SS}	0.5	1.0	2.0	msec	

(Note 1) V_{FB} :FB Pin Voltage, V_{EN} :EN Pin Voltage, I_{SW} :SW Pin Current
(Note 2) Current capability should not exceed Pd.

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Typical Performance Curves

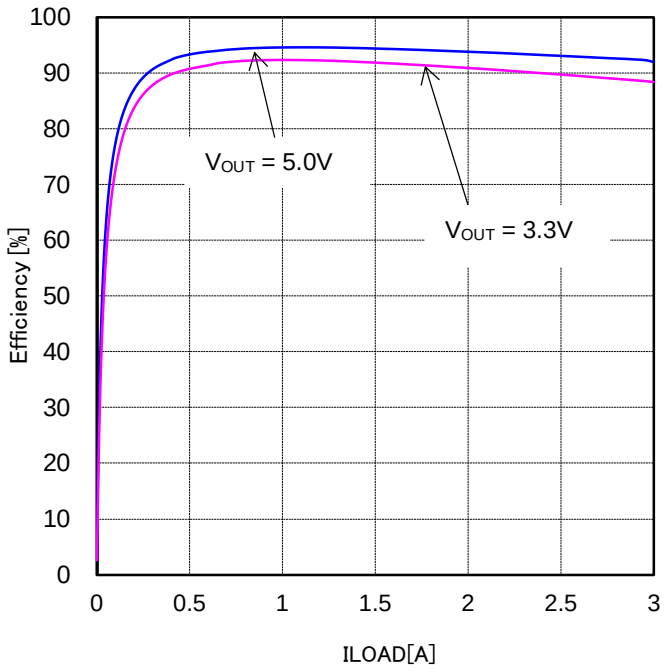


Figure 4. Efficiency
(VIN=12V, L=4.7µH)

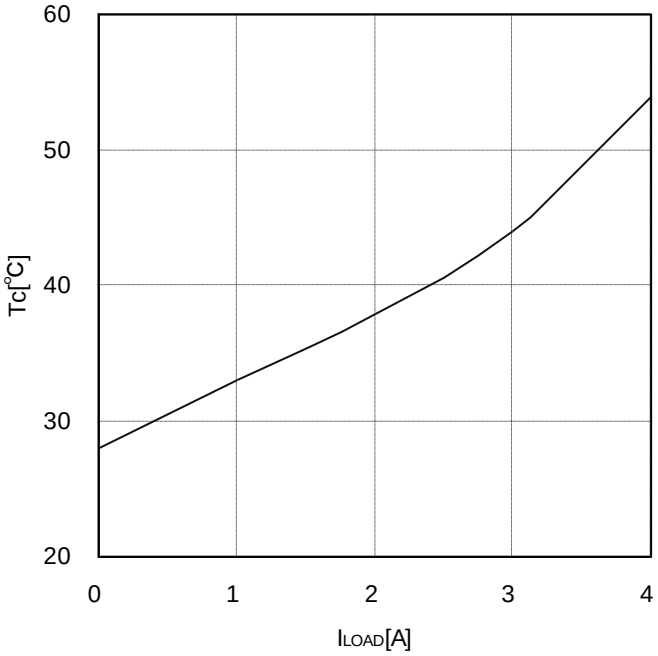
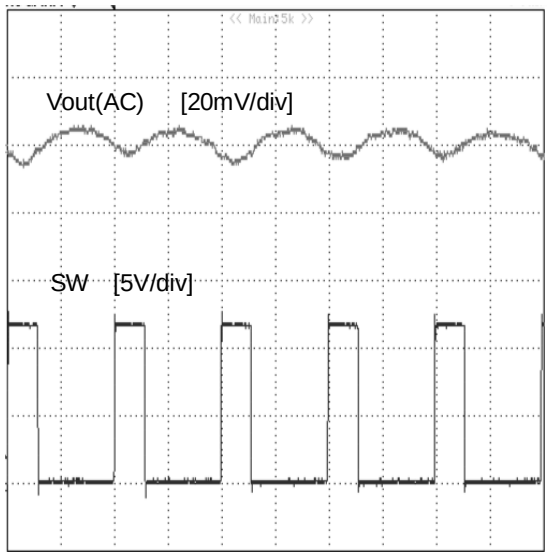
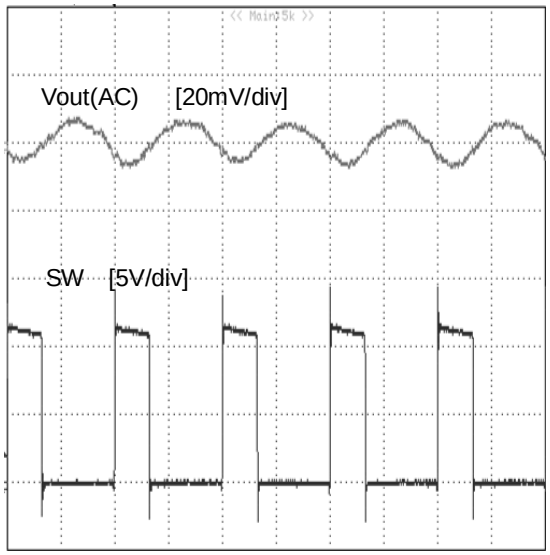


Figure 5. T_C vs I_{LOAD}
(VIN=12V, Vout=3.3V, L=4.7µH, Cout=44µF)



T - Time - 1µsec/div

Figure 6. Vout Ripple
(VIN=12V, Vout=3.3V, L=4.7µH, Cout=44µF, Iout=0A)



T - Time - 1µsec/div

Figure 7. Vout Ripple
(VIN=12V, Vout=3.3V, L=4.7µH, Cout=44µF, Iout=4A)

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Typical Performance Curves (Continued)

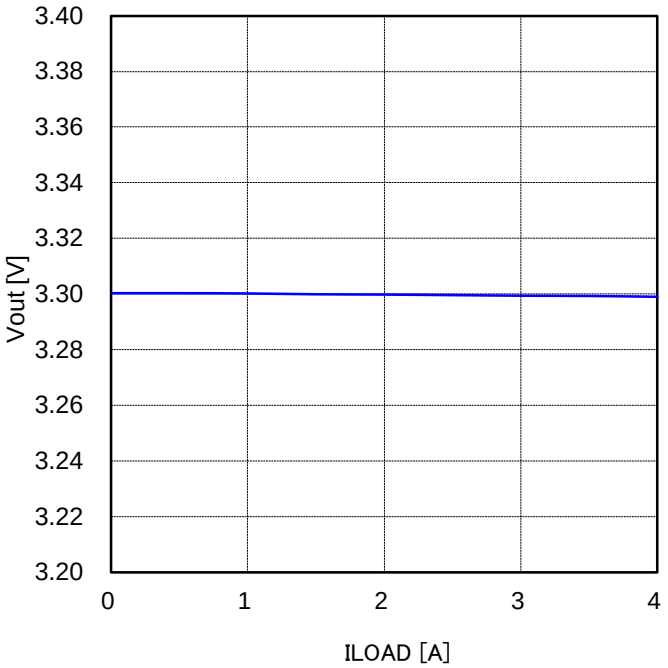

Figure 8. Load Regulation
(VIN=12V, Vout=3.3V, L=4.7µH, Cout=44µF)

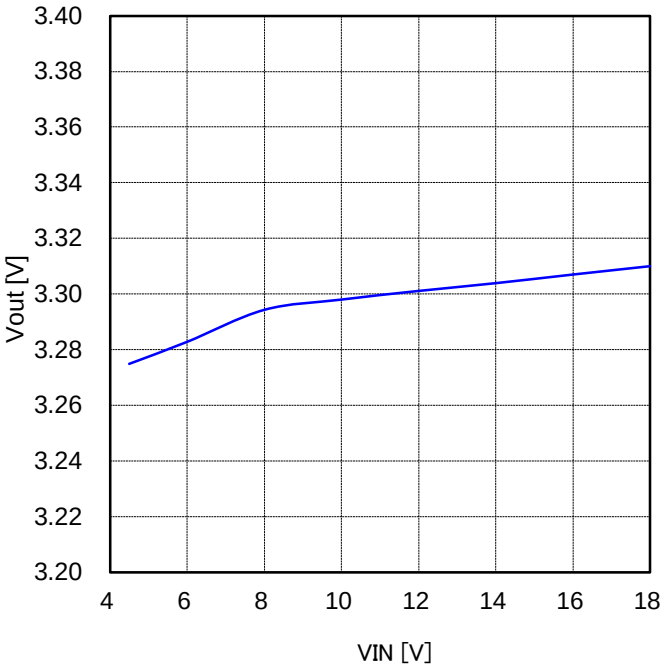

Figure 9. Line Regulation
(Vout=3.3V, L=4.7µH, Cout=44µF, Iout=0A)

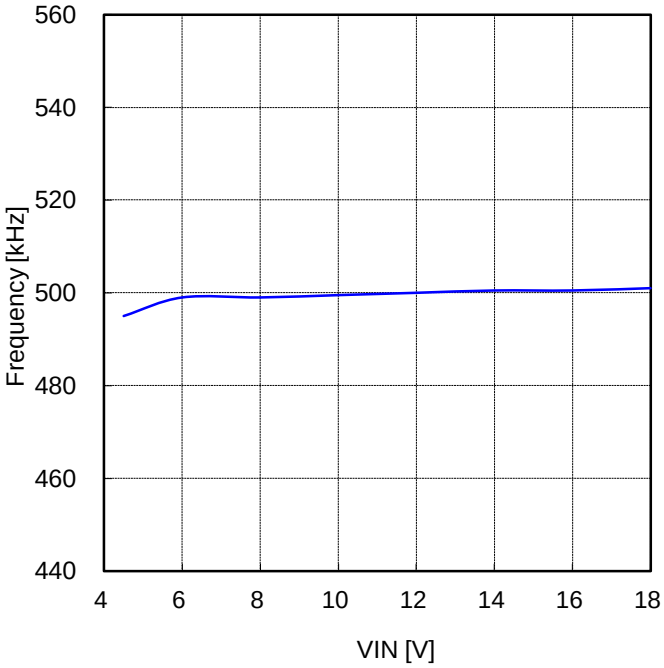

Figure 10. Switching Frequency
(Vout=3.3V, L=4.7µH, Cout=44µF, Iout=0A)

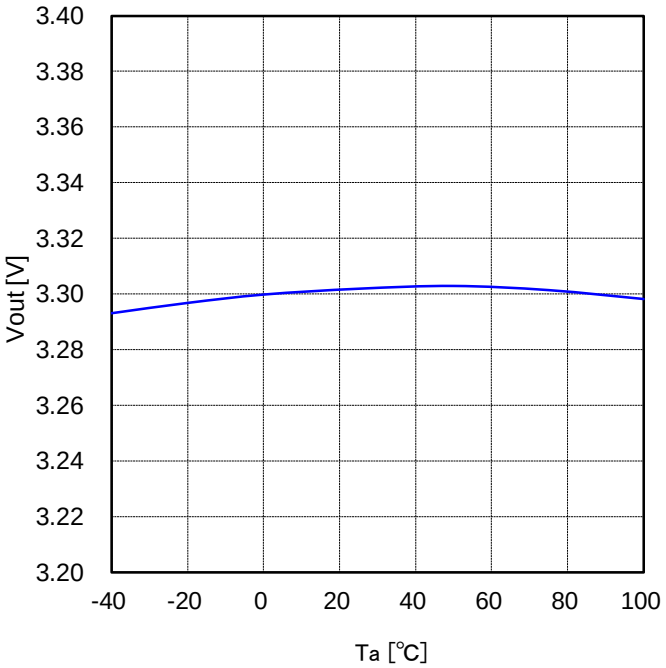

Figure 11. Vout vs Temperature
(Vin=12V, Vout=3.3V, L=4.7µH, Cout=44µF, Iout=0A)

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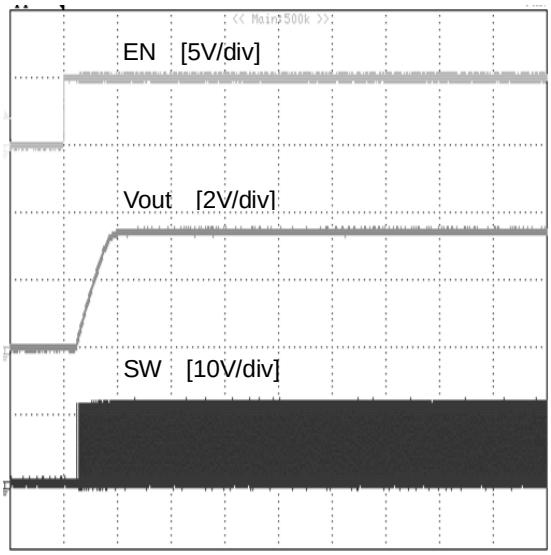
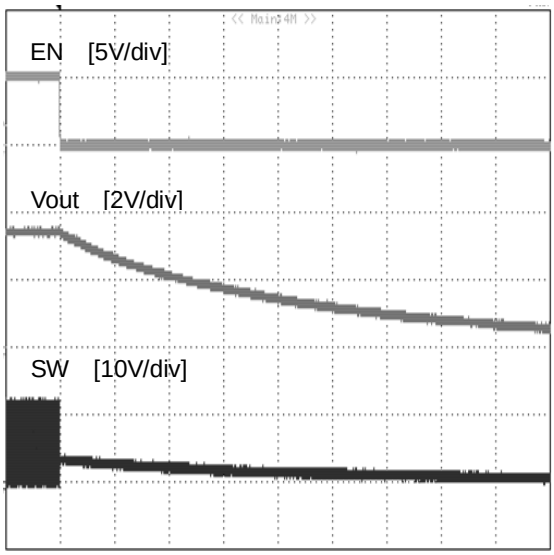
Typical Performance Curves (Continued)



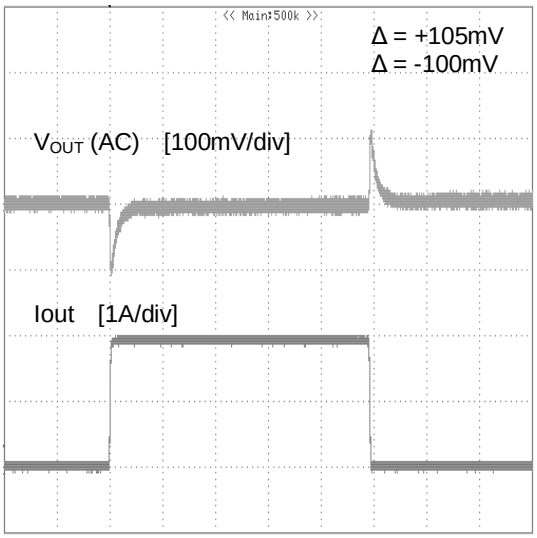
T - Time – 1msec/div

Figure 12. Start-up with EN
(Vin=12V, Vout=3.3V, L=4.7µH, Cout=44µF, Iout=0A)



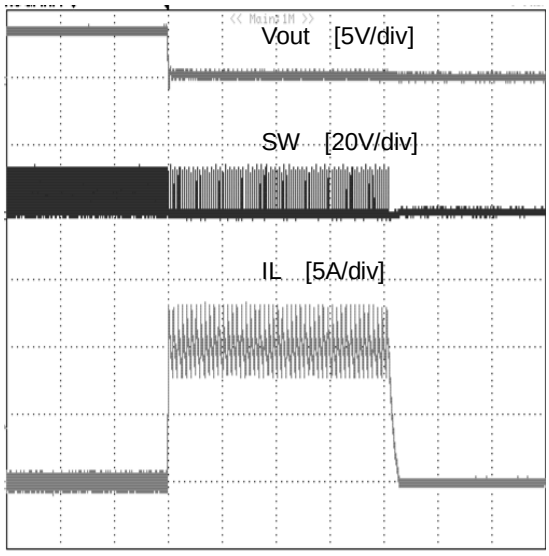
T - Time – 200msec/div

Figure 13. Shutdown Wave Form
(Vin=12V, Vout=3.3V, L=4.7µH, Cout=44µF, Iout=0A)



T - Time – 1msec/div

Figure 14. Transient Response
(Vin=12V, Vout=3.3V, L=4.7µH, Cout=44µF, Iout=2A)



T - Time - 200µsec/div

Figure 15. OCP Function
(Vin=12V, Vout=3.3V, L=4.7µH, Cout=44µF, Vout is short to GND)

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Function Explanations

1. Enable control

The IC shutdown can be controlled by the voltage applied to the EN pin. When VEN reaches 2.0 V, the internal circuit is activated and the IC starts up.

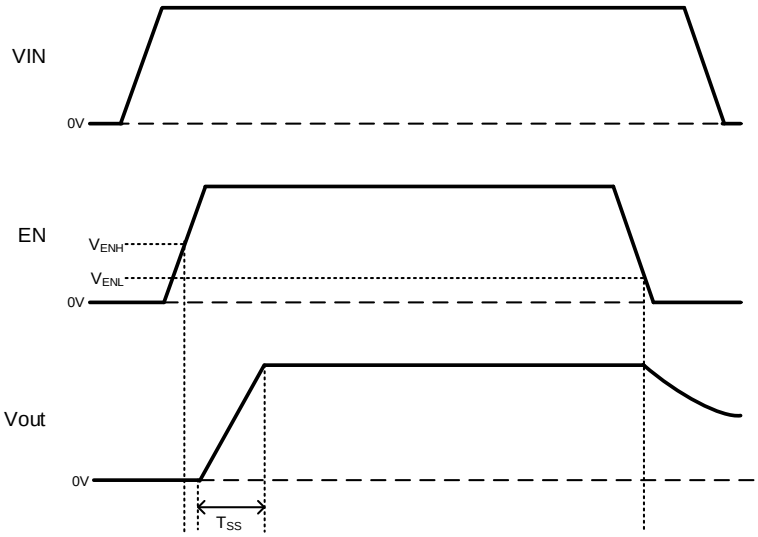

Figure 16. Timing Chart of Enable Control

2. Protective Functions

The protective circuits are intended for prevention of damage caused by unexpected accidents. Do not use them for continuous protective operation.

2-1. Short Circuit Protection Function (SCP)

The short circuit protection block (SCP) compares the FB pin voltage with the internal reference voltage VREF. When the FB pin voltage fall below V_{SCP} (= VREF – 240mV) and with that situation continuing for off latch time, it latches output in off situation.

Table 1. Short Circuit Protection Function

EN Pin	FB Pin	Short Circuit Protection Function	Short Circuit Protection Operation
2.0 V or higher	< V_{SCP}	Enabled	ON
	> V_{SCP}		OFF
0.8 V or lower	-	Disabled	OFF

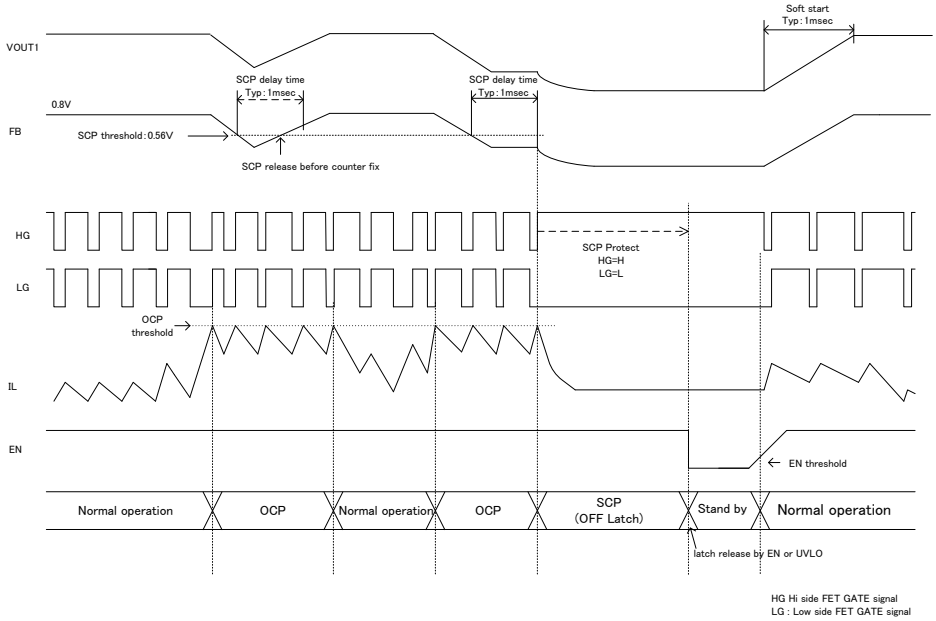

Figure 17. Short Circuit Protection function (SCP) timing chart

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2-2. Under Voltage Lockout Protection (UVLO)

The Under Voltage Lockout Protection (UVLO) circuit monitors the VIN pin voltage.
The device stops the switching operation and the output voltage drops when the VIN pin voltage is 3.8V (Typ) in the case of VIN sweep down. The device starts the switching operation and the output voltage gradually rises when the VIN pin voltage is 4.0V (Typ) in the case of VIN sweep up.

In the case of the application that EN pin is shortened to VIN pin like Figure 18-a, please use the UVLO function on the below conditions.

- VIN Sweep Down: Set the falling slew rate of VIN to 0.9V/ms or more and drop the VIN voltage to 0V.
- VIN Sweep Up: Set the rising slew rate of VIN to 1.8V/ms or more and start the VIN voltage from 0V.

If the slew rate is slower than the above values, UVLO circuit is not able to operate normally and the output of UVLO block may become indefinite at the lower VIN voltage than UVLO release or detect voltage. The Vout voltage may be re-outputted in the case of the indefinite UVLO output.

If the VIN pin voltage has the rising slew rate of less than 1.8V/ms or the falling slew rate of less than 0.9V/ms, the start-up and shutdown must be controlled by EN function instead of UVLO function as shown Figure 18-b.

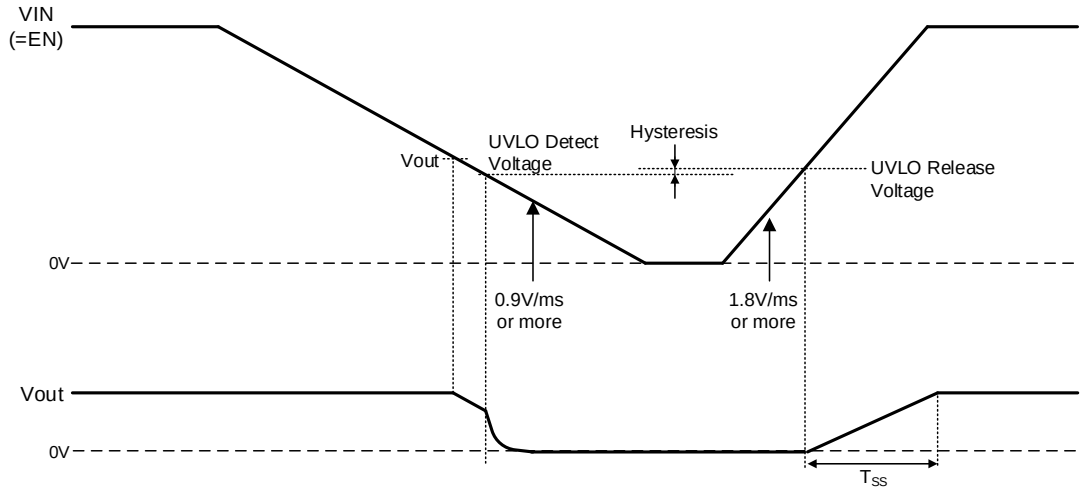

Figure 18-a. UVLO Timing Chart (VIN=EN)

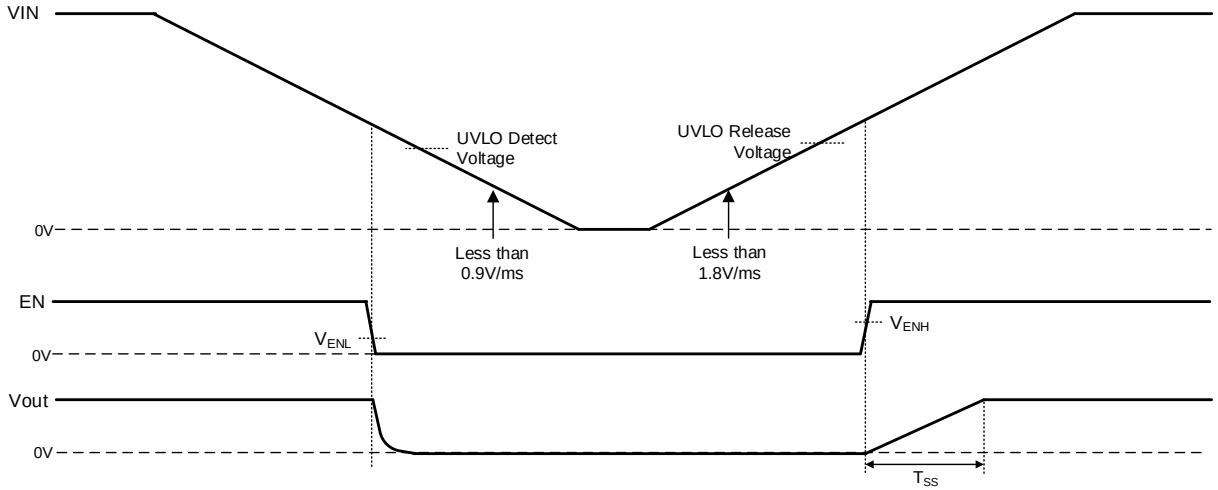

Figure 18-b. EN Control Timing Chart in the case of slow VIN slew rate

<u>If there is any questions about above EN control or considerations of other control method, please contact us.</u>

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2-3. Thermal Shutdown

When the chip temperature exceeds Tj = 175°C (Typ), the DC/DC converter output is stopped. The thermal shutdown circuit is intended for shutting down the IC from thermal runaway in an abnormal state with the temperature exceeding Tjmax = 150°C (Typ). It is not meant to protect or guarantee the soundness of the application. Do not use the function of this circuit for application protection design.

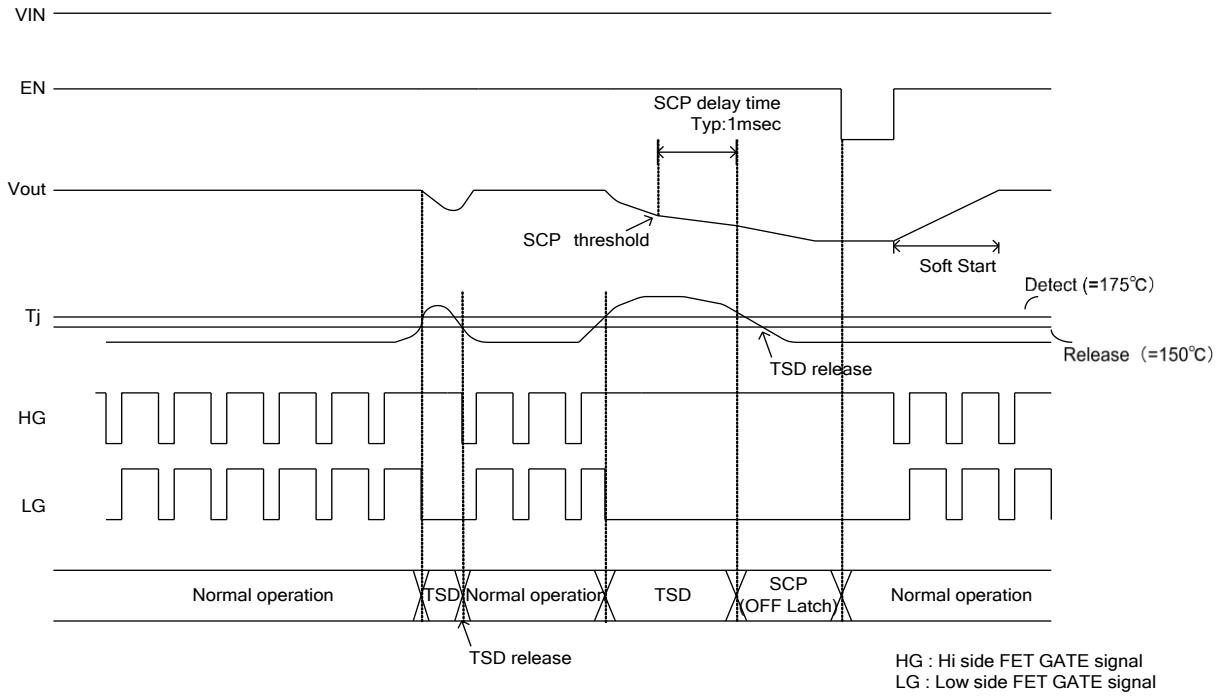

Figure 19. TSD Timing chart

2-4. Over Current Protection

The Over Current Protection operates by using the current mode control to limit the current that flows through the top MOSFET at each cycle of the switching frequency. When an abnormal state continues, the output is fixed in a low level.

2-5. Error detection (off latch) release method

BD9C401EFJ enters the state of off latch when the protection function operates. To release the off latch state, the VIN pin voltage should be changed to less than UVLO level (=3.8V [Typ]) or, the EN pin voltage falls below V_{ENL}.voltage.

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Application Example

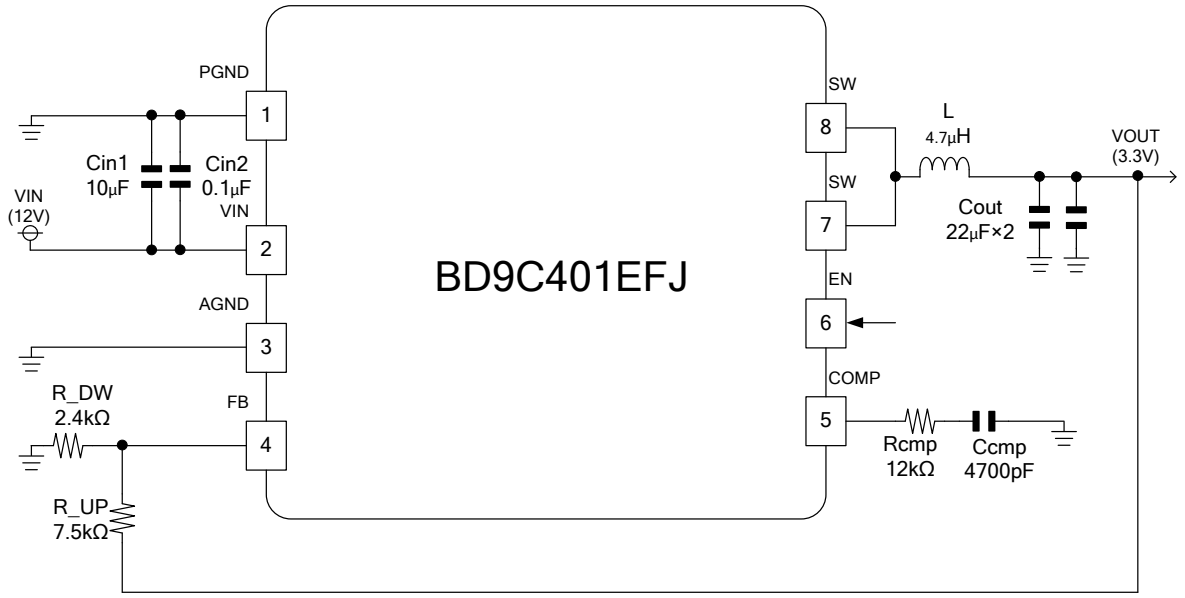

Figure 20. Application Circuit
(V_{IN}=12V, V_{OUT}=3.3V)

*Please confirm the above components values and the characteristics on the application board because there is a case needed to adjust the values due to the application load.

*If it is considered to use the other application circuit or the other components values, please contact us.

		Maker	**Part No**
Input capacitor(Cin1)	10μF/25V	TDK	C3225JB1E106K
Input capacitor(Cin2)	0.1μF/25V	TDK	C1608JB1H104K
Output capacitor(Cout)	22μF/16V x 2	TDK	C3216JB1C226M x 2
Inductor (L)	4.7μH	TDK	SPM6530-4R7

The example of output voltage setting at V_{IN}=12V

	FB	
Vo(V)	R_UP [kΩ]	R_DW [kΩ]
5	4.3	0.82
3.3	7.5	2.4
1.8	15	12
1.5	16	18
1.2(Note1)	10	20
1(Note1)	5.1	20

(Note 1) V_{OUT} has restriction with V_{IN}. See page 14.

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PCB Layout Design

In the step-down DC/DC converter, a large pulse current flows into two loops. The first loop is the one into which the current flows when the top FET is turned ON. The flow starts from the input capacitor C_{IN}, runs through the FET, inductor L and output capacitor C_{OUT} and back to GND of C_{IN} via GND of C_{OUT}. The second loop is the one into which the current flows when the bottom FET is turned on. The flow starts from the bottom FET, runs through the inductor L and output capacitor C_{OUT} and back to GND of the bottom FET via GND of C_{OUT}. Route these two loops as thick and as short as possible to allow noise to be reduced for improved efficiency. It is recommended to connect the input and output capacitors directly to the GND plane. The PCB layout has a great influence on the DC/DC converter in terms of all of the heat generation, noise and efficiency characteristics.

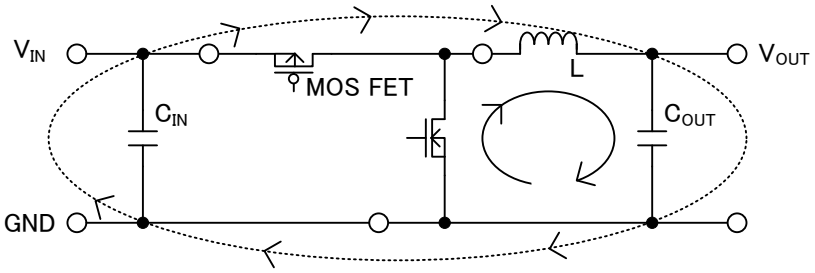
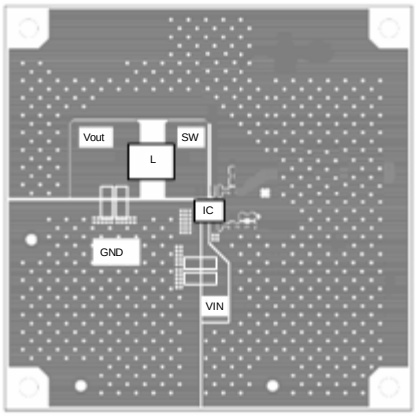


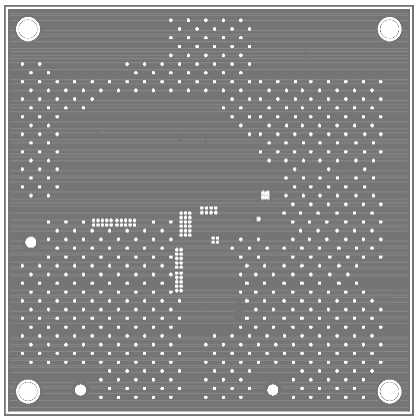
Figure 21. Current Loop of Buck Converter

Accordingly, design the PCB layout considering the following points.

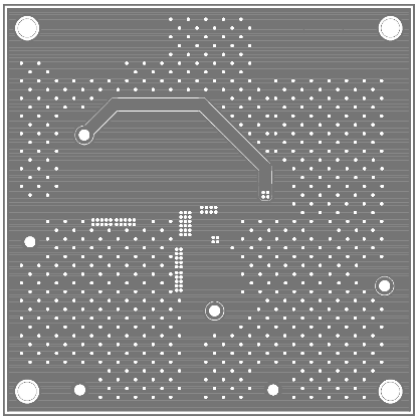
- Connect an input capacitor as close as possible to the IC VIN pin on the same plane as the IC.
- If there is any unused area on the PCB, provide a copper foil plane for the GND node to assist heat dissipation from the IC and the surrounding components.
- Switching nodes such as SW are susceptible to noise due to AC coupling with other nodes. Route the coil pattern as thick and as short as possible.
- Provide lines connected to FB and COMP far from the SW nodes.
- Place the output capacitor away from the input capacitor in order to avoid the effect of harmonic noise from the input.



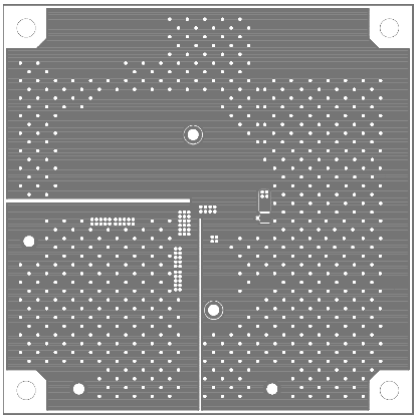
Top layer



Mid layer1



Mid layer2



Bottom layer

Figure 22. Example of evaluation board layout

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Selection of Components Externally Connected

1. Output LC Filter Constant

The DC/DC converter requires an LC filter for smoothing the output voltage in order to supply a continuous current to the load. Selecting an inductor with a large inductance causes the ripple current ΔI_L that flows into the inductor to be small. However, decreasing the ripple voltage generated in the output is not advantageous in terms of the load transient response characteristic. An inductor with a small inductance improves the transient response characteristic but causes the inductor ripple current to be large which increases the ripple voltage in the output voltage, showing a trade-off relationship. It is recommended to select an inductance such that the size of the ripple current component of the coil will be 20% to 40% of the average output current (average inductor current).

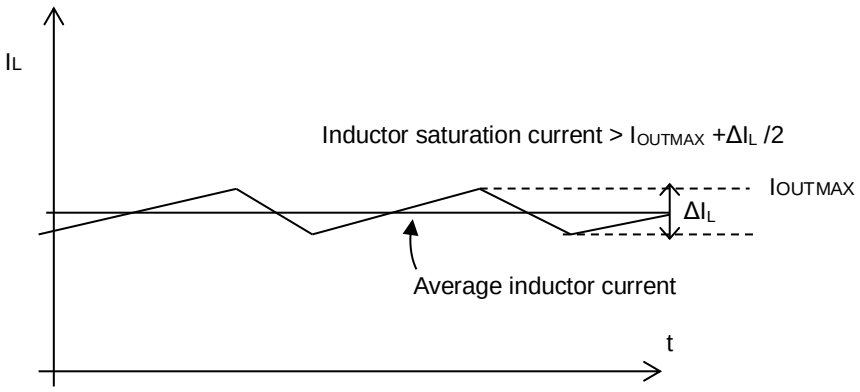

Figure 23. Waveform of current through inductor

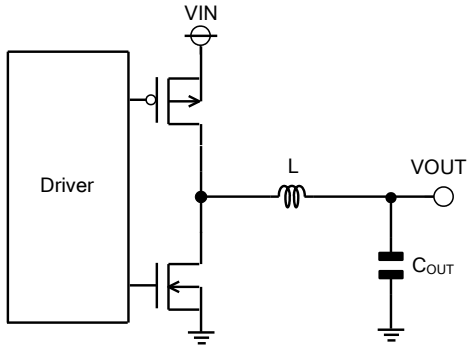

Figure 24. Output LC filter circuit

With VIN = 12 V, VOUT = 3.3 V and the switching frequency F_{OSC} = 500 kHz, the calculation is shown in the following equation.
Coil ripple current ΔIL = 30% x Average output current (4A) = 1.2 [A]

$$L = V_{OUT} \times (V_{IN} - V_{OUT}) \times \frac{1}{V_{IN} \times F_{OSC} \times \Delta I_L} = 3.99\mu \fallingdotseq 4.7\mu \quad \text{[H]}$$

where :

F_{OSC} is a switching frequency

The saturation current of the inductor must be larger than the sum of the maximum output current and 1/2 of the inductor ripple current ΔI_L.

The output capacitor C_{OUT} affects the output ripple voltage characteristics. The output capacitor C_{OUT} must satisfy the required ripple voltage characteristics.

The output ripple voltage can be represented by the following equation.

$$\Delta V_{RPL} = \Delta I_L \times (R_{ESR} + \frac{1}{8 \times C_{OUT} \times F_{OSC}}) \quad \text{[V]}$$

where :

R_{ESR} is the Equivalent Series Resistance (ESR) of the output capacitor.

Also this IC provides 1msec[Typ] soft start function to reduce sudden current which flows in output capacitor when startup. But when capacity value of output capacitor C_{OUT} becomes bigger than the following method, correct soft start waveform may not appear in some cases. (ex. Vout over shoot at soft start .)
Select output capacitor C_{OUT} fulfilling the following condition including scattering and margin..

$$C_{OUT} < \frac{I_{OCP}(= 4.5A[min]) \times T_{SS}(= 0.5ms[min])}{V_{OUT}} \quad \text{[F]}$$

where :

I_{OCP} is switch current restricted value

T_{SS} is soft start time

<u>Caution) Concerning C_{OUT} total the capacity value of every part connected to Output line.</u>

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2. Output Voltage Setting

The output voltage value can be set by the feedback resistance ratio.

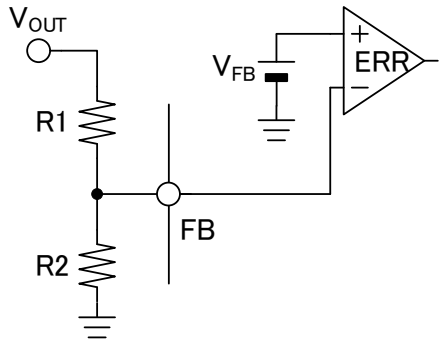

Figure 25. Feedback Resistors Circuit

$$V_{OUT} = \frac{R_1+R_2}{R_2} \times V_{FB} \qquad [V]$$

V_{FB} is 0.8V (Typ) at V_{IN}=12V. The output voltage can be calculated as below formula.

$$V_{OUT} = \frac{R_1+R_2}{R_2} \times 0.800 \qquad [V]$$

Output voltage V_{OUT} and V_{FB} have the V_{IN} dependence as shown in Figure 9 V_{OUT} Line Regulation.
For example, the output voltage at V_{IN}=5V can be set as below.

$$V_{OUT} = \frac{R_1+R_2}{R_2} \times 0.793 \qquad [V]$$

If it is considered to use on the other input voltage, please refer to Figure 9 and set the output voltage value by considering the V_{IN} dependence. Please contact us if needed.

V_{OUT} has restriction with V_{IN} by the following equation.

V_{OUTMIN}: V_{IN} x 0.125
(V_{IN} x 0.125 ≥ 0.8V)
V_{OUTMAX}: V_{IN} x 0.7

3. Phase Compensation Component

A current mode control buck DC/DC converter is a two-pole, one-zero system. Two poles are formed by an error amplifier and load and the one zero point is added by phase compensation. The phase compensation resistor R_{CMP} determines the crossover frequency F_{CRS} where the total loop gain of the DC/DC converter is 0 dB. A high value crossover frequency F_{CRS} provides a good load transient response characteristic but inferior stability. Conversely, a low value crossover frequency F_{CRS} greatly stabilizes the characteristics but the load transient response characteristic is impaired. Here, select the constant so that the crossover frequency F_{CRS} will be 1/20 of the switching frequency.

(1) Selection of Phase Compensation Resistor R_{CMP}

The Phase Compensation Resistance R_{CMP} can be determined by using the following equation.

$$R_{CMP} = \frac{2\pi \times V_{OUT} \times F_{CRS} \times C_{OUT}}{V_{FB} \times G_{MP} \times G_{MA}} \qquad [\Omega] \qquad (3\text{-}1)$$

V_{OUT} is Output Voltage
F_{CRS} is Crossover Frequency
C_{OUT} is Output Capacitance
V_{FB} is Feedback Reference Voltage (0.8 V (Typ))
G_{MP} is Current Sense Gain (7.8 A/V (Typ))
G_{MA} is Error Amplifier Transconductance (300 µA/V (Typ))

(2) Selection of Phase Compensation Capacitance C_{CMP}

The phase compensation capacitance C_{CMP} can be determined by using the following equation.

$$C_{CMP} = \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R_{CMP}} \qquad [F] \qquad (3\text{-}2)$$

*When capacity value of C_{CMP} and resistance value of R_{CMP} don't meet the following method, correct soft start waveform may not appear in some cases.
Select C_{CMP} and R_{CMP} fulfilling the following condition including scattering and margin so that V_{CMP} voltage reaches 1.4V or over within Off-latch delay time of SCP detection (500µsec(MIN)).

$$V_{CMP} = R_{CMP} \times I_{CMP} + \frac{I_{CMP} \times T}{C_{CMP}} \geq 1.4 \qquad [V] \qquad (3\text{-}3)$$

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$$\frac{I_{CMP} \times T}{C_{CMP}} \geq 0.715 \quad [V] \qquad (3\text{-}4)$$

V_{CMP} is COMP Terminal voltage
R_{CMP} is resistor connected to COMP Terminal
C_{CMP} is capacitor connected to COMP Terminal
I_{CMP} is Error Amplifier Source Current (45uA(MIN))
T is SCP delay time(500µsec(MIN))

(3) Loop Stability
To ensure the stability of the DC/DC converter, make sure that a sufficient phase margin is provided. A phase margin of at least 45º in the worst conditions is recommended.

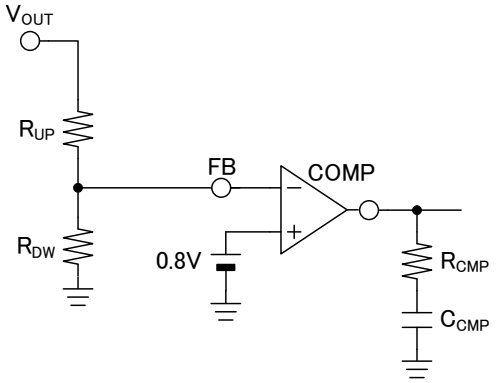

Figure 26. Phase Compensation Circuit

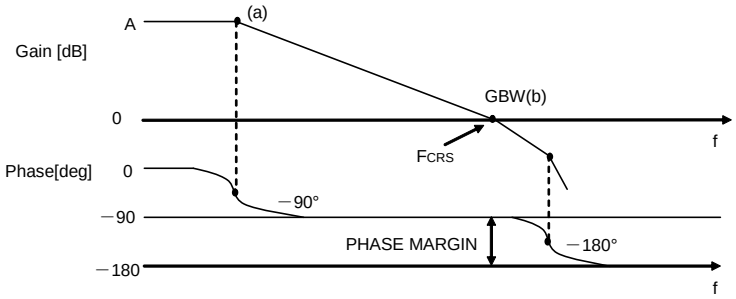

Figure 27. Bode Plot

I/O Equivalent Circuit Diagram

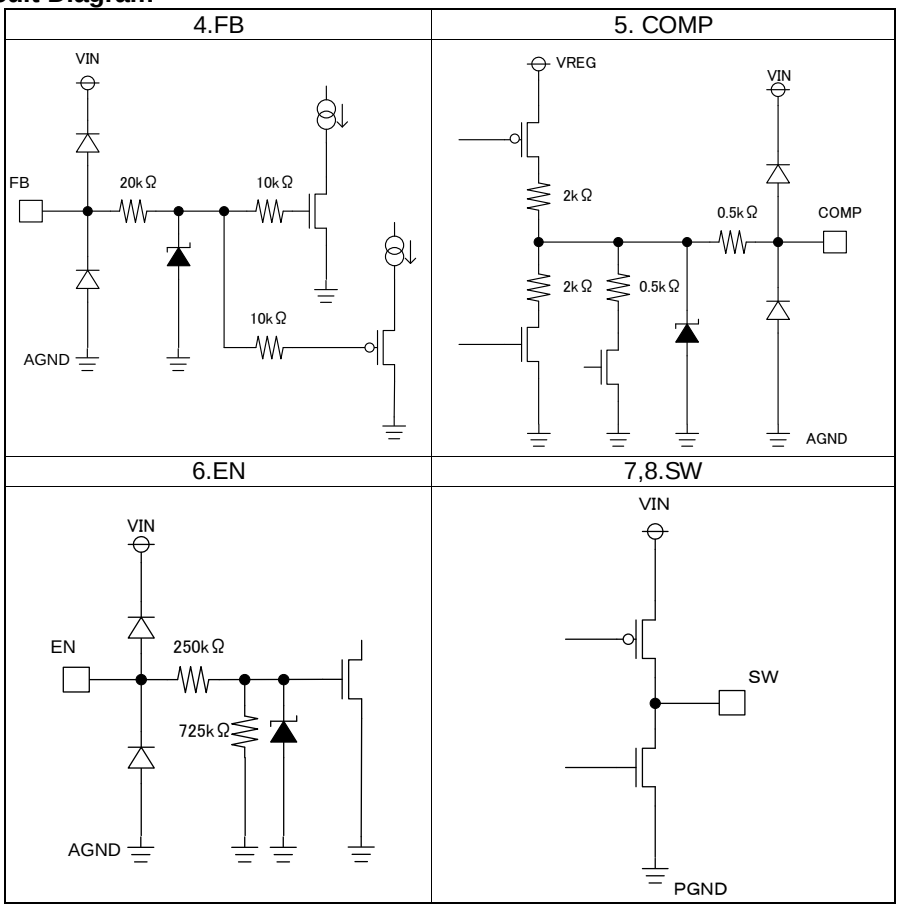

Figure 28.

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm 4-layer glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

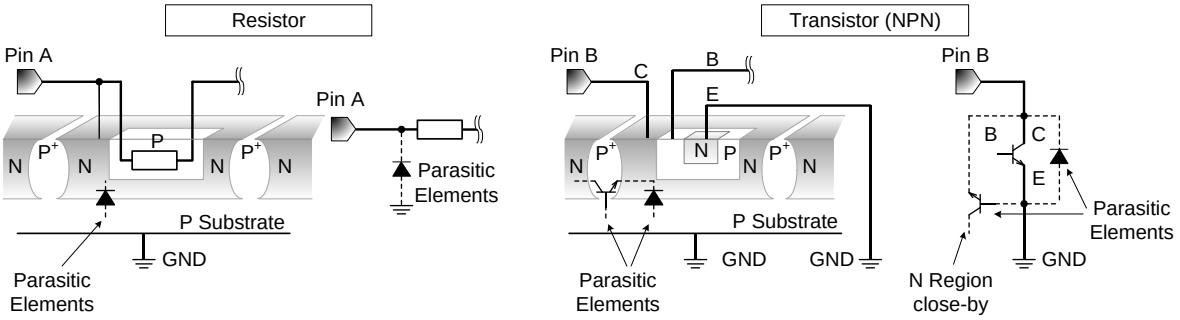

Figure 29. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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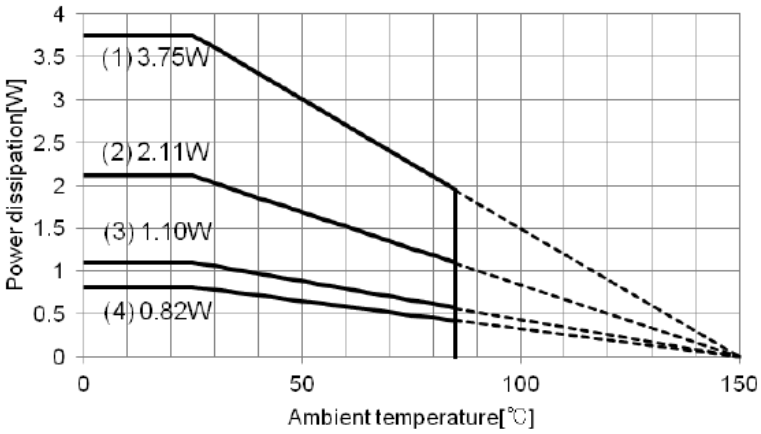
Power Dissipation



HTSOP-J8 Package

Board size: 70mm x 70mm x 1.6mm

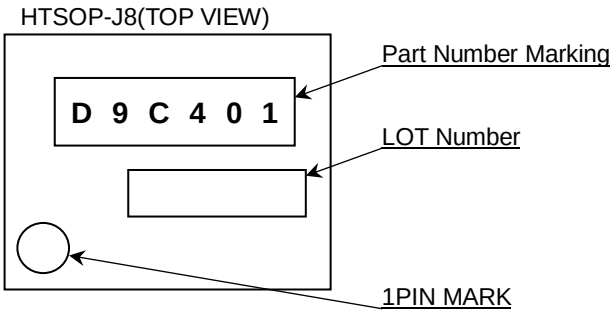
(1) 4-layer board (surface heat dissipation copper foil 70mm × 70mm)
(2) 2-layer board (surface heat dissipation copper foil 70mm × 70mm)
(3) 2-layer board (surface heat dissipation copper foil 15mm × 15mm)
(4) 1-layer board (surface heat dissipation copper foil 0mm × 0mm)

Ordering Information

B D 9 C 4 0 1 E F J - E 2

- Part Number
- Package: EFJ: HTSOP-J8
- Packaging and forming specification: E2: Embossed tape and reel

Marking Diagram (TOP VIEW)



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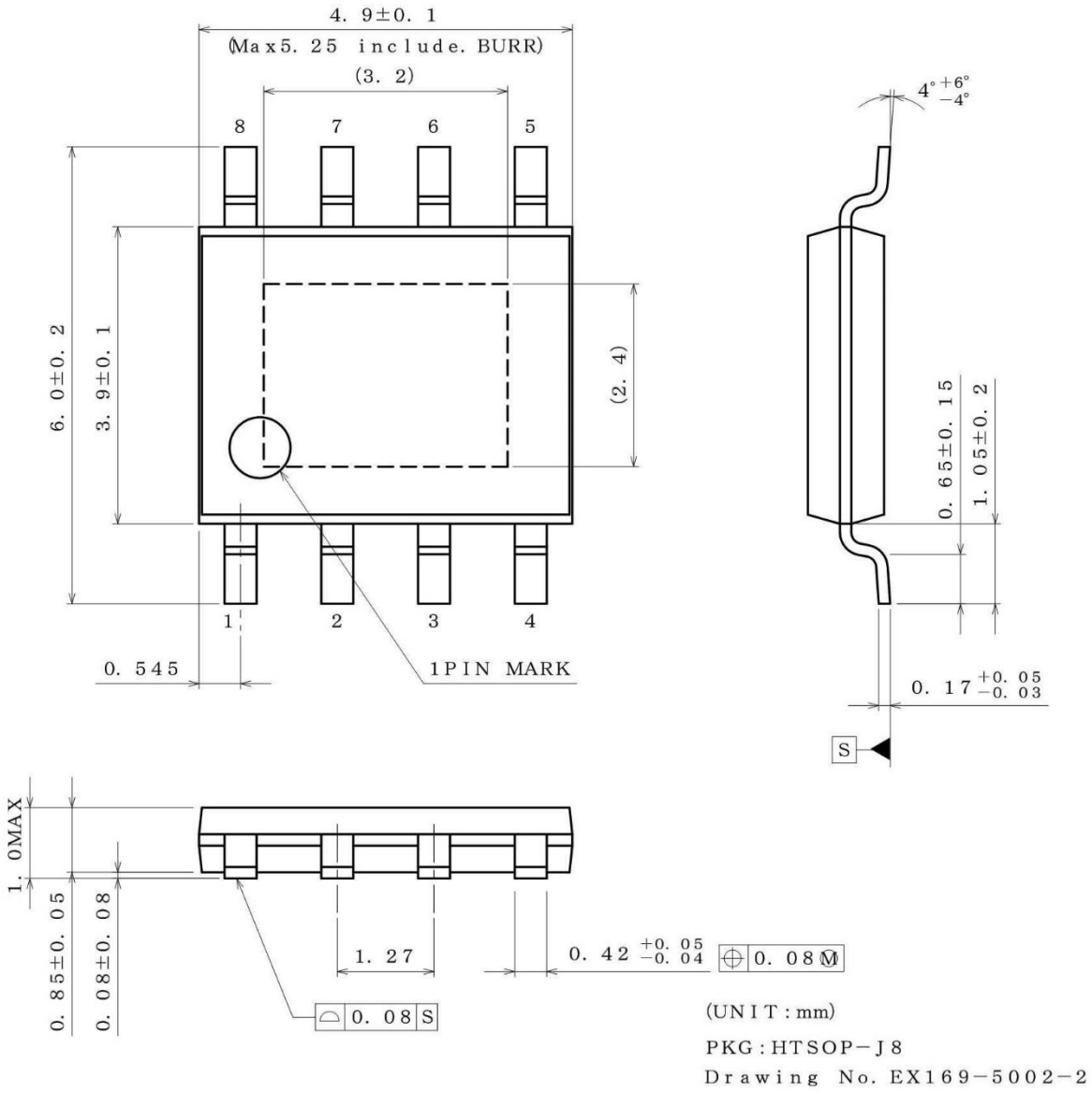
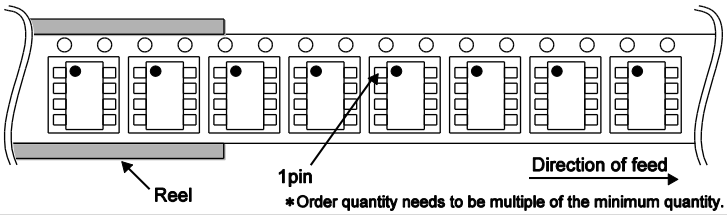
Physical Dimension, Tape and Reel Information

Package Name	HTSOP-J8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

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Revision History

Date	Revision	Changes
7.MAR.2013	001	New Release
6.AUG.2013	002	Add Example of evaluation board layout
8.APR.2014	003	Expression change Output Voltage Setting
24.JUL.2018	004	P.8 Add VIN signal on Figure16. P.9 Add the explanation of UVLO and detailed timing chart. P.11 Add the description. P.14 Add the description.

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

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5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

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