Low Consumption and High Accuracy Shunt Regulator Built-in

High Efficiency and Low Standby Power, CCM corresponding Secondary Side Synchronous Rectification Controller IC

BM1R00146F BM1R00147F BM1R00148F BM1R00149F BM1R00150F

General Description

BM1R00146F-150F are synchronous rectification controller to be used in the secondary-side output. It has a built-in low consumption and high accuracy shunt regulator, which significantly reduces standby power. The shunt regulator is constructed in a completely independent chip that enables it to operate as a GND reference even when used in high side.

At continuous mode operation, further space saving can be realized when operating without the input switching synchronizing signal of the primary side.

BM1R00146F-150F also features a wide operating power supply voltage range of 2.7V to 32V for various output applications.

Finally, by adopting the high-voltage 120V process, it is possible to monitor the drain voltage directly.

Features

- Built-in Low Consumption Shunt Regulator Reducing Standby Power Consumption
- Synchronous Rectification FET Supports High and Low Side
- 120V High Voltage Process DRAIN terminal
- Wide Input Operating Voltage Range of 2.7V to 32V
- Supports LLC and PWM QR Controller
- No Input Required on the Primary-Side at CCM
- Built-in Overvoltage Protection for SH_IN and SH_OUT Terminal
- Built-in Thermal Shutdown Function
- Built-in Auto Shutdown Function
- SOP8 package

Applications

- AC-DC Output Power Conversion Applications: Charger, Adapter, TV, Rice Cooker, Humidifier, Air Conditioning, Vacuum Cleaner, etc.

Key Specifications

- Input Voltage Range: 2.7V to 32V
- Circuit Current (No Switching): 800μA(Typ)
- Circuit Current (Auto Shutdown) : 120μA (Typ)
- DRAIN Terminal Absolute Voltage: 120V
- Operating Temperature Range: -40°C to +105°C

Package **W(Typ) x D(Typ) x H(Max)**
5.00mm x 6.20mm x 1.71mm

SOP8

Lineup Table

Auto Restart Protection Series

Part Number	Compulsion ON Time (μs)	Compulsion OFF Time (μs)
BM1R00146F	NONE	1.3
BM1R00147F	NONE	2
BM1R00148F	NONE	3
BM1R00149F	NONE	3.6
BM1R00150F	NONE	4.6

Part Number	SH_IN OVP	SH_OUT OVP	TSD
BM1R00146F	Auto Restart	Auto Restart	Auto Restart
BM1R00147F			
BM1R00148F			
BM1R00149F			
BM1R00150F			

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

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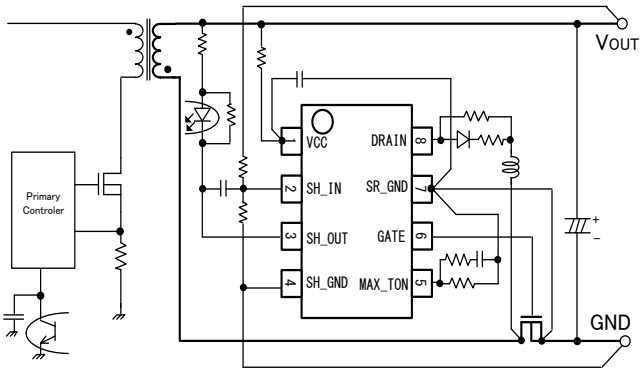
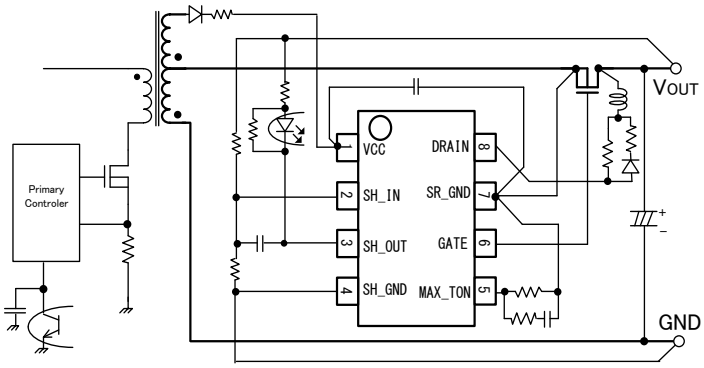
Typical Application Circuits



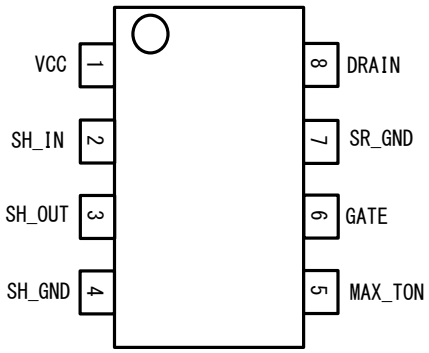
Low Side Application (FLYBACK)



High Side Application (FLYBACK)

Pin Configuration

(TOP VIEW)



Pin Description

Pin No.	Pin Name	Function
1	VCC	Power supply
2	SH_IN	Shunt regulator reference
3	SH_OUT	Shunt regulator output
4	SH_GND	Shunt regulator ground
5	MAX_TON	Set maximum on time
6	GATE	Gate drive
7	SR_GND	Synchronous rectification ground
8	DRAIN	DRAIN monitor

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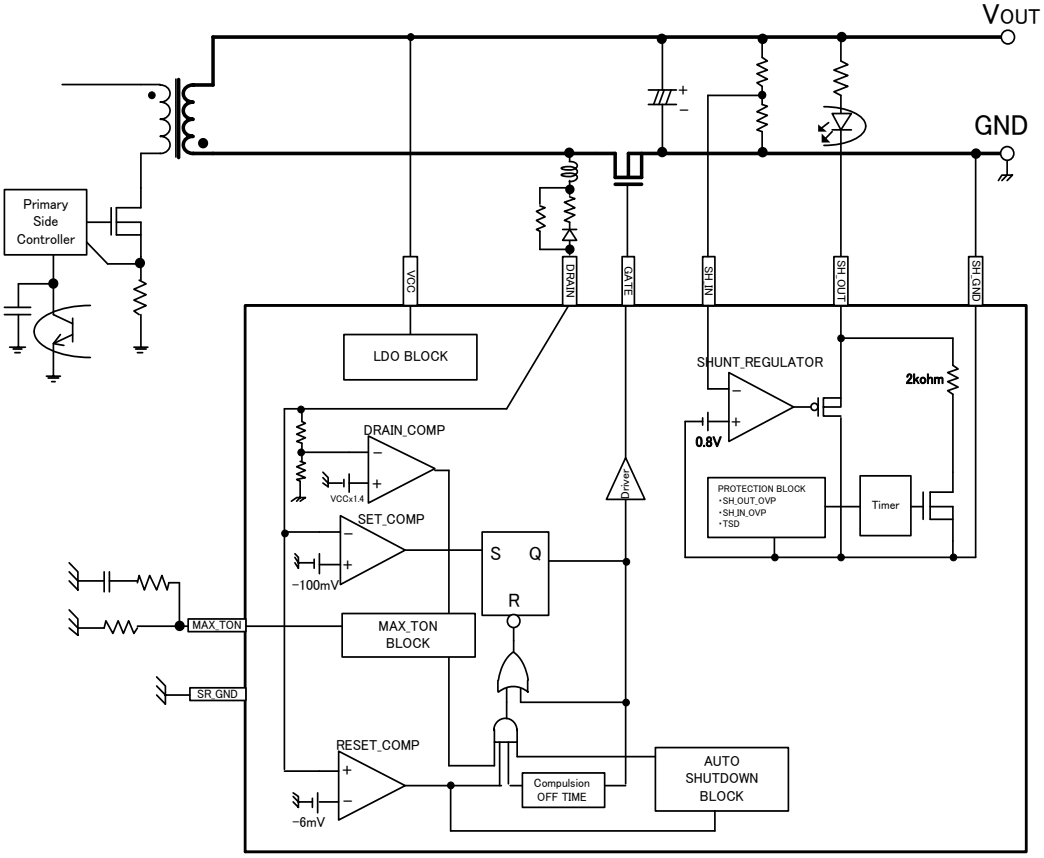
Block Diagram



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Description of Block

1. **SET_COMP Block**
   Monitors the DRAIN terminal voltage, and outputs a signal to turn ON the FET if the DRAIN terminal voltage is less than or equal to -100mV (Typ).

2. **RESET_COMP Block**
   Monitors the DRAIN terminal voltage and outputs a signal to turn OFF the FET if the DRAIN terminal voltage is more than or equal to -6mV (Typ).

3. **Compulsion OFF TIME Block**
   When the FET is turned OFF due to RESET_COMP detection, resonance waveforms appear on the DRAIN terminal. To prevent the noise from turning ON the FET, an OFF state should be forced for a certain time. Compulsion OFF time is within a range of 1.3μs to 4.6μs, which is different for each series number (refer to page.1 table).

   Operation sequence of each block is shown on the figure below.

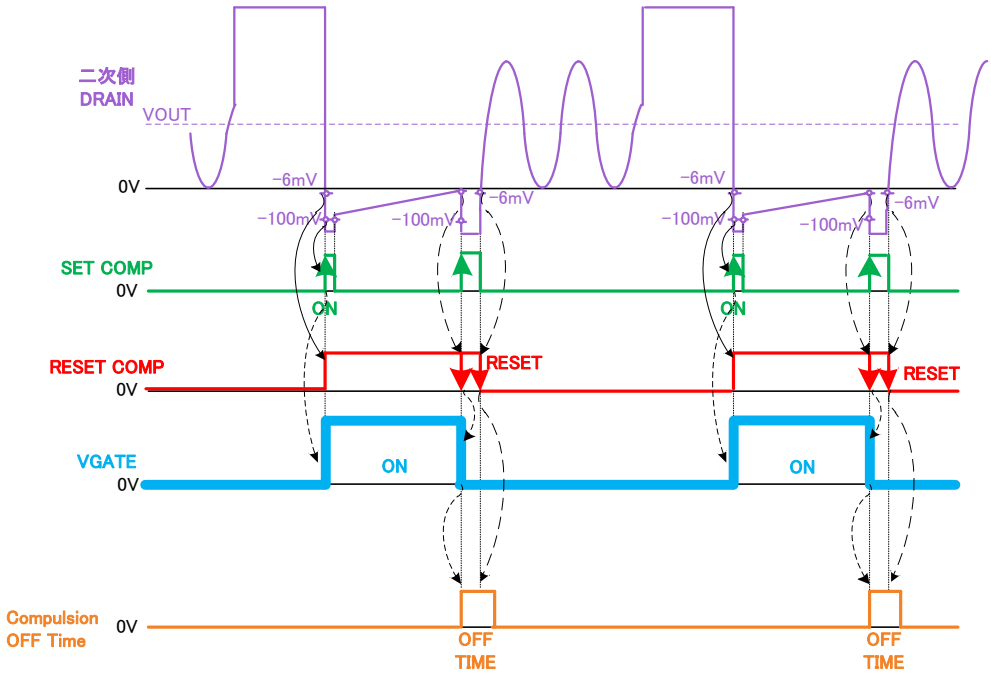

Figure 1. Operation sequence

About Maximum Input Frequency

The Maximum Operating Frequency of the IC depends on the Compulsion ON/OFF Time. For example, BM1R00146F Compulsion ON Time is equal to 0μs (None), Compulsion OFF Time is equal to 1.3μs. Considering a variation of 9%, the maximum input frequency is given by the following:

$$f_{MAX} = 1 / ((0\mu s + 1.3\mu s) \times 1.09) = 706kHz$$

However, since the frequency varies greatly due to the input voltage and load, it will be necessary to select the series in accordance with each application.

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Description of Block – continued

4. MAX_TON Block

MAX_TON block sets the maximum ON time. DRAIN terminal voltage starts counting when the rising edge of the output voltage exceeds V_{CC} × 1.4V (Typ). In addition, the recounting starts when it detects another rising edge. The synchronous rectification FET will be forced OFF after the set time has elapsed. The time can be adjusted by varying the resistance value of the resistor connected to the MAX_TON terminal.
The relationship between the resistance value (R_{MAX_TON}) and set time (T_{MAX_TON}) is described as follows:

$$R_{MAX_TON}\ (k\Omega) = t_{MAX_TON}\ (\mu s) \times 10(k\Omega / \mu s)$$

Calculation Example:
If you want to set the maximum ON time to 10μs, the value of R_{MAX_TON} is as follows:

$$10\mu s \times 10(k\Omega / \mu s) = 100k\Omega$$

However, the formula above is for an ideal approximation only; it is still strongly advised that the operation of the actual application should still be verified.
By setting this time, it becomes possible to prevent the simultaneous ON operation of the primary side and the secondary side in continuous mode.
The drive sequence in continuous mode operation is shown in the figure below:

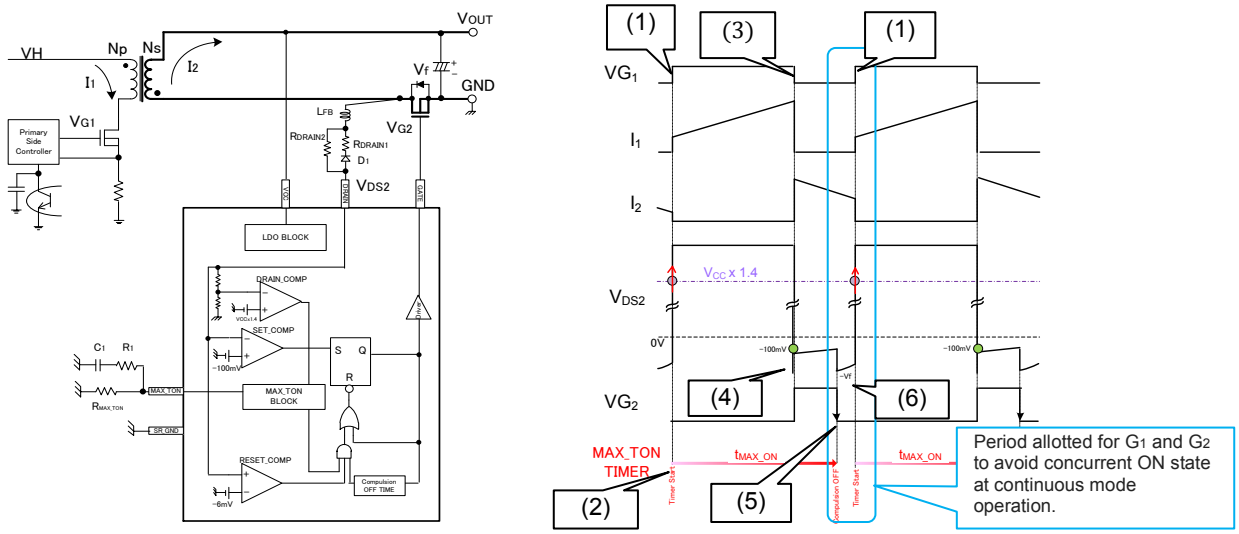

Figure 2. The drive sequence in continuous mode operation

(1) Primary side FET = ON. Current I_1 flows to the primary side FET. Secondary side drain voltage V_{DS2} rises.
(2) The V_{DS2} = V_{CC} × 1.4 detects the rise edge of the threshold, MAX_TON timer start.
(3) Primary side FET = OFF. Current I_2 flows through the Body Diode of the secondary side FET (OFF state).
(4) Secondary side drain voltage V_{DS2} < - 100mV by I_2 Current, Secondary side FET=ON.
(5) Elapsed the set time in MAX_TON terminals, the secondary-side FET = compulsory OFF.
(6) Since the I_2 current flows through the Body Diode, V_f voltage occurs.

a capacitor C_1 and a Moreover, in order to reduce as much as possible the influence of the switching noise, resistor R_1 in series should be connected to the MAX_TON terminal. The capacitance should approximately be 1000pF, and the resistance value is recommended to be around 1kΩ.This also serves as phase compensation of MAX_TON terminal and therefore should be connected.
This function may be disabled by pulling up the MAX_TON terminal to VCC pin in quasi-resonant and current resonance applications which do not operate on continuous mode. The 1000pF and 1kΩ resistor is also unnecessary.

5. AUTO SHUTDOWN Block

The Auto Shutdown block automatically turns the synchronous rectification ON/OFF depending on the presence or absence of the DRAIN terminal pulse. Shutdown occurs if the input pulses on the DRAIN terminal has more than 200us between pulses. This stops the synchronous rectification operation. The IC will restart the synchronous rectification after it detects 265 occurrences of input pulses on the DRAIN terminal.

6. SHUNT REGULATOR Chip

A high-accuracy shunt regulator with low consumption is used for controlling the output voltage of the AC/DC. Since the synchronous rectification and the shunt regulator are built in a completely different chip, GND separation is possible. Therefore, it becomes possible to place the shunt regulator on the secondary-side GND reference in the synchronous rectification applications in case of disposing the High Side FET. It can also be used as protection for the comparator, the secondary side OVP, FET overheat protection, etc.

7. PROTECTION Block

When an abnormal condition is detected after the timer count is completed, the photo coupler from SH_OUT terminal is driven to stop the switching operation on the primary side.

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Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
VCC Input Voltage	V_{MAX_VCC}	-0.3 to +40(Note 1)	V
MAX_TON Input Voltage	$V_{MAX_MAX_TON}$	-0.3 to +40(Note 1)	V
SH_IN Input Voltage	$V_{MAX_SH_IN}$	-0.3 to +40(Note 2)	V
SH_OUT Input Voltage	$V_{MAX_SH_OUT}$	-0.3 to +40(Note 2)	V
Gate Input Voltage	V_{MAX_GATE}	-0.3 to 15.5(Note 1)	V
Drain Input Voltage	V_{MAX_DRAIN}	120(Note 1)(Note 3)	V
Maximum Junction Temperature	Tjmax	+150	°C
Operating Temperature Range	Topr	-40 to +105	°C
Storage Temperature	Tstr	-55 to +150	°C

(Note 1) Reference SR_GND
(Note 2) Reference SH_GND
(Note 3) When a negative voltage is applied, current flows through the ESD protection device.
This current value is about 6mA or less and will require a current limiting resistor to the DRAIN terminal
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse in case the IC is operated over the absolute maximum ratings.

Thermal Resistance (Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s (Note 3)	2s2p (Note 4)	
SOP8				
Junction to Ambient	θ_{JA}	197.4	109.8	°C/W
Junction to Top Characterization Parameter (Note 2)	Ψ_{JT}	21	19	°C/W

(Note 1) Based on JESD51-2A(Still-Air)
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

Recommended Operating Conditions (Ta = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	20	32	V
MAX_TON Resistor Range	R_{MAX_TON}	56	-	300	kΩ
MAX_TON R1	R_1	0.5	1	2	kΩ
MAX_TON C1	C_1	680	1000	2200	pF

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Electrical Characteristics (Unless otherwise specified V_{CC}=20V Ta=25°C)

Parameter	Symbol	Spec			Unit	Conditions
		MIN	TYP	MAX		
Circuit Current						
Circuit Current1	I_{ON1}	0.5	1	2	mA	f_{SW}=50kHz at Switching Mode (GATE=OPEN)
Circuit Current at Sleep Mode	I_{SLEEP}	60	120	200	μA	At Shutdown Mode
Circuit Current at Normal Mode	I_{ACT}	350	800	1400	μA	Switching STOP Mode
Circuit Current at UVLO Mode	I_{OFF}	18	35	60	μA	V_{CC}=1.9V
VCC Item						
VCC UVLO Threshold Voltage1	V_{UVLO1}	2.00	2.30	2.65	V	V_{CC} Sweep Up
VCC UVLO Threshold Voltage2	V_{UVLO2}	1.95	2.25	2.60	V	V_{CC} Sweep Down
SR Controller BLOCK						
GATE Turn ON Threshold	V_{GONN}	-150	-100	-50	mV	V_{DRAIN}=+300mV to -300mV
GATE Turn OFF Threshold	V_{GOFF}	-10	-6	-1	mV	V_{DRAIN}=-300mV to +300mV
Compulsion OFF Time(Note 5)	t_{COFF}	1.140	1.300	1.460	μs	BM1R00146F
		1.700	2.000	2.300	μs	BM1R00147F
		2.730	3.000	3.270	μs	BM1R00148F
		3.276	3.600	3.924	μs	BM1R00149F
		4.186	4.600	5.014	μs	BM1R00150F
MAX_TON BLOCK						
MAX_TON Timer Start Threshold Voltage	$V_{MAX_ON_START}$	24	28	32	V	V_{CC}=20V, DRAIN Terminal Voltage
MAX_TON Timer	t_{MAX_ON}	9.4	10	10.6	μs	R_{MAX_TON}=100kΩ, V_{CC}=3V, V_{DRAIN}=-0.3↔7V
MAX_TON Output Voltage	V_{MAX_ON}	0.24	0.40	0.56	V	
Auto Shutdown BLOCK						
Auto Shutdown Detect Time	t_{SHD}	120	200	320	μs	No Pulse to DRAIN Terminal
Auto Shutdown Cancel Pulse Number	P_{ACT}	-	265	-	time	Input Pulse to DRAN Terminal
Drain Monitor BLOCK						
Drain Sink Current	I_{D_SINK}	130	250	550	μA	V_{DRAIN}=120V
Drain Terminal Source Current1	I_{DRAIN_SO1}	-23	-11	-5	μA	V_{DRAIN}=0.1V
Drain Terminal Source Current2	I_{DRAIN_SO2}	-3	-1	-0.3	μA	V_{DRAIN}=-0.2V
Driver BLOCK						
GATE Terminal High Voltage	V_{GATE_H1}	11	12	14	V	V_{CC}=20V
High Side FET ON-Resistance (V_{CC}=2.7V)	R_{HIONR1}	12.0	23.0	50.0	Ω	V_{CC}=2.7V, I_{OUT}= -10mA
High Side FET ON-Resistance (V_{CC}=5V)	R_{HIONR2}	6.0	12.0	24.0	Ω	V_{CC}=5.0V, I_{OUT}= -10mA
High Side FET ON-Resistance (V_{CC}=10V)	R_{HIONR3}	4.0	9.0	18.0	Ω	V_{CC}=10V, I_{OUT}= -10mA
Low Side FET ON-Resistance (V_{CC}=2.7V)	$R_{LOWONR1}$	1.1	2.2	4.4	Ω	V_{CC}=2.7V, I_{OUT}= +10mA
Low Side FET ON-Resistance (V_{CC}=5V)	$R_{LOWONR2}$	0.9	1.8	3.6	Ω	V_{CC}=5.0V, I_{OUT}= +10mA
Propagation Delay to FET Turn ON	t_{DELAY_ON}	-	50	-	ns	V_{DRAIN}=+300mV to -300mV
Propagation Delay to FET Turn OFF	t_{DELAY_OFF}	-	100	-	ns	V_{DRAIN} =-300mV to +300mV

(Note 5) See the lineup table in page1.

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Electrical Characteristics (Unless otherwise specified V_{SH_OUT}=20V Ta=25°C)

Parameter	Symbol	Spec			Unit	Conditions
		MIN	TYP	MAX		
Shunt Regulator BLOCK (Other Chip)						
Reference Voltage	V_{SHREF}	0.796	0.800	0.804	V	V_{SH_OUT}=5V SH_OUT Sink Current =100μA
Reference Voltage Changing Ratio by Temperature	ΔV_{SHEMP}	-	-4	-	mV	V_{SH_OUT}=5V SH_OUT Sink Current =100μA Temperature=25°C to 105°C
SH_OUT Coefficient of the Reference Voltage1	ΔV_{SHREF1}	-	1	-	mV	V_{SH_OUT}=2.7V to 5V SH_OUT Sink Current =100μA
SH_OUT Coefficient of the Reference Voltage2	ΔV_{SHREF2}	-	2	-	mV	V_{SH_OUT}=5V to 20V SH_OUT Sink Current =100μA
Reference Input Current	I_{SH_IN}	-0.2	0.0	0.2	μA	V_{SH_IN}=2V
Dynamic Impedance1	Z_{SH_OUT1}	-	0.3	-	Ω	SH_OUT Sink Current =100μA to 300μA (V_{SH_OUT}=2.7V)
Dynamic Impedance2	Z_{SH_OUT2}	-	0.2	-	Ω	SH_OUT Sink Current =100μA to 300μA (V_{SH_OUT}=20V)
SH_OUT Current at SH_IN=Low	I_{SH_OUT}	20	40	75	μA	V_{SH_IN}=0V, V_{SH_OUT}=20V
SH_OUT Sink Current	$I_{SH_OUT_MIN}$	1	-	-	mA	V_{SH_IN}=0.85V, V_{SH_OUT}=2.7V
SH_IN OVP Detection Voltage1	V_{SHI_OVP1}	0.90	1.00	1.10	V	V_{SH_IN}= Sweep Up
SH_IN OVP Detection Voltage2	V_{SHI_OVP2}	0.85	0.95	1.05	V	V_{SH_IN}= Sweep Down
SH_OUT OVP Detection Voltage1	V_{SHO_OVP1}	32.5	35	37.5	V	V_{SH_OUT} Sweep Up
SH_OUT OVP Detection Voltage2	V_{SHO_OVP2}	31.5	34	36.5	V	V_{SH_OUT} Sweep Down
Protection Timer	$t_{PROTECTION}$	100	200	300	μs	
SH_OUT Sink Current at Protection Mode	$I_{PROTECTION}$	1.3	2.5	5	mA	V_{SH_OUT}=5V, V_{SH_IN}=0V

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Typical Performance Curves

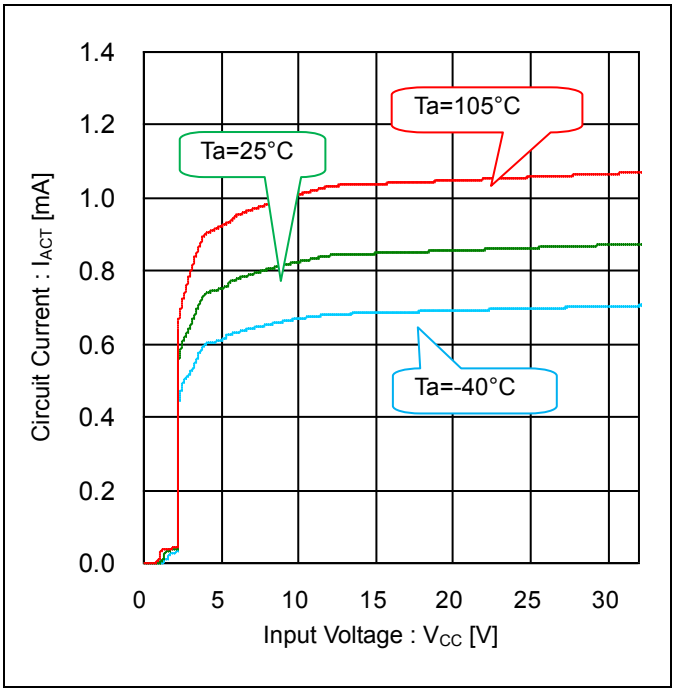

Figure 3. Circuit Current vs Input Voltage
(Stop Switching State)

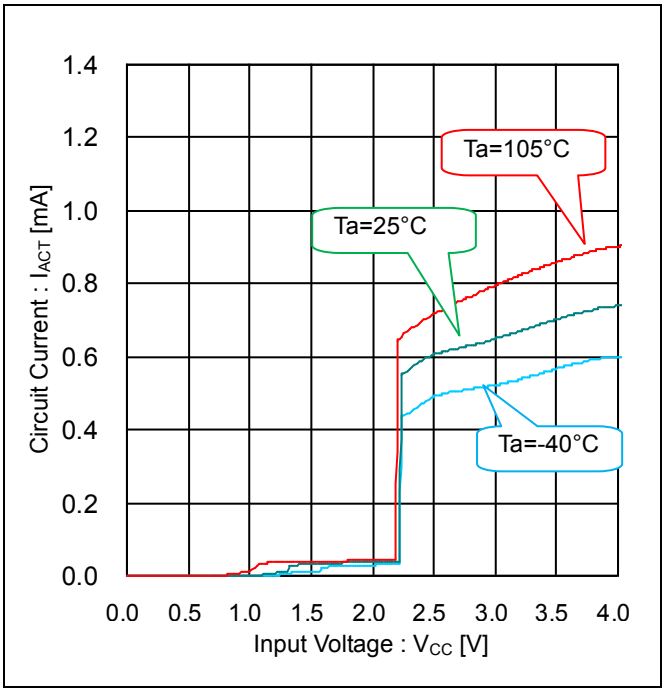

Figure 4. Circuit Current vs Input Voltage
(Stop Switching State VCC Zoom)

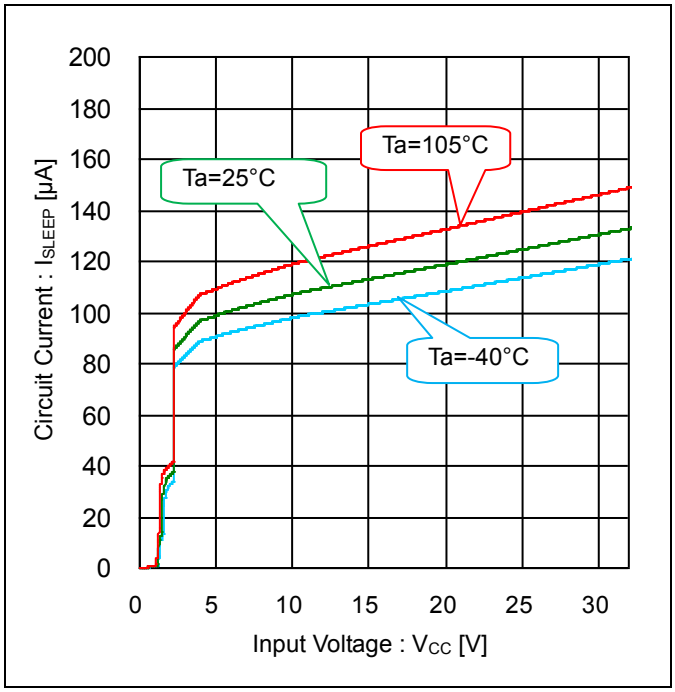

Figure 5. Circuit Current vs Input Voltage
(at Shut Down State)

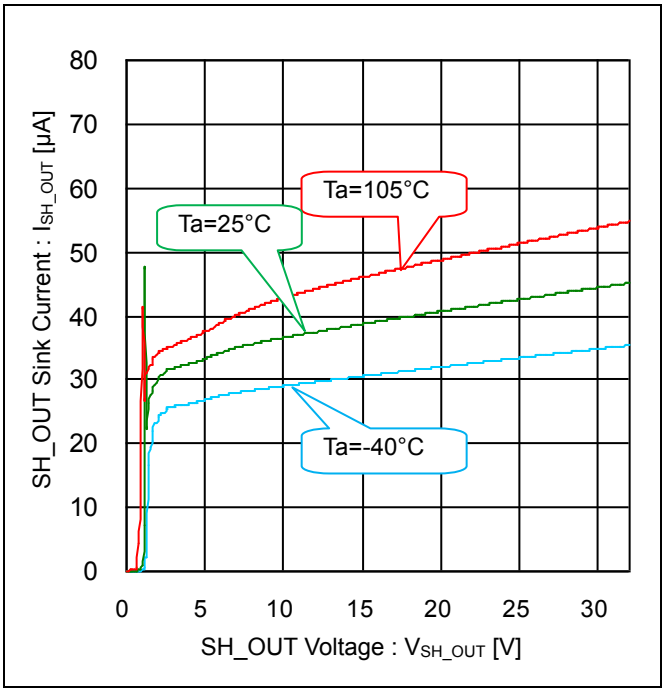

Figure 6. Circuit Current vs SH_OUT Voltage
(V_{SH_IN}=0V)

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Typical Performance Curves - continued

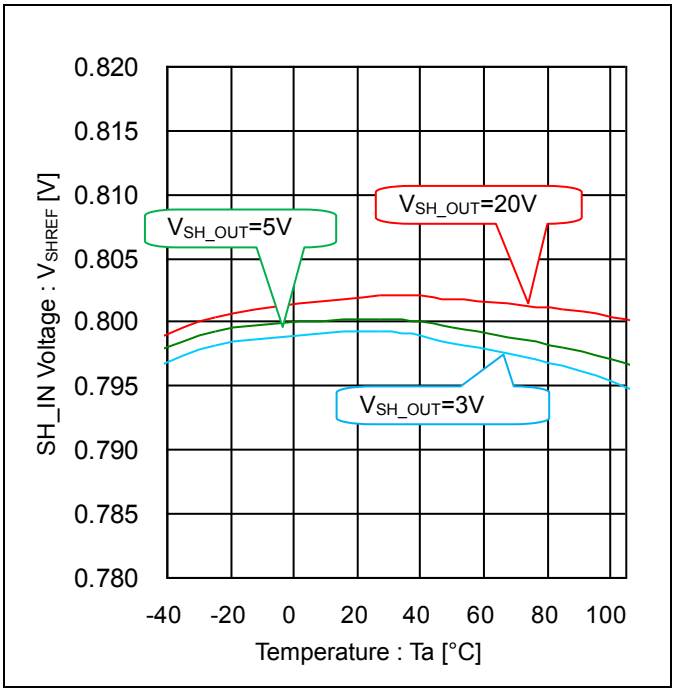

Figure 7. SH_IN Voltage vs Temperature
(I_{SH_OUT}=100μA)

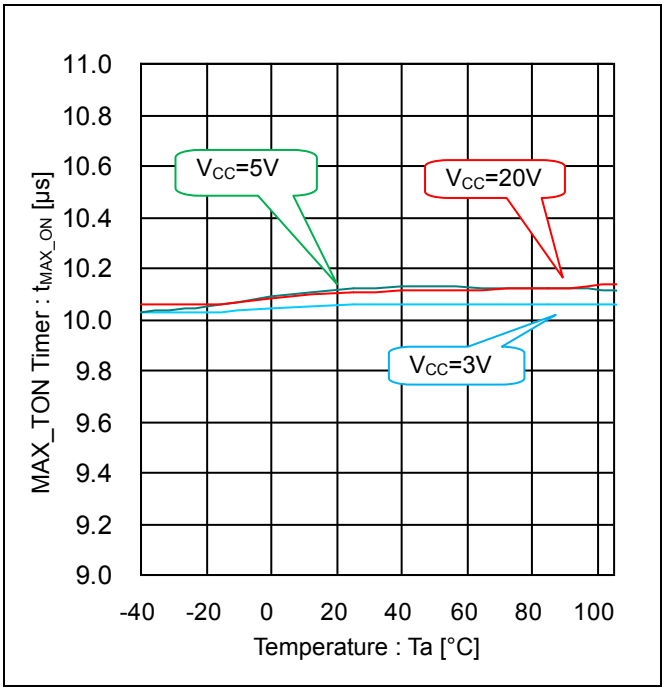

Figure 8. MAX_TON Timer vs Temperature
(R_{MAX_TON}=100kΩ, V_{DRAIN}=-0.3V<->VCC x 2)

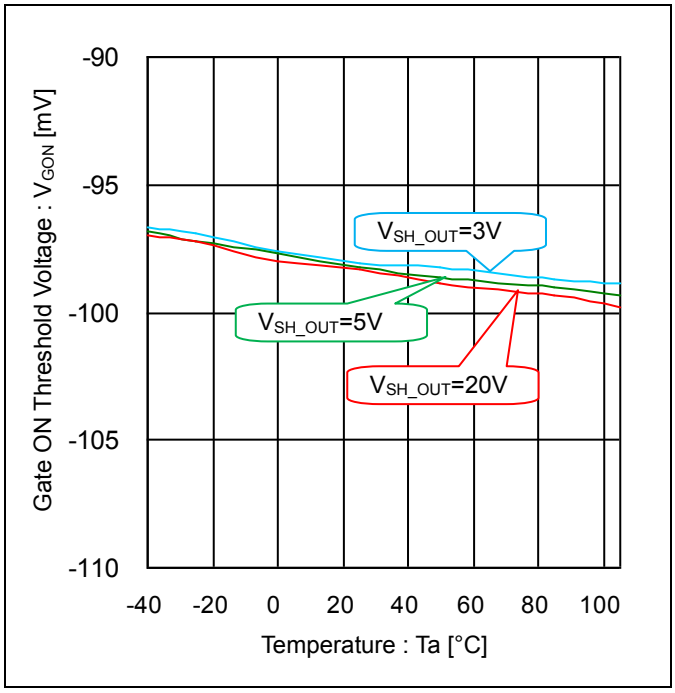

Figure 9. Gate ON Threshold vs Temperature
(DRAIN Sweep Down)

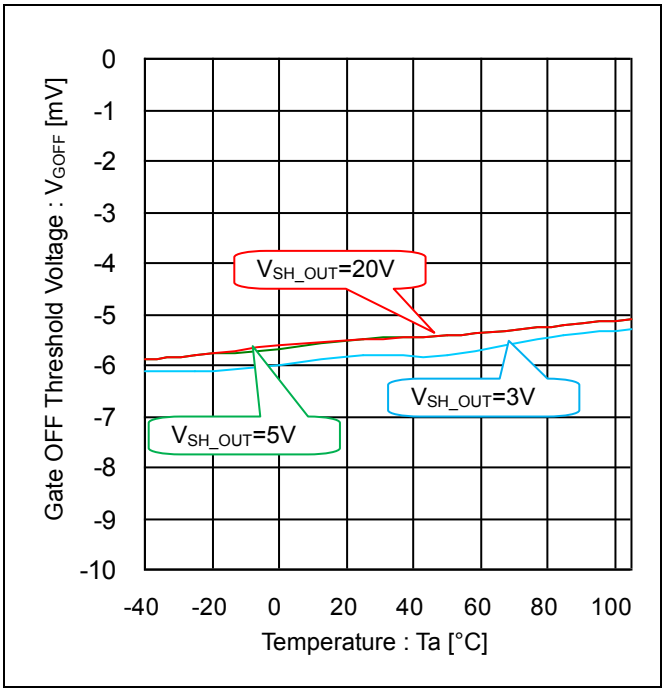

Figure 10. Gate OFF Threshold vs Temperature
(DRAIN Sweep Up)

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Typical Performance Curves - continued

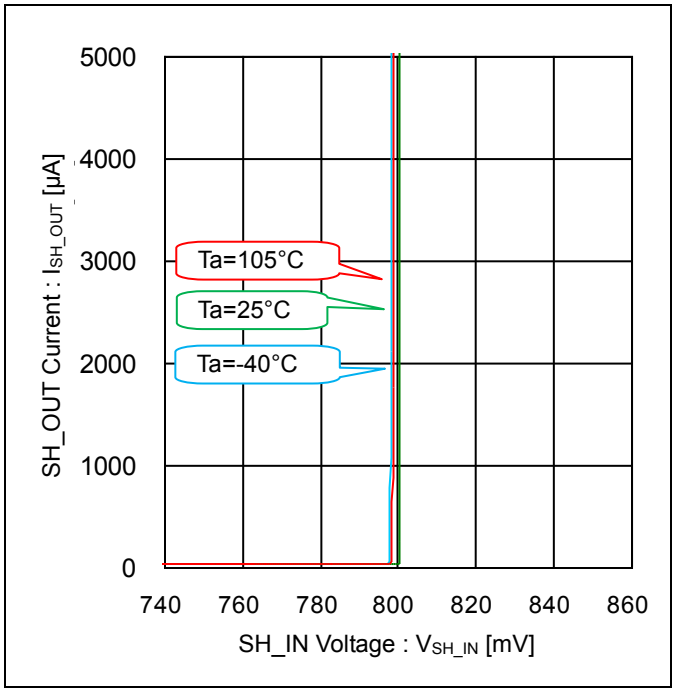

Figure 11. SH_OUT Current vs SH_IN Voltage
(V_{SH_OUT}=5V)

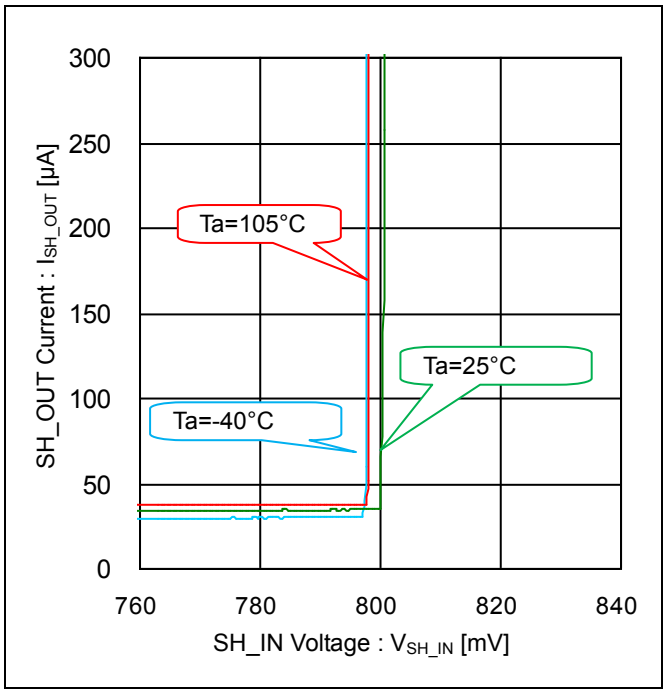

Figure 12. SH_OUT Current vs SH_IN Voltage
(V_{SH_OUT}=5V, ZOOM UP)

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Timing Chart

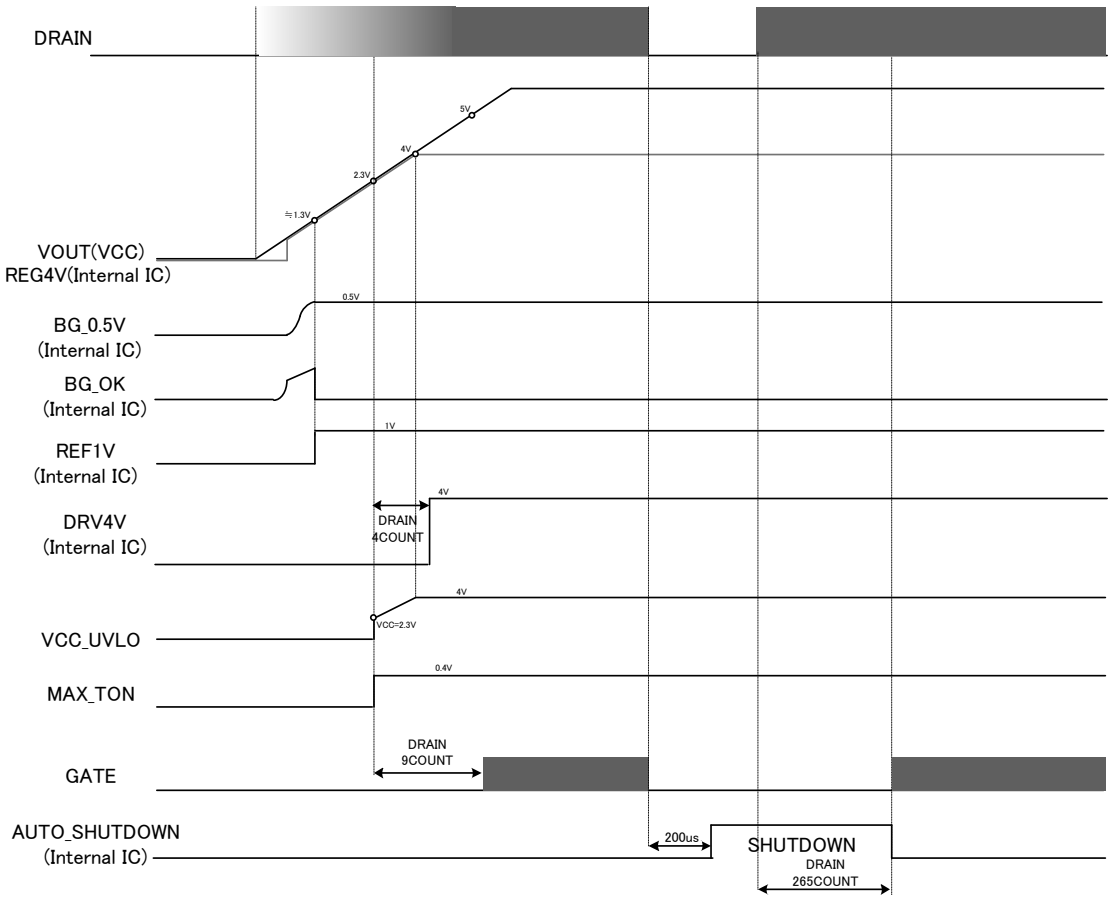

Figure 13. Start Up Sequence

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Application Examples

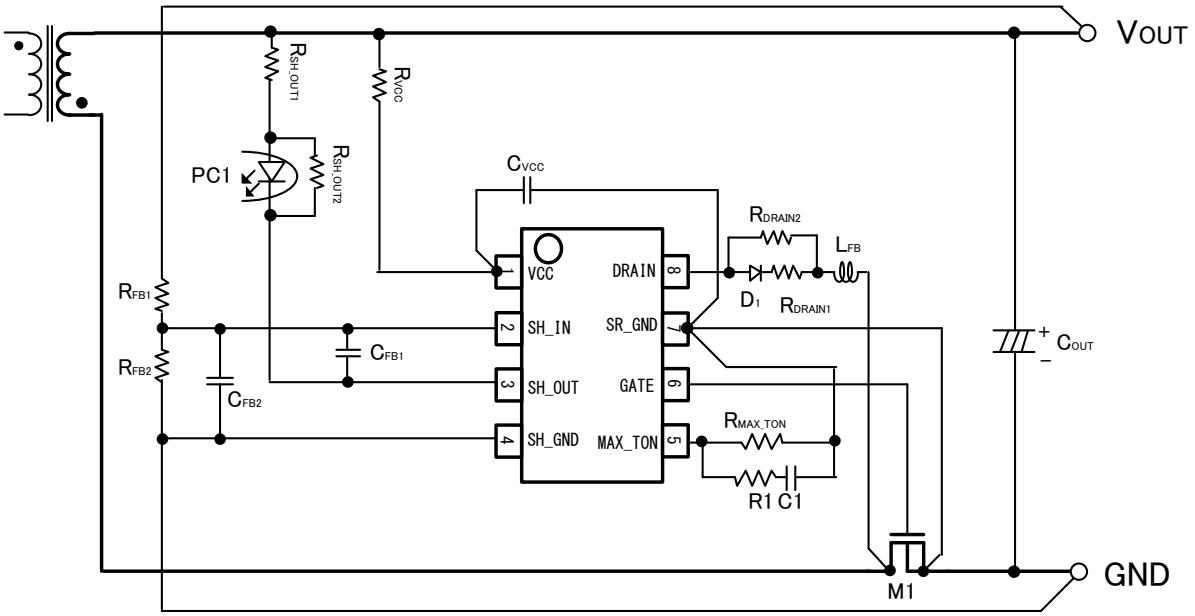

Figure 14. Flyback Application Circuit
(Low Side FET)

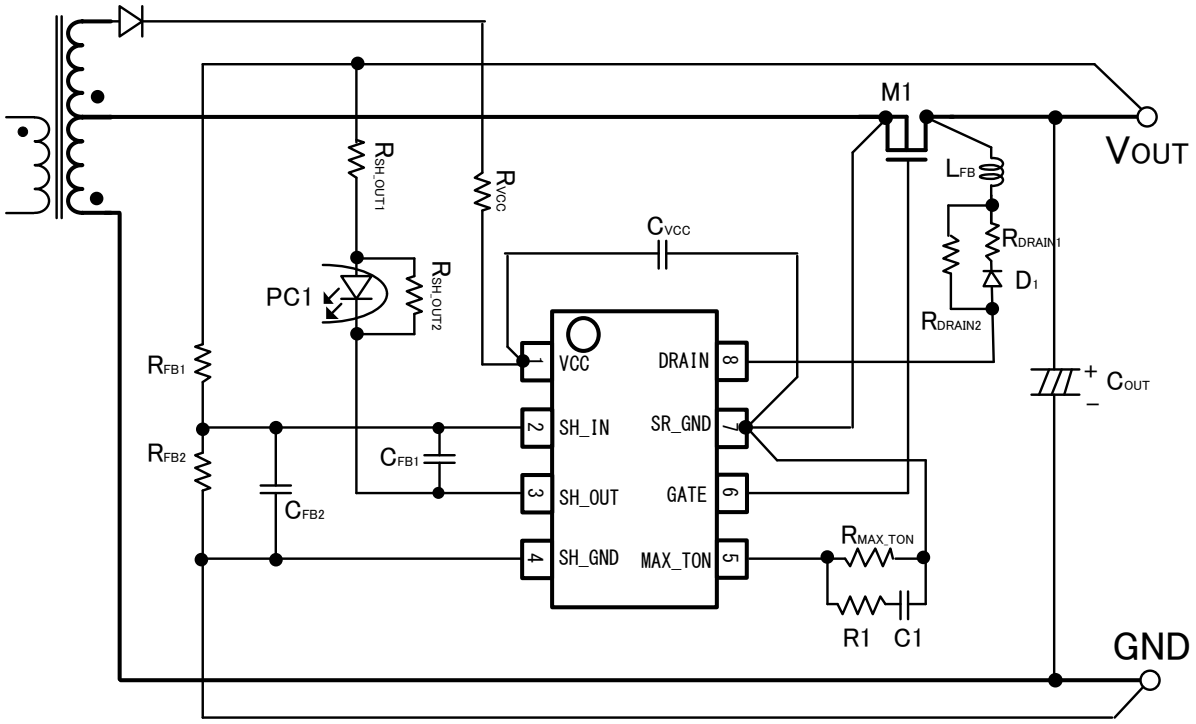

Figure 15. Flyback Application Circuit
(High Side FET)

Built-in shunt regulator in the IC has been completely separated from internal and synchronous rectification control IC. Therefore, the shunt regulator is possible to be used as a GND reference in High Side type of flyback application.

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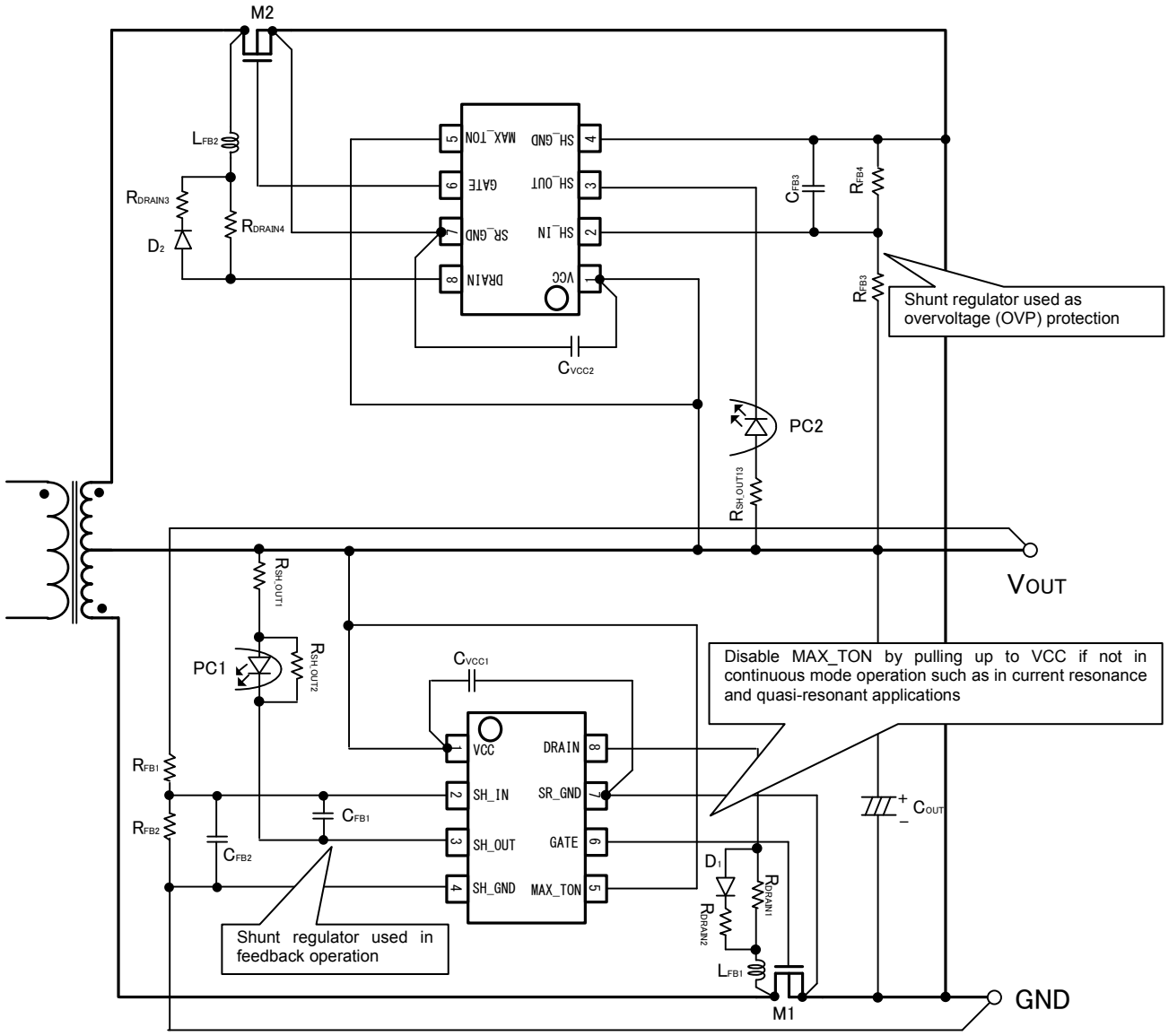

Figure 16. Resonant Half-bridge Application Circuit

Regarding Protection Applications

The built-in shunt regulator is high-voltage, low current consumption, high accuracy, and also suitable as a comparator for protection application. On the above current resonant circuit, the shunt regulator is used as an overvoltage protection circuit.

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Selection of Externally Connected Components

1. MAX_TON Pin Setting
   A resistance value which is connected to the MAX_TON terminal is used to set the timer to force the GATE output OFF. (For detailed operation, please see "each block Operation / MAX_TON blocks")
   Set timer is proportional to the resistance value which can be set in the range of 56k to 300k. This IC is capable of an accuracy of 10us ± 6% at 100kΩ. However, accuracy deteriorates as the resistance value gets further away from 100kΩ.
   For example, 5.6μs ±0.9μs at 56kΩ, 30μs ±4.5μs at 300kΩ.
   (See graph below)

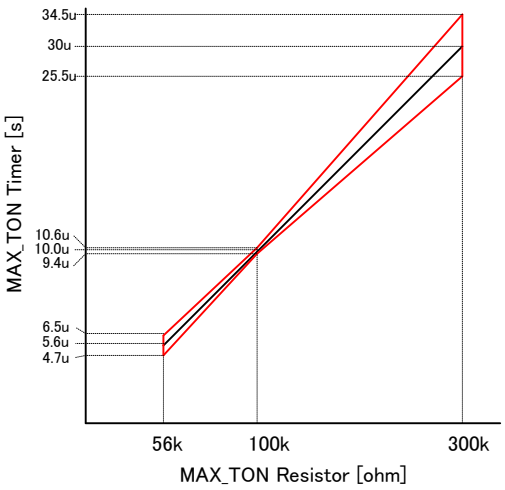

Figure 17. MAX_TON Timer vs MAX_TON Resistor(R_{MAX_TON})

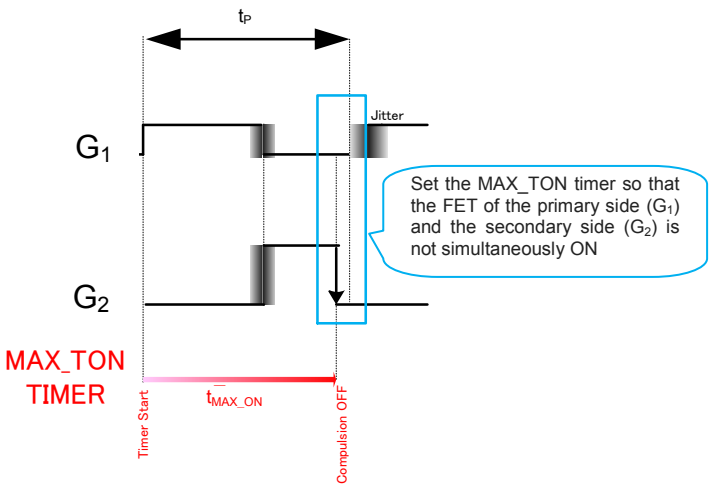

Figure 18. Primary FET and Secondary FET Sequence at CCM Mode

To prevent destruction due to surge current in continuous mode, set the MAX_TON timer before turning on the primary side FET (G_1) to forcibly OFF the secondary side FET (G_2). Regarding such variations, select a resistance value of MAX_TON terminal so that the MAX_ON timer setting time is less than one cycle in the primary side ($T_P > T_{MAX_ON}$).
- The primary side of the maximum frequency = f_{MAX} [Hz]
- The primary side of the maximum frequency accuracy = Δf_{MAX} [%]
- The primary side of the jitter frequency = f_{JITTER} [Hz]
- Secondary side MAX_TON timer time = t_{MAX_ON}
- Secondary side MAX_TON timer time accuracy = Δt_{MAX_ON}
- Secondary side MAX_TON When the connection resistance accuracy = ΔR

$$R_{MAX_TON}[k\Omega] < \frac{10000\ [k\Omega][kHz]}{(1+\Delta t_{MAX_ON}[\%]+\Delta R[\%]+\Delta f_{MAX}[\%])\times(f_{MAX}[kHz]+f_{JITTER}\ [kHz])}$$

Frequency Variation Ratio

Maximum Frequency Value

2. Calculation Example
   Primary side frequency 100kHz ± 5%
   Primary side jitter frequency 8kHz
   Secondary side MAX_TON timer accuracy = 7%
   Secondary side MAX_TON connection resistance accuracy = 1%

$$R_{MAX_TON}\ [k\Omega] < \frac{10000\ [k\Omega][kHz]}{(1+5\%+1\%+7\%)\times(100kHz+8kHz)} = 81.94\ [k\Omega]$$

With these conditions, MAX_TON Resistor(R_{MAX_TON}) should be set to 81kΩ or less. In addition, it is recommended that the temperature characteristics of each component should also be taken into account.

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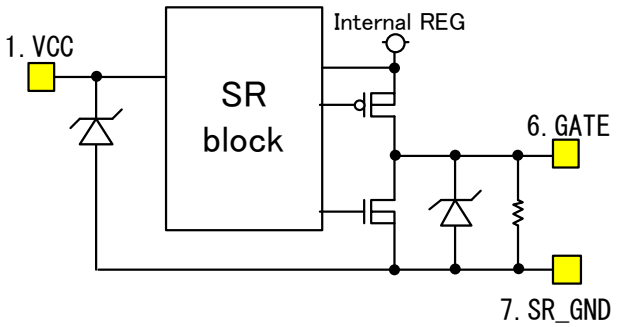
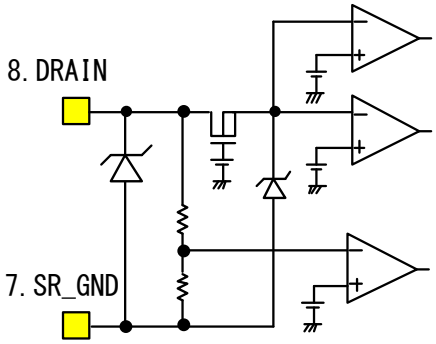
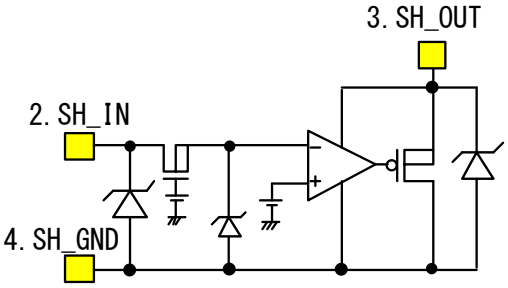
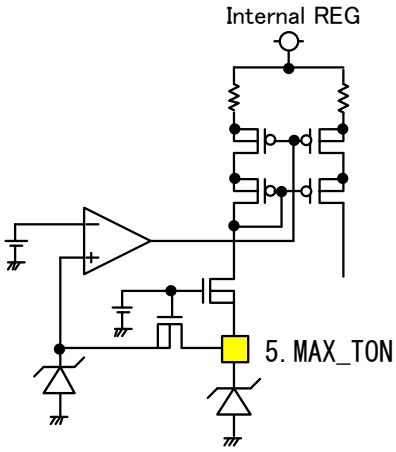
I/O Equivalent Circuits

PIN 1: VCC / PIN 6: GATE / PIN 7: SR_GND	PIN 8: DRAIN
	
PIN 2: SH_IN / PIN 3: SH_OUT / PIN 4: SH_GND	**PIN 5: MAX_TON**
	

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Notes on the layout

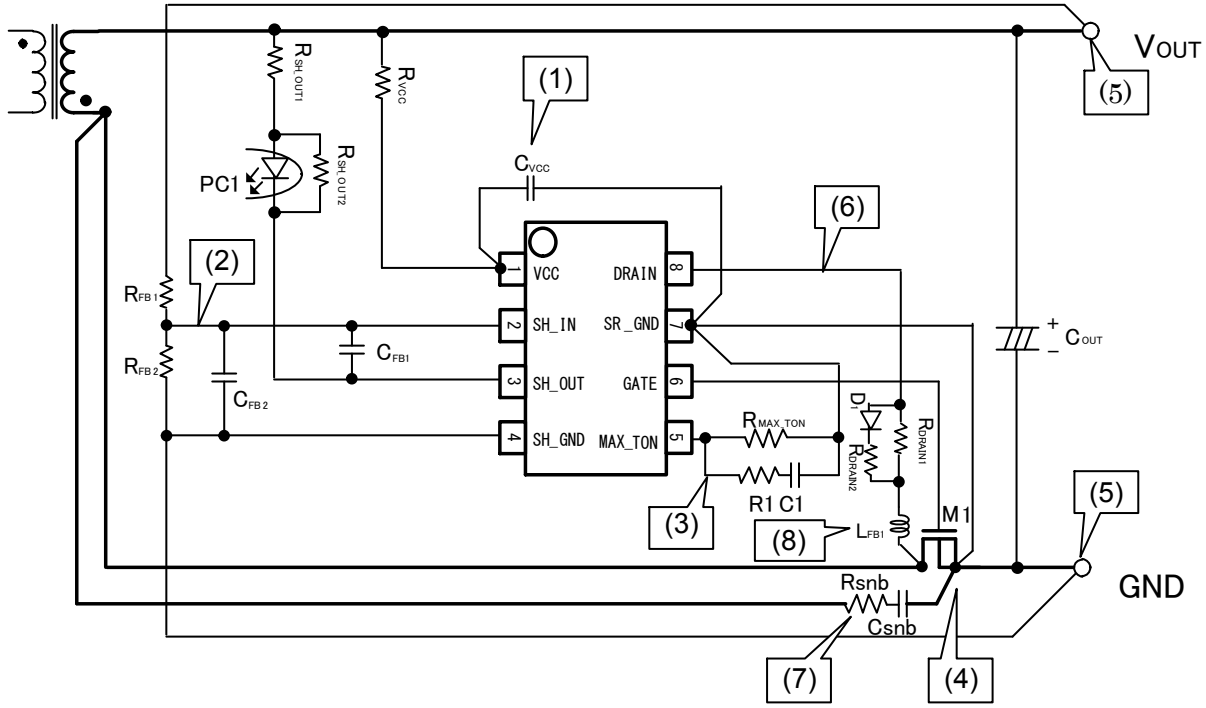

Figure 19. Flyback Application Circuit
(Low Side FET)

(1) VCC line may malfunction under the influence of switching noise.
Therefore, it is recommended to insert a capacitor C_{VCC} between the VCC and SR_GND terminal.
(2) SH_IN terminal is a high impedance line. To avoid crosstalk, electrical wiring should be as short as possible and not in parallel with the switching line.
(3) MAX_TON terminal has a 0.4V output. The external components of the MAX_TON terminal affects the forced OFF time due to switching. Thus, R1 and C1 should be connected to MAX_TON terminal as near as possible. It is also recommended to use an independent electrical wiring in connection with SR_GND terminal.
(4) The synchronous rectification controller IC must accurately monitor the V_{DS} generated in the FET. Accordingly, the electrical wiring between the DRAIN to DRAIN and SR_GND to SOURCE of the IC and FET respectively **should be connected independently.**
(5) The SH_GND of the shunt regulator and the feedback resistors of V_{OUT} are recommended to be connected to the GND of the output with an independent electrical wiring.
(6) The DRAIN terminal is a 0↔100V switching line. Use a narrow wiring and connect as short as possible.
(7) Use an independent wiring if connecting a snubber circuit between the DS of the FET. The connection of the transformer output and the SOURCE of the FET should be thick and short as possible.
(8) Due to the DRAIN pin detects the small voltage, a malfunction which the switch turns ON/OFF caused by the surge voltage may occur. So that, the filters such as the ferrite bead are recommended for alleviating the surge voltage.

Configuration example(Note 6) :
L_{FB1} (a ferrite bead for suppressing the surge voltage) : MMZ1608S202A
D_1 (a schottky barrier diode) : RB751G-40
R_{DRAIN1} (a filter resistor for the FET turn off) : 0.3k - 2kΩ
R_{DRAIN2} (a current limiting resistor to the DRAIN terminal) : 150Ω

(Note 6) The value is not a guaranteed value, but for reference. Please choose the optimum values of the components after sufficient evaluations based on the actual application.

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Terminals**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes - continued

12. Regarding Input Pins of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

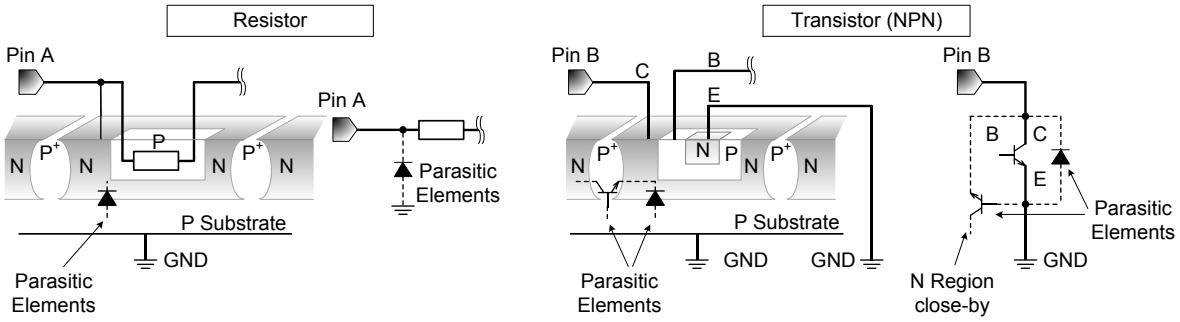

Figure 20. Example of Monolithic IC Structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

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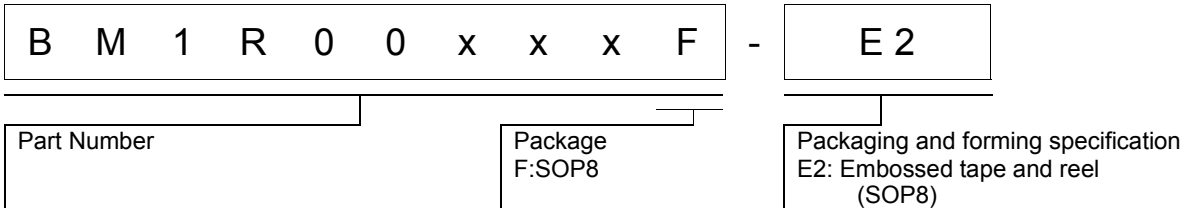
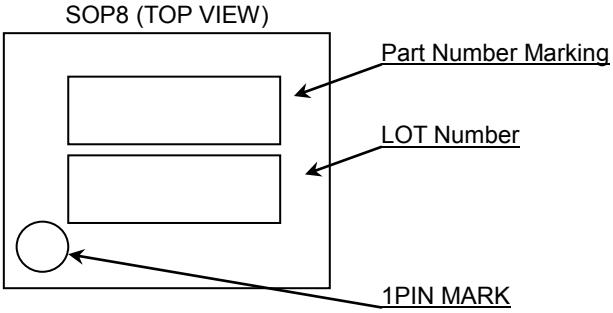
Ordering Information



Marking Diagram



Part Number Marking	Package	Orderable Part Number
00xxx	SOP8	BM1R00xxxF-E2

Auto Restart Protection Series

Part Number	Part Number Marking	Compulsion ON Time (μs)	Compulsion OFF Time (μs)
BM1R00146F	00146	NONE	1.3
BM1R00147F	00147	NONE	2
BM1R00148F	00148	NONE	3
BM1R00149F	00149	NONE	3.6
BM1R00150F	00150	NONE	4.6

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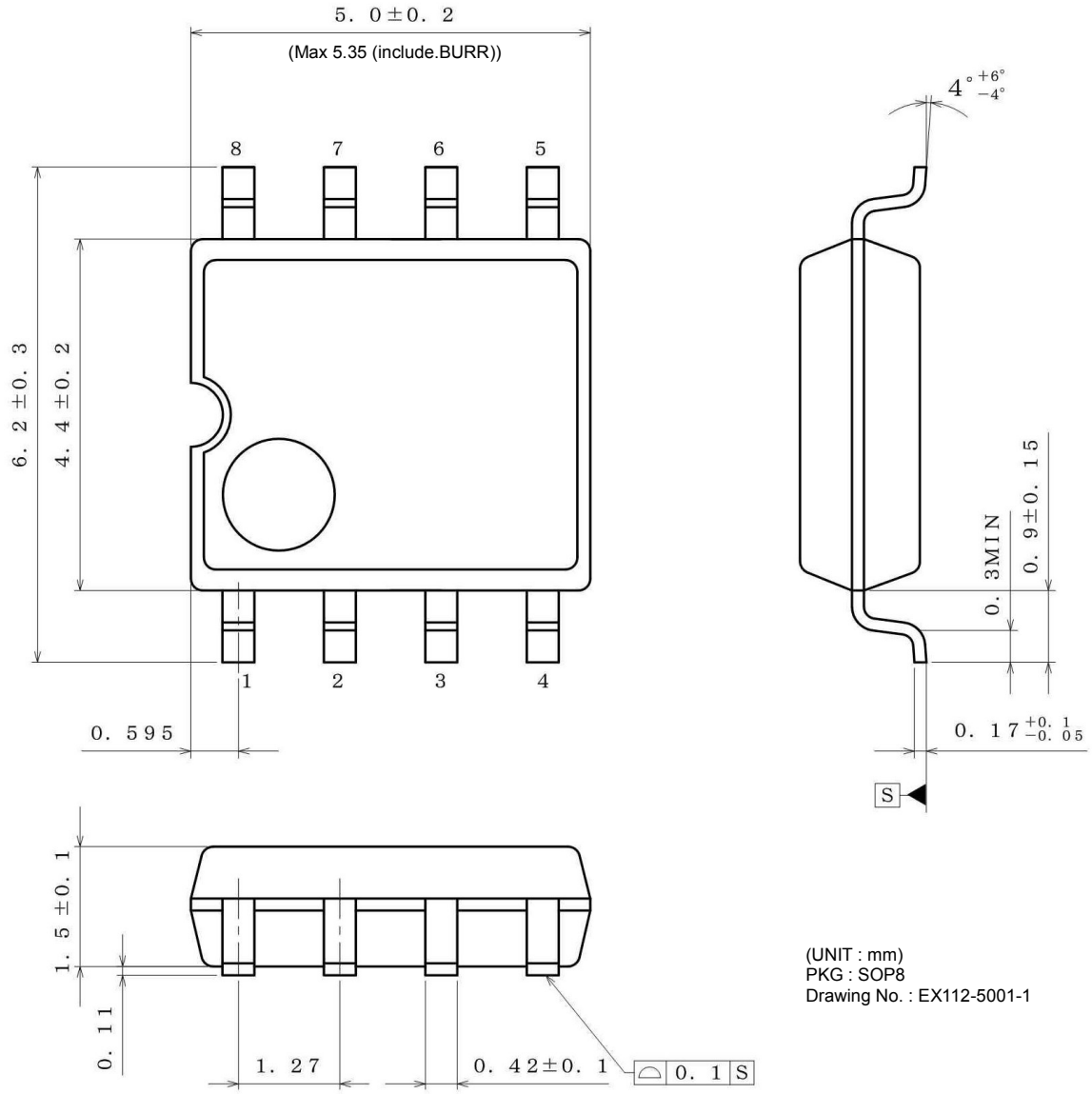
Physical Dimension, Tape and Reel Information

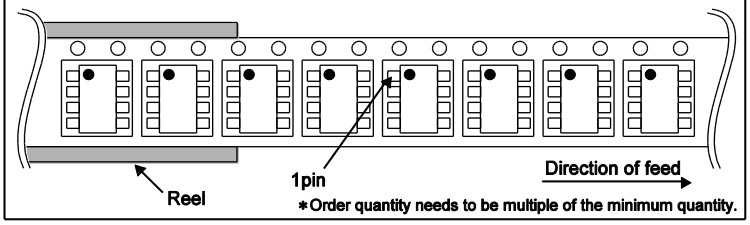
Package Name	SOP8



(UNIT : mm)
PKG : SOP8
Drawing No. : EX112-5001-1

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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Revision History

Date	Revision	Changes
2.Mar.2016	001	Data Sheet Revision1 Release.
20.Apr. 2016	002	Modification: P4, P5 VOUT->VCC
20.Apr. 2016	002	Modification: P6, 74.2mm2->74.2mm x 74.2mm
20.Apr. 2016	002	Modification: P15, Fig17 graph.
18.Oct. 2016	003	Data Sheet Revision3 Release
18.Oct. 2016	003	Modification: P1, BM1R00xxxF->BM1R00146F, BM1R00147F, BM1R00148F, BM1R00149F,BM1R00150F
18.Oct. 2016	003	Modification: P1, P20, Lineup Table
18.Oct. 2016	003	Modification: P1, BM1R00xxxF->BM1R00146F-150F
18.Oct. 2016	003	Delete: P1, P5, ultra-
18.Oct. 2016	003	Delete: P3, Comment in Block Diagram
18.Oct. 2016	003	Delete: P4, Description of Block ”Compulsion ON Time”
18.Oct. 2016	003	Delete: P4, BM1R00026F
18.Oct. 2016	003	Delete: P7, Electrical Characteristics “Compulsion ON Time”
18.Oct. 2016	003	Modification: P7, ”%” -> ”μs”
18.Oct. 2016	003	Modification: P8, “LATCH Timer” -> “Protection Timer”
18.Oct. 2016	003	Modification: P8, “SH_OUT Sink Current at LATCH Mode” -> “SH_OUT Sink Current at Protection Mode”
18.Oct. 2016	003	Delete: P19, Comment of “15.Thermal Shutdown Circuit(TSD)”

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

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