Wireless Power Consortium Qi Compliant
AirFuel Alliance PMA Compliant

Wireless Power Receiver IC

BD57015GWL

General Description

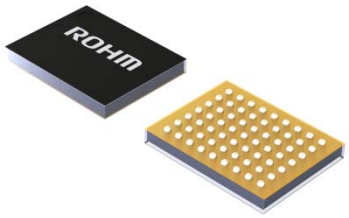
BD57015GWL is a stand-alone wireless power receiver IC. The device integrates a fully synchronous rectifier circuit with low-impedance FETs, Qi compliant and PMA compliant packet controller, adjustable regulated voltage output, and an open-drain output terminal to communicate with the power transmitter using amplitude modulation.
BD57015GWL is targeted at mobile applications implementing wireless charging compliant to Qi Extended Power Profile (EPP) standard and the PMA standard.

Key Specification

- 7 Programmable Output Voltages 5.0 to 12.0 V
- Maximum Input Voltage 20 V (Max)
- Maximum Input/ Output Current 1.5 A (Max)
- AC Input Frequency Range 100 to 480 kHz

Package

UCSP50L4C W(Typ) D(Typ) H(Max)
4.1mm × 3.2mm × 0.57mm
(0.4mm pitch)



Features

- Low Impedance FET rectifier
- High efficiency fully synchronous rectifier
- Maximum Input Voltage of 20V
- Supports Qi standard ver1.2, PMA standard SR1
- Automatic Detection of Qi / PMA, or selection by external pin
- Open-Drain output terminal for modulation
- TX-RX coil Position Gap alarm

Applications

Qi and/or PMA Compliant Devices
- Smart Phones
- Cell Phones
- Hand-held Mobile Devices

Typical Application Circuit

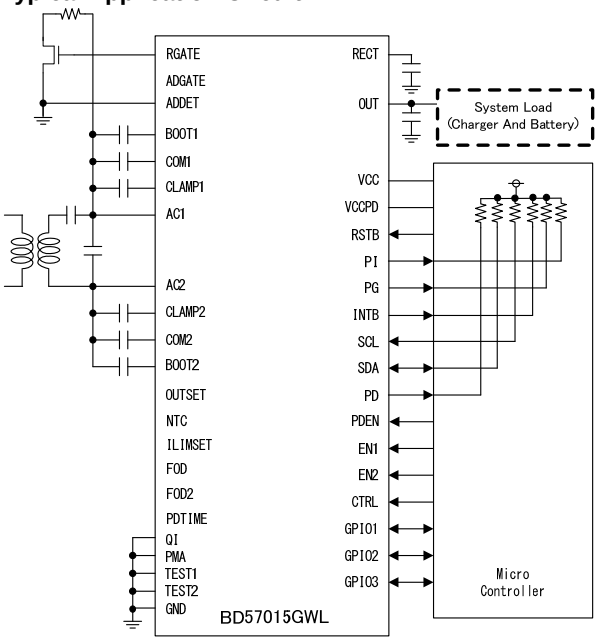


Figure 1. Typical Application Circuit

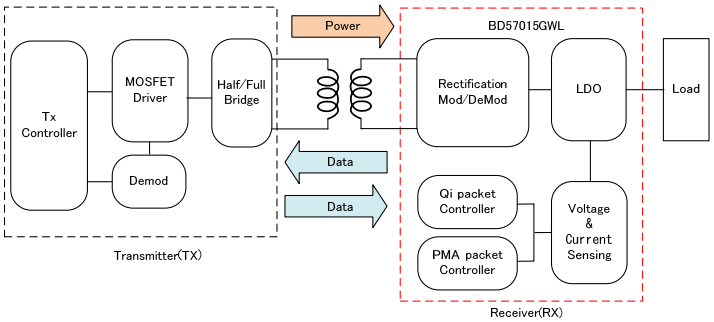


Figure 2. Wireless Power Transfer System

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays

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Absolute Maximum Ratings

Parameter	Symbol	Limit	Unit
RECT,OUT, AC1,AC2,COM1, COM2,CLAMP1,CLAMP2 Voltage	VINOUT_H1	-0.3 to +20	V
BOOT1,BOOT2 Voltage	VINOUT_H2	-0.3 to +26	V
BOOT1-AC1, BOOT2-AC2 Voltage	VBOOT_AC	-0.3 to +7.0	V
PG, PI, INTB, SDA,SCL,TEST1,TEST2,EN1,EN2, PMA,QI,CTRL,RGATE,PD, PDEN Voltage	VINOUT_L1	-0.3 to +7.0	V
VCC,REG25,GPIO1-3,FOD,FOD2 OUTSET,NTC,ILIMSET,RSTB, PDTIME,VCCPD Voltage	VINOUT_L2	-0.3 to +4.5	V
ADDET, ADGATE Voltage	VAD_H1	-0.3 to +28	V
Input/ Output Rating Current	IMAX	1.5(Note 1)	A
PG, PI, INTB pin rated Current	IMAX_PG	15	mA
Power Dissipation	Pd	1.64(Note 2)	W
Operation Temperature Range	Ta	-30 to +85	°C
Storage Temperature Range	Tstg	-55 to +150	°C

(Note 1) Applies to AC1, AC2, RECT, GND terminals when all of them are connected to a common pattern on the PCB.
(Note 2) If mounted on a standard ROHM PCB (PCB size: 54mm x 62mm x 1.6mm), reduce by 13.12mW/°C (Ta ≥25°C).
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum rating

Recommended Operating Range

Parameter	Symbol	Range	Unit
Rectified Voltage Range	VRECT	0 to 17.4	V
AC1,AC2 Input Peak Voltage Range	VAC1,VAC2	17.4	V
ADDET Input Voltage	VADDET	15.0	V
OUT Terminal Voltage	VOUT	5.0 to 12.0(Note 3)	V
VCC Voltage Range	VCC	2.5 to 3.0	V
VCCPD Voltage Range	VCCPD	2.5 to 3.0	V
Capacitance between RECT-GND	CRECT	Min 20	μF

(Note 3) Supported VOUT is up to 10V.

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Electrical Characteristics (Unless otherwise specified, Ta = 25 °C, VRECT = 5.0V, VCC = 2.65V)

Parameter	Symbol	Compliant Value			Unit	Conditions
		Min	Typ	Max		
General						
Operating Circuit Current 1	I_{RECT1}	-	44	50	mA	VRECT=5.0V, OUT off.
Operating Circuit Current 2	I_{RECT2}	-	27	35	mA	VRECT=5.0V, OUT on
OUT Terminal Quiescent Current (wireless charging is disabled)	I_{OUT}	-	50	100	μA	VOUT=5.0V, RECT=0V ADDET=OPEN
Protection circuit						
RECT Under Voltage Lockout	V_{RECTUV}	2.5	2.6	2.7	V	VRECT:0V → 5V
RECT Under Voltage Lockout Hysteresis	$V_{RECTUVHYS}$	150	300	450	mV	VRECT:5V → 0V
RECT Over Voltage Protection Detection Voltage	V_{RECTOV}	15.6	16.5	17.4	V	VRECT:10V → 20V
RECT Over Voltage Protection Hysteresis	$V_{RECTOVHYS}$	75	150	300	mV	VRECT:20V → 10V
LDO Block						
OUT Terminal Output Voltage 1	$V_{OUTLDO1}$	6.86	7.00	7.14	V	I load=100mA,VOUT=7.0V setting, VRECT=7.5V
OUT Terminal Output Voltage Accuracy	$RATE_{OUT}$	-3	0	+3	%	VOUT=5V,5.3V,8V,9V,10V, 12V
OUT Terminal Load Regulation	dV_{OUT}	-	-	200	mV	Iload=0-500mA VRECT=7.2V VOUT=7V
Maximum Output Current	$I_{LOADmax}$	-	-	1.5	A	
PADDET Block						
PDTIME Input Off Leak Current	$I_{LEAKPDTIME}$	-	-	2.0	μA	VCCPD=2.65V, AC2=Open, PDTIME=2.65V
PDTIME Detection Voltage	V_{PDDET}	0.4	0.7	1.0	V	
PD Output L Level	V_{PDVOL}	-	0.1	0.2	V	Isink=1mA
PD Pin Leak Current	I_{LEAKPD}	-	-	2.0	μA	VPD=2.65V, AC2=Open, PDTIME=0V, PD=7V
COM Block						
COM1, COM2 ON Resistance	RON_{COM}	-	1.5	3.0	Ω	
COM1, COM2 Pin Leak Current	$ILEAK_{COM}$	-	-	2	μA	VCOM1,2=20V
RGATE Block						
RGATE Pin Output H Level	VH_{RGATE}	4.3	4.8	5.3	V	I_{SOURCE}=-1mA, VRECT=7V
RGATE Pin Output L Level	VL_{RGATE}	-	0.1	0.5	V	I_{SINK}=1mA
CLAMP Block						
CLAMP1, CLAMP2 ON Resistance	RON_{CLAMP}	-	2.5	5.0	Ω	
CLAMP1,CLAMP 2 Pin Leak Current	$ILEAK_{CLAMP}$	-	-	2	μA	VCLAMP1,2=20V

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Electrical Characteristics (Unless otherwise specified, Ta = 25 °C, VRECT = 5.0V, VCC = 2.65V)

Parameter	Symbol	Compliant Value			Unit	Conditions
		Min	Typ	Max		
Adapter Detection Block						
Adapter Input Detection Threshold Voltage	VADDET	3.4	3.6	3.8	V	Vaddet:0 → 5V
Adapter Input Detection Hysteresis Voltage	VHYS_AD	200	400	600	mV	Vaddet:5 → 0V
Adapter Input Overvoltage Detection Voltage	VADDET_OV	14.0	14.5	15.0	V	Vaddet:13 → 16V
Adapter Input Overvoltage Detection Hysteresis Voltage	VHYS_AD_OV	500	720	940	mV	Vaddet:16 → 13V
ADDET Pin Input Current	IADGATE	-	150	300	μA	VADDET=5V, OUT=OPEN
ADGATE Pin Output L Level	VL_{ADGATE}	-	0.12	0.25	V	Isink=1mA
PMA, QI, EN1, EN2, CTRL, PDEN Pin						
PMA,QI,EN1,EN2,CTRL Pin L Level Input Voltage	VIL_{mode}	-	-	0.4	V	
PMA,QI,EN1,EN2,CTRL Pin H Level Input Voltage	VIH_{mode}	1.3	-	-	V	
PMA,QI,EN1,EN2,CTRL Pin Pull Down	RI_{mode}	-	200	-	kΩ	
PDEN Pin L Level Input Voltage	VIL_{PDEN}	-	-	0.4	V	
PDEN Pin H Level Input Voltage	VIH_{PDEN}	1.3	-	-	V	
RSTB Pin						
RSTB Pin L Level Input Voltage	VIL_{RSTB}	-	-	0.6	V	VCC=2.65V
RSTB Pin Pull Up Resistance	RI_{RSTB}	-	100	-	kΩ	
RSTB Pin L Level Output Voltage	VL_{RSTB}	-	0.15	0.30	V	Isink=1 mA
PG,PI Pin						
PG,PI Pin Output L Level	VL_{PG}	-	0.25	0.5	V	Isink=5mA
PG, PI Pin Leak Current	$ILEAK_{PG}$	-	-	2	μA	VPG=7V
INTB Pin						
INTB Pin Output L Level	VL_{INT}	-	0.25	0.5	V	Isink=5mA
INTB Leak Current	$ILEAK_{INT}$	-	-	2	μA	VINTB=7V

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Electrical Characteristics (Unless otherwise specified, Ta = 25 °C, VRECT = 5.0V, VCC = 2.65V)

Parameter	Symbol	Compliant Value			Unit	Conditions
		Min	Typ	Max		
GPIO Pin						
GPIO Pin L Level Input Voltage	VIL_{GPIO}	-	-	VCC×0.3	V	
GPIO Pin H Level Input Voltage	VIH_{GPIO}	VCC×0.7	-	-	V	
GPIO Pull Down Resistance	PD_{GPIO}	-	100	-	kΩ	
GPIO Pull Up Resistance	PU_{GPIO}	-	100	-	kΩ	
L Level Output Voltage	VOL_{GPIO}	-	-	VCC×0.2	V	Isink=1mA
H Level Output Voltage	VOH_{GPIO}	VCC×0.8	-	-	V	Isource=-1mA
Serial Interface						
SCL, SDA Pin L Level Input Voltage	VIL_{SCL} VIL_{SDA}	-	-	0.4	V	
SCL, SDA Pin H Level Input Voltage	VIH_{SCL} VIH_{SDA}	1.3	-	-	V	
SCL, SDA Pin L Level Input Current	IIL_{SCL} IIL_{SDA}	-1	-	-	μA	VSCL=VSDA=0V
SCL, SDA Pin H Level Input Current	IIH_{SCL} IIH_{SDA}	-	-	1	μA	VSCL=VSDA=2.65 V
SDA Pin L Level Output Voltage	VOL_{SDA}	-	-	0.4	V	Isink=2.5 mA

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Pin Configuration (Bottom View)

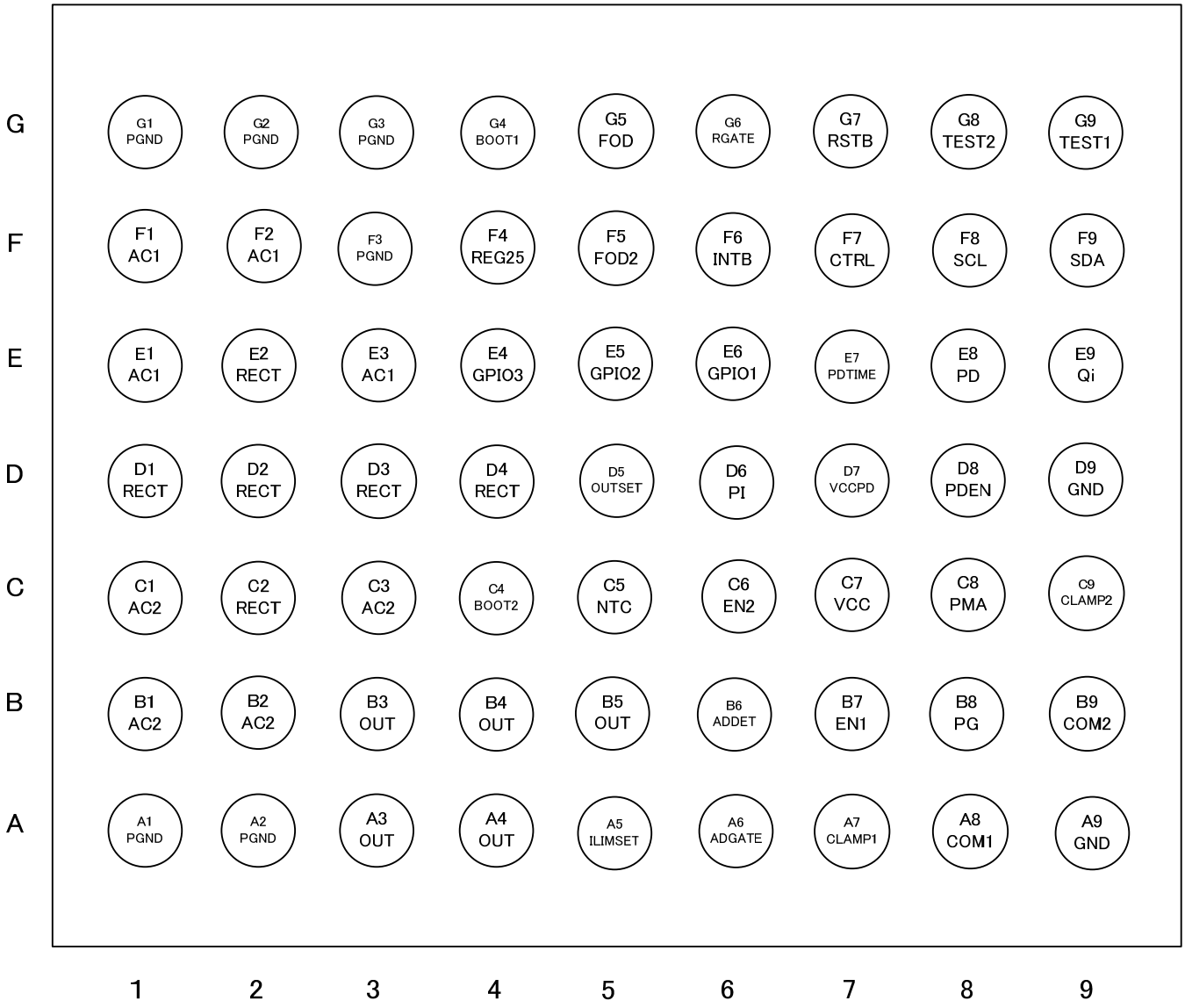

Figure 3. Pin Configuration

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Pin Description

Pin No.	Pin Name	I/O	Function
E1,F1,F2,E3(NOTE1)	AC1	Out	AC input pin 1
B1,B2,C1,C3(NOTE1)	AC2	Out	AC input pin 2
G4	BOOT1	Out	Bootstrap capacitor connection pin 1 for the internal FET driver
C4	BOOT2	Out	Bootstrap capacitor connection pin 2 for the internal FET driver
A3,A4,B3,B4, B5(NOTE1)	OUT	Out	LDO Output pin
C2,D1,D2,D3,E2, D4(NOTE1)	RECT	Out	Rectifier Output pin
D5	OUTSET	Input	Resistance Connection pin for the Output Voltage setting
G6	RGATE	Output	Output Control pin for PMA setting If only Qi mode is used, leave the pin OPEN.
A7	CLAMP1	Input	AC1 Clamp protection pin
A8	COM1	Output	Output Control pin 1
B9	COM2	Output	Output Control pin 2
C9	CLAMP2	Input	AC2 Clamp protection pin
C5	NTC	Input	Resistance Connection pin for the thermal Detection setting(NOTE3)
F5	FOD2	Input	Resistance Connection pin 2 for the Foreign Object Detection Adjustment setting If only PMA mode is used, leave the pin OPEN.
G5	FOD	Input	Resistance Connection pin 1 for the Foreign Object Detection Adjustment setting If only PMA mode is used, leave the pin OPEN.
A5	ILIMSET	Input	Resistance Connection pin for the Current Limit setting
D6	PI	Output	Qi BPP(Baseline Power Profile) / EPP(Extended Power Profile) identification pin
D8	PDEN	Input	PAD Detection Enable pin(NOTE2)
E7	PDTIME	Input	PAD Detection Time setting pin(NOTE2)
E8	PD	Output	PAD Detection Output pin
A6	ADGATE	Output	External Adaptor Path Gate Driver pin
B6	ADDET	Input	External Adaptor Voltage Detection pin(NOTE2)
B7	EN1	Input	Enable pin 1 for Wired or Wireless Charging
C6	EN2	Input	Enable pin 2 for Wired or Wireless Charging
B8	PG	Output	Open Drain Output pin to notify if LDO Output is ON
G7	RSTB	Input/Output	System Reset Input and Output pin(NOTE3)
F6	INTB	Output	Interrupt Output pin
F7	CTRL	Input	Control pin for Wireless Charging
G9	TEST1	Input	Test pin 1 (Usually these pins are connected to GND.)
G8	TEST2	Input	Test pin 2 (Usually these pins are connected to GND.)
F8	SCL	Input	Serial Interface Clock Input pin(NOTE2)
F9	SDA	Input/Output	Serial Interface Data Input/Output pin(NOTE2)
E6	GPIO1	Input/Output	GPIO 1 pin(NOTE4)
E5	GPIO2	Input/Output	GPIO 2 pin(NOTE4)
E4	GPIO3	Input/Output	GPIO 3 pin(NOTE4)
C8	PMA	Input	PMA setting pin
E9	Qi	Input	Qi setting pin
D7	VCCPD	Power	Power Supply for Pad Detection pin(NOTE2)
C7	VCC	Power	External Power Supply Application pin for LOGIC Block(NOTE4)
F4	REG25	Output	2.5V Internal Voltage pin
A9,D9(NOTE1)	GND	Ground	Ground pin
A1,A2,F3,G1,G2, G3(NOTE1)	PGND	Ground	Power Ground pin

(NOTE1) If one function pin have several pin numbers, please connect same function pins to a common board node.
(NOTE2) When the pin is unused, please connect the pin to GND.
(NOTE3) When the pin is unused, please leave the pin OPEN.
(NOTE4) When the pin is unused, please connect the pin to GND or leave the pin OPEN.

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Block Diagram

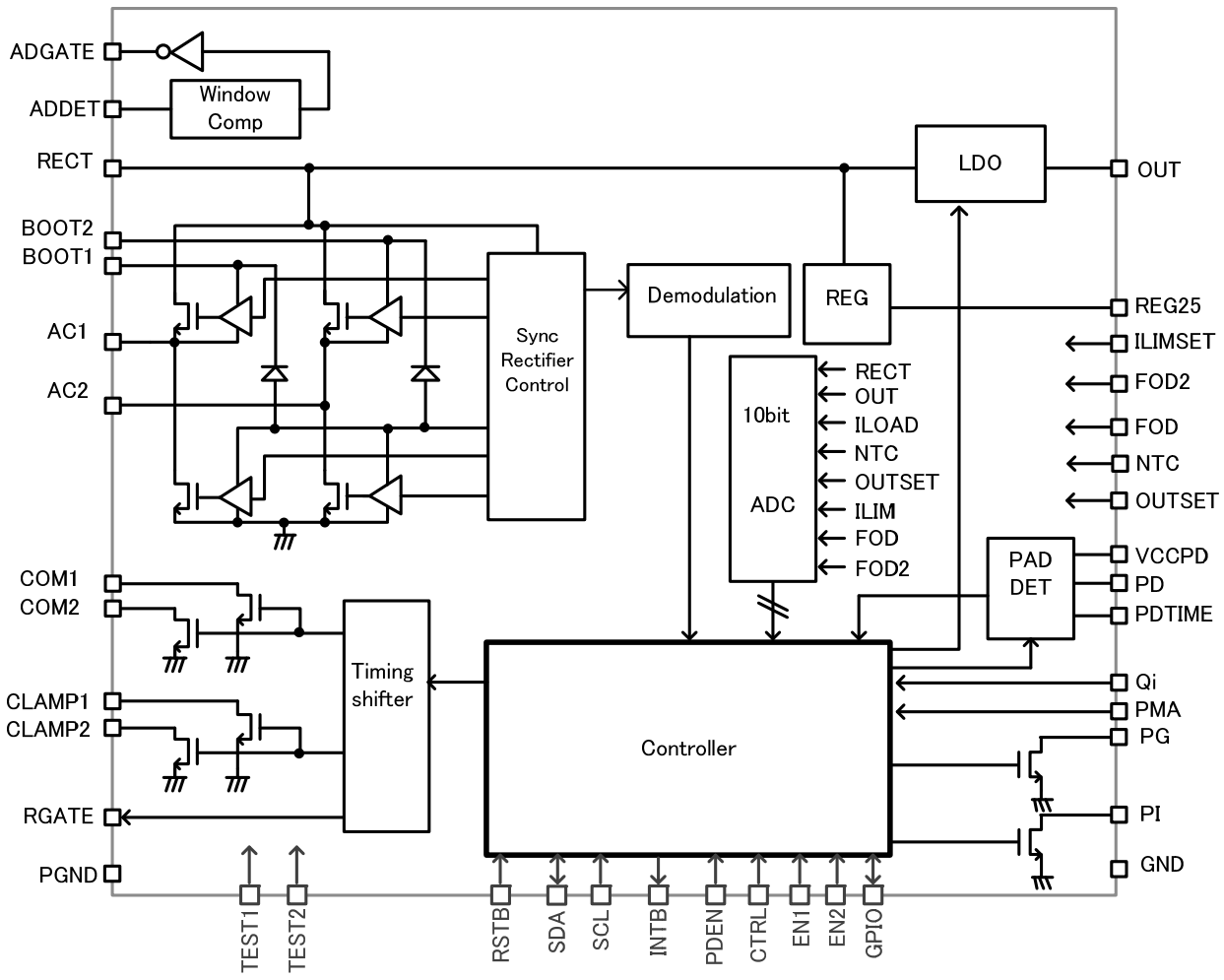

Figure 4. Block Diagram

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Description of operation

1. Qi/PMA operation mode selection

The BD57015GWL is compliant with both Qi and PMA standards. Qi/PMA operation mode can be detected automatically by the internal circuit or set by external terminal. The automatic detection depends on the carrier frequency from TX during Digital Ping. The operation mode is shown as follow:

PMA pin	QI pin	Operation Mode
L	L	Automatic detection based on the internal circuit
L	H	Qi mode only (It won't operate in other modes)
H	L	PMA mode only (It won't operate in other modes)
H	H	Reserved (Do not use this setting)

If H is needed connect these pins to the REG25 pin using a pullup resistance.
When the Automatic detection of operation mode is selected, the active operation mode can be reported using the Mode Status Register (0x8D).

Mode Status register (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial Value	R/W
MODE STATUS	0x8D	[7] Reserved [6] PMA_MODE PMA mode detection 0x0: Undetected 0x1: Operating in PMA mode [5] QI_MODE Qi mode detection 0x0: Undetected 0x1: Operating in Qi mode [4:0] Reserved	0x00	R

Reserved bits read an undefined value.

The charge start detection interrupt can be used as an indicator for when to check this register. Refer to section "*16.Interrupt Control Block"* for the details on the charge start detection interrupt.

2. Qi Controller block

If Qi mode is detected as the operation mode of BD57015GWL, it will proceed to following the Qi compliant Ping phase. In this phase, it will send the Signal Strength value which indicates the degree of coupling between the RX and TX. Then BD57015GWL will proceed to the Identification & Configuration phase and send the ID information and the necessary information about RX to the TX. When BD57015GWL is in EPP mode, (set by Qi Power Mode setting register (0x0E)), it sends the information of the configuration and requests a transition to the Negotiation phase. If TX responses the ACK message, it will proceed to the Negotiation phase.
If this negotiation succeeds, it will move to the Calibration phase and the Power Transfer phase at EPP. If this negotiation fails, or the TX does not respond, or BPP mode is set by register, it will move to the Power Transfer phase at BPP.
The power transfer mode can be checked by the PI pin. If PI pin is L, it is in EPP mode, and if it is H, it means that it is charging in BPP mode. The power mode can be also confirmed by checking the Qi Monitor Mode register (0x0F).

Qi Power Mode setting register (Only for Qi)

Register Name	Address	Bit[7:0]	Initial Value	R/W
EPP_MODE	0x0E	[7:0] EPP_MODE_SET EPP Mode setting 0x10 : BPP Mode only 0x01 : EPP Mode (During PI=L, this must be selected) 0x11 : EPP Mode (During PI=H, this must be selected) Other : Reserved	0x10	R/W

Please don't set Reserved value.

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Qi Monitor Mode register (Only for Qi)

Register Name	Address	Bit[7:0]	Initial Value	R/W
MONI_MODE	0x0F	[7:1] Reserved [0] EPP_MODE Classification of the operation mode 0x0 : Operation in BPP Mode 0x1 : Operation in EPP Mode	0x00	R

Reserved bits read “0”

In the Power Transfer Phase, the previously specified output voltage is output at the OUT pin and the device is ready to start charging. The charging will be stopped when setting the EN1 pin to “H” which then sends the End Power Transfer packet (Charging Complete, EPT) to the TX. The following are the supporting messages regarding EPT packet. The EPT value can be checked in the Qi EPT Code Register (0x1C) when EPT is sent.

End Power Transfer Packet			
Value	**Reason**	**Support**	**Condition**
0x00	Unknown	Send	Adapter Input detection
0x01	Charge Complete	Send	Charge Complete (EN1=H Detection)
0x02	Internal Fault	Send	Internal Temperature error, ILIMSET pin setting error, OUTSET pin setting error, FOD pin setting error, FOD2 pin setting error.
0x03	Over Temperature	Send	External Temperature Error (CTRL=H Detection, Detection for using the information from NTC pin)
0x04	Over Voltage	Not Sent	-
0x05	Over Current	Not Sent	-
0x06	Battery Failure	Not Sent	-
0x07	Reserved	Not Sent	-
0x08	No Response	Send	No convergence to desired point for RECT voltage
0x09	Reserved	Not Sent	-
0x0A	Negotiation Failure	Send	Negotiation can’t be done normally
0x0B	Restart Power Transfer	Not Sent	-

When sending this packet, an interrupt can be generated for the external microcontroller.

Qi EPT Code register (Only for Qi)

Register Name	Address	Bit[7:0]	Initial Value	R/W
EPT_CODE	0x1C	[7:0] EPT_CODE EPT value (code) When the status is not EPT, this register is 0xFF.	0xFF	R

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3. PMA Controller block

When the operation of BD57015GWL is set to PMA mode, BD57015GWL will proceed to the digital Ping phase of PMA. In this phase, BD57015GWL will send the ACK message to the TX and signal that a device based on PMA exists. Next, BD57015GWL proceeds to the Identification phase and sends information to the TX. TX will check the ID Information and if it is correct, it will proceed to the Power Transfer phase. However if it is incorrect, it will go back to the Digital Ping phase. In the Power Transfer phase, an output voltage is produced in the OUT pin and charging can start. The charging can be stopped when setting the EN1 pin to “H” which then sends an EOC signal to the TX. When the charging stops, it can also generate an interrupt signal. The reason for charging stop is stored in the PMA EOC Code register (0x1D. Other conditions that produce an End of Charge (EOC) signal are described below.

PMA EOC Code register (Only for PMA)

Register Name	Address	Bit[7:0]	Initial Value	R/W
EOC_WR	0x1D	[7:0] EOC_CODE Cause of the output EOC. (”1” indicates “Detection”) [7] : During NTC detection [6] : No Load Detection (continuous for more than 42 seconds)NOTE 1 [5] : Full Charge Detection (Low Current Detection for long hours)NOTE 1 [4] : UVLO Detection of Output [3] : External Temperature Error (CTRL=H Detection) 150 degrees [2] : Internal Temperature Error or ILIMSET pin setting Error or OUTSET pin setting Error [1] : Charge Complete (EN1=H Detection) [0] : Adapter Input Detection	0x00	R

(NOTE1) These functions are cleared when the device is reset. This setting shall remain in effect with the following registers (EOC MASK:0x86)

PMA EOC Mask register (Only for PMA)

Register Name	Address	Bit[7:0]	Initial Value	R/W
EOC_MASK	0x86	[7:4] Reserved [3] MASK _NO LOAD EOC output for the No Load Detection Disable (0x0 : Enable 0x1 : Disable) [2] MASK _FULL EOC output for the Full Charge Detection Disable (0x0 : Enable 0x1 : Disable) [1:0] Reserved	0x0C	R/W

Please set an initial value into Reserved bits.

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Description of Operation for Common Blocks

4. Rectifier block

By inputting AC signal into both ends of a primary side (TX) coil, a voltage is generated by electromagnetic induction in the secondary side coil. Full-wave rectification is performed after detection of output current from the secondary coil as mentioned above, and using the built-in FET connected to AC1 and AC2 pins. The current detection is done by comparing the AC pin voltage (FET Ron × Icoil) with GND level. The on/off signal of built-in FET will be generating based on this detection signal. The on/off timing of L side FET and H side FET are monitored to prevent a shoot through current. The bootstrap drive system for the Nch FET on H side and L side is used for high efficiency. Therefore, a capacitor is needed between BOOT1 (BOOT2) pin and AC1 (AC2) pin.

5. Low Drop Out (LDO) Block

The OUT pin output voltage can be set through the OUTSET pin or through a register, please refer to section "*13. OUTSET setting*" for details. The current limit value of the OUT pin can be set through the ILIMSET pin or through a register as explained in section "*9. ILIM setting*".

6. A/D Converter Block

When making a packet, every analog signal that is needed for calculation will be converted to digital value. The A/D converter uses the 10bit sequential comparison (SAR) architecture. This conversion cannot be controlled from outside.

7. External control input (CTRL, EN1 and EN2).

When CTRL = H, during an external temperature error, the wireless power transfer will stop after an EPT or EOC output.
Charging from wireless supply or wired (adapter) supply can be enabled or disabled using EN1 and EN2.
In the default condition (EN1=L and EN2=L), both wireless power supply and adapter control are active. When both sources are available, priority is given to the adapter (wired power), wireless power is stopped according to the sequence explained in adapter detection block, and the electrical connection of the path from an adapter is active.
When EN1 becomes H, the Qi mode will produce an End Power Transfer (0x01: Charge Complete) packet and the PMA mode will produce an End of Charge (EOC) packet and wireless power supply will be stopped.

CTRL	Operation
L	Will maintain the normal feed condition.
H	During external temperature error, the wireless power transfer will stop because of an EPT or EOC output.

EN1	EN2	Operation
L	L	Both the wireless power charging and external adapter control are enabled. Priority is given to the external adapter. That is, if a sufficient adapter input is detected during wireless power charging, wireless power will immediately stop and only an adapter charging will continue.
L	H	Both the wireless power charging and external adapter control are enabled. Priority is given to the external adapter. That is, if a sufficient adapter input is detected during wireless power charging, wireless power will immediately stop and only an adapter charging will continue.
H	L	Wireless power charging is disabled. Wired power charging is enable.
H	H	Both an adapter and wireless power charging are disabled. That is, in this mode, power cannot be supplied from OUT.

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8. Adapter detection block

If the ADDET pin detects more than 3.6V (Typ), ADGATE will output LOW and turn ON the PMOS switch of the adapter line. Since priority is given to adapter (cable), wireless power supply will be stopped (EPT / EOC output), and then the OUT output will be stopped. After that, the voltage at OUT will be checked and if it is less than 0.7V and the adapter line of PMOS switch will be turned ON (ADGATE: H to L).
The sequence of operation during adapter detection is as follows.

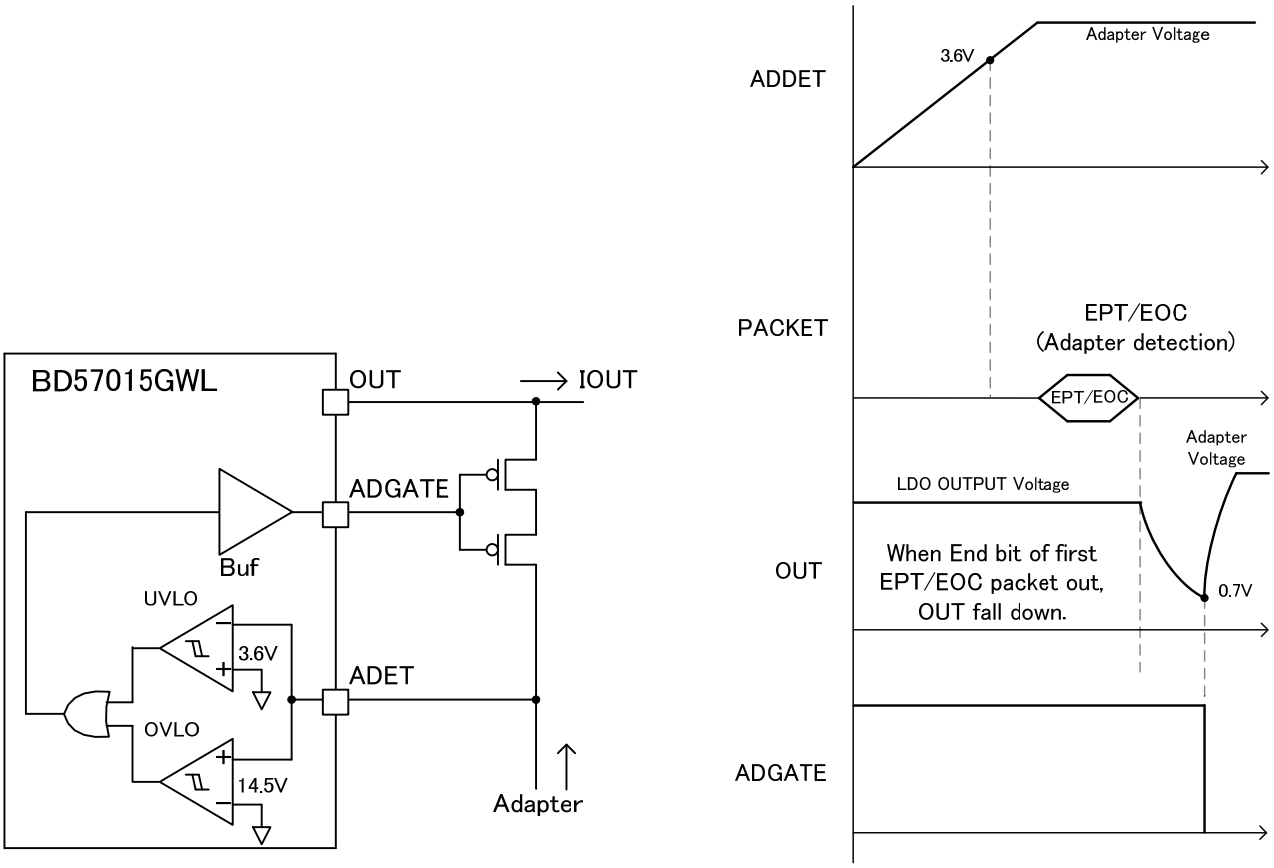

Figure 5. Adapter Detection

If the ADDET voltage is more than the threshold of OVP, the PMOS will be switched off regardless of the wireless power supply.

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9. ILIM setting

The current limit of the OUT pin can be set by the resistance connected to the ILIMSET pin or the register shown below. The following formula shows the relation between setting resistance and limit current (ILIM).

Current Limit ILIM [mA]	RILIMSET [kΩ]
ILIMSET register setting	OPEN
500	120
700	75
900	56
1000	43
1100	36
1200	30
1300	24
1500	20
EPT or NoCh	SHORT

The resistance should have accuracy of ±1%.

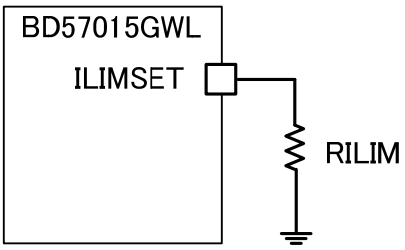

Figure 6. ILIMSET setting

If ILIMSET pin is shorted to GND, there will be a setting error and BD57015GWL will send EPT (internal fault) in Qi mode..And BD57015GWL will send NoCh signal repeatedly, then the charging will not be started in PMA mode.
When the ILIMSET pin is OPEN or the bit [7] of the following register is set to “1”, the Output Current Limit value (of ILIM) can be set depending on the following register (0x0A). If the bit [7] of this register is set to “1”, the register setting has priority regardless of the resistance connected to the ILIMSET pin. Furthermore, the state related to the ILIMSET pin can be confirmed by the ILIM_STATE register (0x0B).

ILIMSET setting register (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial Value	R/W
ILIM_SET	0x0A	[7] ILIM_REG_EN 0x0 : If ILIMSET pin is not OPEN, the setting of this register (bit[5:0]) is invalid. 0x1 : The setting of this register (bit[5:0]) is valid forcibly. [6] Reserved [5:0] ILIM_SET_VAL OUT Pin Current Limit Level setting 0x5 : 0.5A 0x10 : 1.05A 0x6 : 0.55A 0x11 : 1.1A 0x7 : 0.6A 0x12 : 1.15A 0x8 : 0.65A 0x13 : 1.2A 0x9 : 0.7A 0x14 : 1.25A 0xA : 0.75A 0x15 : 1.3A 0xB : 0.8A 0x16 : 1.35A 0xC : 0.85A 0x17 : 1.4A 0xD : 0.9A 0x18 : 1.45A 0xE : 0.95A 0x19 : 1.5A 0xF : 1.0A Other : Reserved	0x0F	R/W
ILIM_STATE	0x0B	[7] ILIM_SHORT_DET Short detection of ILIMSET pin. 0x0 : not short 0x1 : short [6:4] ILIM_ADC_VAL Current limit value set based on the read value in A/D. If the read value in A/D is outside the setting range, it is 0x0. 0x0 : 500mA 0x4 : 1100mA 0x1 : 700mA 0x5 : 1200mA 0x2 : 900mA 0x6 : 1300mA 0x3 : 1000mA 0x7 : 1500mA [3] ILIM_OPEN_DET Enable/Disable of the register setting. 0x0 : Disable 0x1 : Enable (make ILIMSET pin OPEN to enable this) [2:0] : Reserved	0x00	R

Please set an initial value into Reserved bits.

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10. FOD setting (Qi mode only)

To implement FOD (Foreign Object Detection) function in Qi mode, it is required to compute the received power and to compare it with the transmitted power from the TX side. Fine power adjustment to adjust for other power losses (e.g. LC loss) outside the IC is performed by using the resistance connected to the FOD and FOD2 pin or the register shown below. The relation of the received power (PRP) supply and each parameter is shown on the formula below.

$$P_{PR} = \alpha \times f(RECT, IOUT) + \beta[W]$$
$$\alpha = FOD2$$
$$\beta = FOD[W]$$

FOD Value [mW]	RFOD[kΩ]
FOD1_SET register setting	OPEN or 820
-64	300
-32	180
32	130
64	100
96	82
128	68
160	56
192	47
224	39
256	33
288	27
320	24
352	22
384	20
EPT or NoCh	SHORT

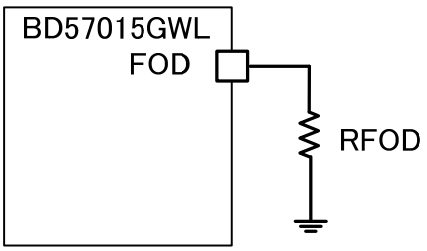

Figure 7. FOD setting

The resistance should have accuracy of ±1%.

If FOD pin is shorted to GND, there will be a setting error and BD57015GWL will send EPT (Internal Fault) in Qi mode. And BD57015GWL will send NoCh signal repeatedly, then the charging will not be started in PMA mode.

FOD2 Value [-]	RFOD2[kΩ]
FOD2_SET register setting	OPEN or 820
1.054	300
1.062	180
1.070	130
1.078	100
1.086	82
1.094	68
1.102	56
1.110	47
1.118	39
1.126	33
1.134	27
1.142	24
1.150	22
1.158	20
EPT or NoCh	SHORT

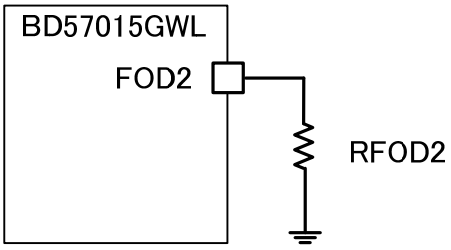

Figure 8. FOD2 setting

The resistance should have accuracy of ±1%.

If FOD2 pin is shorted to GND, there will be a setting error and BD57015GWL will send EPT (Internal Fault) in Qi mode. And BD57015GWL will send NoCh signal repeatedly, then the charging will not be started in PMA mode.

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In the formula shown above, α is the inclination adjustment. β is the offset adjustment. Function f(RECT, IOUT) is proportional to the received power and calculated in the internal IC.

When these parameters are adjusted, external physical factors have to be considered. For example, external physical factors are a materials and shape of a coil, an environments around coil, and a distance to a coil of TX.

It is possible to set the FOD and FOD2 parameters in the registers (0x01, 0x03) by leaving FOD and FOD2 pins OPEN or setting the bit [7] of these registers (0x01, 0x03) to “1”. If bit [7] of these registers is set to “1”, the setting of the registers have priority regardless of the resistance connected to the FOD and FOD2 pin.

In addition, the related states in FOD and FOD2 can be confirmed on the next registers (0x02, 0x04).

FOD1 register (Only for Qi)

Register Name	Address	Bit[7:0]	Initial Value	R/W
FOD1_SET	0x01	[7] FOD1_REG_EN 0x0 : If FOD pin is not OPEN, the resistance has priority. 0x1 : The setting of this register (bit[4:0]) has priority. [6] FOD1_POLARITY Set the polarity 0x0 : Plus mode (Add the setting value) 0x1 : Minus mode (Subtract the setting value) [5] Reserved [4:0] FOD1 Setting of the FOD value. 0x00 : 0 mW 0x01 : 32 mW 0x02 : 64 mW 0x03 : 96 mW 0x04 : 128 mW 0x05 : 160 mW 0x06 : 192 mW 0x07 : 224 mW 0x08 : 256 mW 0x09 : 288 mW 0x0A : 320 mW 0x0B : 352 mW 0x0C : 384 mW 0x0D : 416 mW 0x0E : 448 mW Other : Reserved	0x00	R/W
FOD1_STATE	0x02	[7] FOD1_SHORT_DET Short detection of FOD pin. 0x0 : not short 0x1 : short [6:3] FOD1_ADC_VAL The set value based on the read value in A/D. 0xF when the read value in A/D was detected short. 0x0 when the read value in A/D was detected open. 0x1 : -64 mW 0x2 : -32 mW 0x3 : +32 mW 0x4 : +64 mW 0x5 : +96 mW 0x6 : +128 mW 0x7 : +160 mW 0x8 : +192 mW 0x9 : +224 mW 0xA : +256 mW 0xB : +288 mW 0xC : +320 mW 0xD : +352 mW 0xE : +384 mW [2] FOD1_OPEN_DET Enable/ Disable of the register setting. 0x0 : Disable 0x1 : Enable (make FOD pin OPEN to enable this) [1:0] Reserved	0x00	R

Please set an initial value into Reserved bits.

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FOD2 register (Only for Qi)

Register Name	Address	Bit[7:0]	Initial Value	R/W
FOD2_SET	0x03	[7] FOD2_REG_EN 0x0 : If FOD2 pin is not OPEN, the setting of this register (bit[5:0]) is invalid. 0x1 : The setting of this register (bit[5:0]) is valid forcibly. [6] Reserved [5:0] FOD2 Setting of the FOD2 value. 0x01 : 1.054 times 0x08 : 1.110 times 0x02 : 1.062 times 0x09 : 1.118 times 0x03 : 1.070 times 0x0A : 1.126 times 0x04 : 1.078 times 0x0B : 1.134 times 0x05 : 1.086 times 0x0C : 1.142 times 0x06 : 1.094 times 0x0D : 1.150 times 0x07 : 1.102 times 0x0E : 1.158 times Other : Reserved	0x07	R/W
FOD2_STATE	0x04	[7] FOD2_SHORT_DET Short detection of FOD2 pin. 0x0 : not short 0x1 : short [6:3] FOD2_ADC_VAL The set value based on the read value in A/D. 0xF when the read value in A/D was detected short. 0x0 when the read value in A/D was detected open. 0x01 : 1.054 times 0x08 : 1.110 times 0x02 : 1.062 times 0x09 : 1.118 times 0x03 : 1.070 times 0x0A : 1.126 times 0x04 : 1.078 times 0x0B : 1.134 times 0x05 : 1.086 times 0x0C : 1.142 times 0x06 : 1.094 times 0x0D : 1.150 times 0x07 : 1.102 times 0x0E : 1.158 times [2] FOD2_OPEN_DET Enable/ Disable of the register setting. 0x0 : Disable 0x1 : Enable (make FOD2 pin OPEN to enable this) [1:0] Reserved	0x00	R

Please set an initial value into Reserved bits.

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Depending on the situation, fine tuning of the FOD function and additional EPP setting can be done using the following register.

Register Name	Address	Bit[7:0]	Initial Value	R/W
FOD3_H	0x05	For the fine tuning of Received Power packet value.	0x25	R/W
FOD3_L	0x06	For the fine tuning of Received Power packet value.	0x55	R/W
RCOIL_SET	0x07	For the setting of resistance of coil.	0x05	R/W
IDET_DUMP_I	0x41	For the fine tuning of dump current used for calculating Received Power packet value.	0xC0	R/W
IDET_STATE	0x4C	For the monitor of load current.	0x01	R
DUMP_T	0x4E	For the fine tuning of dump current used for calculating Received Power packet value.	0x00	R/W
T_DP_OFFSET_QI_1	0x51	For the fine tuning of target RECT voltage value.	0x00	R/W
T_DP_OFFSET_QI_2	0x52	For the fine tuning of target RECT voltage value.	0x00	R/W
T_DP_I_THRD_QI	0x55	For the fine tuning of setting with regard to target RECT voltage.	0x00	R/W
CALIB_LL_DP_SET	0x5D	For the fine tuning of target RECT voltage value in EPP mode.	0x00	R/W
ADC_RECT_H	0xC5	For the monitor of RECT voltage.	0x00	R
ADC_RECT_L	0xC6	For the monitor of RECT voltage.	0x00	R

Regarding the detail of these register, Rohm support individually. Because the necessity and the setting value of register are different by the configuration of device such as smart phones.

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11. Q value setting

In the Qi standard for EPP it is a requirement for the RX to send FOD Status packet with the information of the Q value to the TX. Then the TX can perform foreign object detection (Foreign Object Detection) . The Q value shown here is a Q value of the coil of the TX when RX is put on Test TX#MP1 as defined in the Qi standard. It is necessary to set it to the following Q value setting register (0x37, 0x3A).

Q value setting register (Only for Qi)

Register Name	Address	Bit[7:0]	Initial Value	R/W
FOD_S_PCKT_EN	0x37	[7] Reserved [6] SEL_FOD_DATA_FUSE 0 : Use the Set Q value in register 0x3A. 1 : Restricted (in EPP mode) [5:1] Reserved [0] FOD_PCKT_EN 0 : Restricted 1 : Enable the sending of the Q value packet (FOD Status packet)	0x41	R/W
FOD_S_PCKT1_1	0x3A	[7:0] FOD_PCKT_B1 Q value sent as FOD Status packet. A Q level does not have a unit. For example, in the case of Q=1, set 0x01.	0x00	R/W

Please set an initial value into Reserved bits.

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12. Position Gap detection function during start-up

The RECT voltage at start-up is monitored, and it can detect the position gap of the RX coil in reference to the XY position on the TX coil. The threshold value (Vthpos) used for position gap detection can also be set through the POSSET setting register (0x24).
When the RECT voltage is lower than Vthpos, the interrupt signal can be generated at the INTB pin. By default, this function is disabled. The Position Gap Detection setting register need to be changed to enable this function in the situation that impressed the external power supply on the VCC pin. Detection of the position gap occurs about 30ms after the RX was put on the TX, RECT waked up, and VRECTUV was released. At that time, the interrupt signal would be generated at the INTB pin.

The initial value of Vthpos is the LDO Output Voltage setting value × 40%.

Vthpos is determined using the formula below.
Vthpos = LDO output voltage setting value × set ratio in the register
(Refer to section "*13.OUTSET setting*" for LDO Output Voltage setting.)

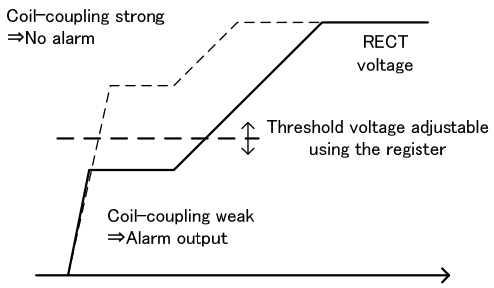

Figure 9. Detection of Position Gap

Position Setting (POSSET) register (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial Value	R/W
POS_GAP_LV_SET	0x24	[7:4] Reserved [3:0] POS_GAP_LV_SET Set the Vthpos voltage. 0x0 : LDO Output Voltage setting ×40% 0x1 : LDO Output Voltage setting ×45% 0x2 : LDO Output Voltage setting ×50% 0x3 : LDO Output Voltage setting ×55% 0x4 : LDO Output Voltage setting ×60% 0x5 : LDO Output Voltage setting ×65% 0x6 : LDO Output Voltage setting ×70% 0x7 : LDO Output Voltage setting ×75% 0x8 : LDO Output Voltage setting ×80% 0x9 : LDO Output Voltage setting ×85% 0xA : LDO Output Voltage setting ×90% 0xB : LDO Output Voltage setting ×95% 0xC : LDO Output Voltage setting ×100% 0xD : LDO Output Voltage setting ×105% 0xE : LDO Output Voltage setting ×110% 0xF : LDO Output Voltage setting ×115%	0x00	R/W

Please set an initial value into Reserved bits.

Position Gap Detection setting register (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial Value	R/W
ALIGN_DET_EN	0x21	[7:1] Reserved	0x00	R/W
		[0] ALIGN_DET_EN_WAKEUP Position Gap Detection Function Enable (during start up) 0x0 : disable 0x1 : enable		

Please set an initial value into Reserved bits.

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13. OUTPUT Voltage (OUTSET) setting

The Output voltage of the OUT pin could be set by the resistance connected to the OUTSET pin or the register setting, as shown below.

OUT Pin Output Voltage[V]	ROUTSET[kΩ]
OUTSET_SET register setting	OPEN or 470
5.0	75
5.3	56
7.0	43
8.0	36
9.0	30
10.0	24
EPT or NoCh	SHORT

The used resistance should have accuracy of ±1%.

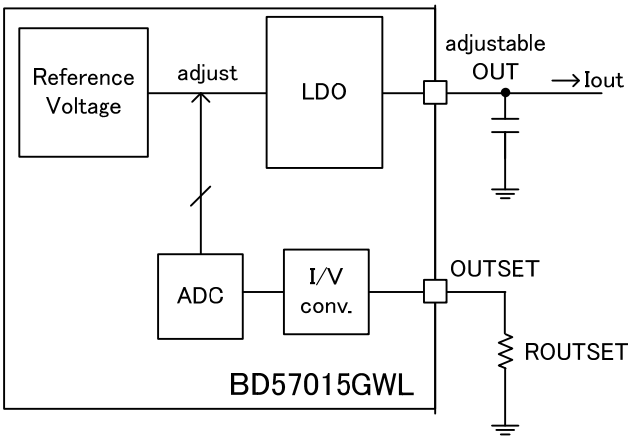

Figure 10. OUTSET setting

If OUTSET pin is shorted to GND, there will be a setting error and BD57015GWL will send EPT (internal fault) in Qi mode. And BD57015GWL will send NoCh signal repeatedly, then the charging will not be started in PMA mode.
If the bit [7] of this register is set to “1”, or OUTSET pin is OPEN, the setting of register has priority regardless of the resistance connected to the OUTSET pin. The related states on OUTSET pin can be confirmed depending on the next register (0x09).

OUTSET setting register (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial Value	R/W
OUTSET_SET	0x08	[7] OUTSET_REG_EN 0x0 : The setting of the resistance has priority. 0x1 : The setting of this register (bit[2:0]) has priority. [6:3] Reserved [2:0] OUTSET Set the LDO output voltage. 0x0 : Restricted setting 0x4 : 8.0V 0x1 : 5.0V 0x5 : 9.0V 0x2 : 5.3V 0x6 : 10.0V 0x3 : 7.0V 0x7 : 12.0V	0x01	R/W
OUTSET_STATE	0x09	OUTSET status [7] OUTSET_SHORT_DET Short detection of the OUTSET pin. 0x0 : not short 0x1 : short [6:4] OUTSET_ADC_VAL Set LDO output voltage on the read value of A/D 0x0 when the read value in A/D is outside the setting range. 0x0 : 4.5V 0x4 : 8.0V 0x1 : 5.0V 0x5 : 9.0V 0x2 : 5.3V 0x6 : 10.0V 0x3 : 7.0V 0x7 : 12.0V [3] OUTSET_OPEN_DET Enable / Disable of the register setting 0x0 : disable 0x1 : enable (make the OUTSET pin OPEN to enable this) [2:0] OUTSET_OUTPUT Actual LDO output voltage to be used 0x0 : 4.5V 0x4 : 8.0V 0x1 : 5.0V 0x5 : 9.0V 0x2 : 5.3V 0x6 : 10.0V 0x3 : 7.0V 0x7 : 12.0V	0x00	R

Please set an initial value into Reserved bits.

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14. NTC setting

Please connect the recommended NTC thermistor to the NTC pin when detecting abnormal temperature as described by the PMA standard. An EOC signal will be sent to the Transmitter in the PMA mode when the voltage on the NTC pin is higher than the threshold Vntc0 set in the NTC setting register (0x0C). The abnormal temperature detection in NTC is not available in Qi mode.

In addition to using the NTC thermistor, the EOC signal can also be sent by using the CTRL pin when temperature is monitored. Refer to section "*7.External Control Input (EN1, EN2, and CTRL)*" for the details. (Common to both PMA and Qi modes.)

The Vntc0 threshold can be defined in the following expressions.

$$Vntc0 = \frac{\mathrm{Vref_{ntc}}}{\mathrm{Rntc}} \times \mathrm{Rntc0}$$
$$= \frac{25000^{(\mathrm{NOTE1})}[\Omega \times \mathrm{V}]}{\mathrm{Rntc}[\Omega]}$$

(NOTE1) precision includes variation of 21250 to 28750.

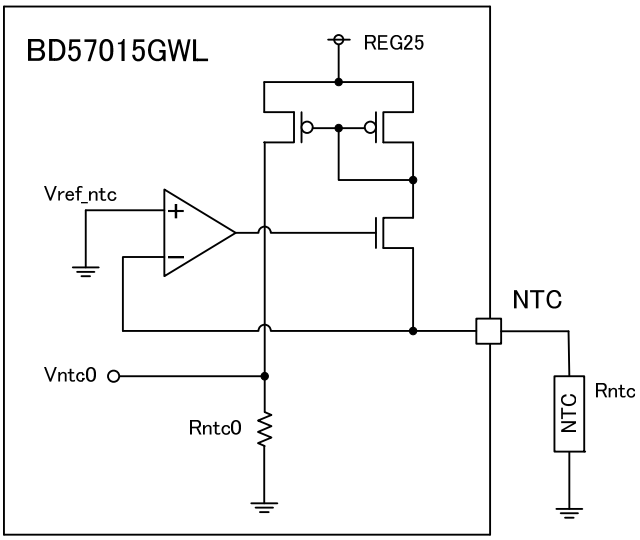

Figure 11. NTC setting

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NTC setting register (Only for PMA)

Register Name	Address	Bit[7:0]	Initial Value	R/W
NTC_SET	0x0C	[7] Reserved [6] NTC_EN (PMA mode) NTC temperature detection function 0x0 : NTC temperature detection function disabled 0x1 : NTC temperature detection function enabled [5:4] Reserved [3:0] NTC_TH Vntc0 threshold setting for the abnormal temperature detection 0x0 : more than 0.5 V 0x8 : more than 1.3 V 0x1 : more than 0.6 V 0x9 : more than 1.4 V 0x2 : more than 0.7 V 0xA : more than 1.5 V 0x3 : more than 0.8 V 0xB : more than 1.6 V 0x4 : more than 0.9 V 0xC : more than 1.7 V 0x5 : more than 1.0 V 0xD : more than 1.8 V 0x6 : more than 1.1 V 0xE : more than 1.9 V 0x7 : more than 1.2 V 0xF : more than 2.0 V	0x44	R/W
NTC_STATE	0X0D	[7:1] Reserved [0] NTC_DET Abnormal temperature detection for NTC. 0x0 : Abnormal temperature undetected 0x1 : Abnormal temperature detected	0x00	R

Please set an initial value into Reserved bits.

Rohm recommends NTC thermistor NCP15WF104F03RC (MURATA Co., Ltd.).

Resistance value (25°C)	100kΩ
Resistance value (25°C) tolerance	±1%
B constant (25/50°C)	4250K
B constant (25/50°C) tolerance	±1%
B constant (25/85°C)(Typ)	4311K

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15. PAD_DETECTION

The PAD_DETECTION function can send a signal to the host when the RX is removed from the TX after charging has been completed. To use this function, connect the external power supply to the VCCPD, with a pull-up resistance to PD and connect to the VCCPD.
The host can detect when the PD signal changes from L to H to monitor if it was removed from the charger.

The flow to the detection
1. After end of charging, Rx receives Digital Ping or Analog Ping signal from Tx. (AC2 of figure below)
2. The Ping fully charges a capacitor connected to PD_TIME pin to VCCPD. PD pin goes L.
3. If Rx is removed from Tx the pulse to AC2 is not generated, so the voltage on PD_TIME pin falls. The PD pin will go H after a time dependent on the CR network.

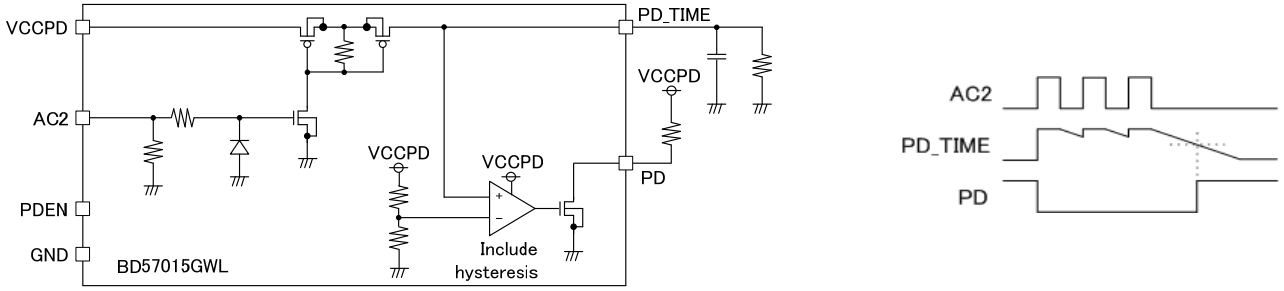

Figure 12. PAD_DETECTION

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16. Interrupt Control Block

The circuit for Interruption Generation is shown below.
This circuit detects the edge of the interrupt signal. An interrupt is sent on INTB pin depending on the events triggering the interrupt as set by the Interrupt Mask register. INTB is active L.

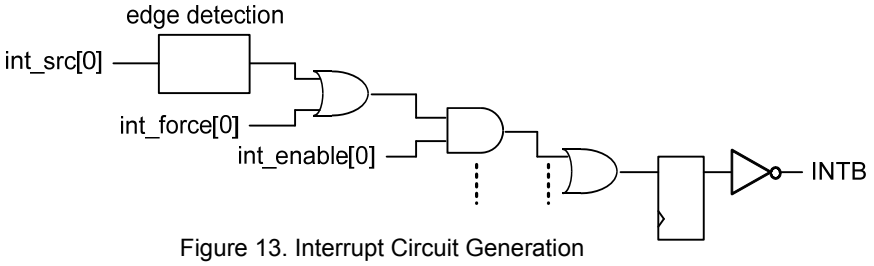

Figure 13. Interrupt Circuit Generation

16.1 Interrupt Control Register

The generation of interruption for each can be controlled by this register. If a bit is set to 1, the corresponding interrupt event will be enabled, if it is set to 0, it will be masked. The interrupt is masked by default.

Interrupt Control register 1 (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial value	R/W
INTEN1	0x10	[7:6] Reserved [5] INT_EN_PMA_EOC PMA EOC interrupt detection activation setting [4:2] Reserved [1] INT_EN_EPT_DET End Power Transfer interrupt detection activation setting [0] INT_EN_CHG_START_DET Charging start interrupt detection activation setting	0x00	R/W

Please set an initial value into Reserved bits.

Interrupt Control register 2 (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial value	R/W
INTEN2	0x11	[7:2] Reserved [1] INT_EN_ERR_POSSET_CLR Clear POSSET Error interrupt detection activation setting (During start-up) [0] INT_EN_ERR_POSSET POSSET Error interrupt detection activation setting (During start-up)	0x00	R/W

Please set an initial value into Reserved bits.

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16.2 Interrupt Status Register

This register identifies the source of an interrupt. In order to clear the interrupt event, refer to section "*16.3 Clear Interrupt Register*".

Interrupt Status register 1 (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial value	R/W
INTSTAT1	0x12	[7:6] Reserved [5] INT_PMA_EOC Interrupt due to PMA EOC [4:2] Reserved [1] INT_EPT_DET Interrupt due to End Power Transfer [0] INT_CHG_START_DET Interrupt due to Charging start	0x00	R

Reserved bits read "0"

Interrupt Status register 2 (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial value	R/W
INTSTAT2	0x13	[7:2] Reserved [1] INT_ERR_POSSET_CLR Clear POSSET Error interrupt detection (During start-up) [0] INT_ERR_POSSET POSSET Error interrupt detection (During start-up)	0x00	R

Reserved bits read "0"

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16.3 Clear Interrupt Register

This register is used to clear any interrupt.
Each interrupt will be cleared by entering “1” to each bit.
Please re-enter “0” after resetting with “1”, so the device can report the next interrupt.

Clear Interrupt register 1 (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial value	R/W
INTCLR1	0x14	[7:6] Reserved [5] INT_CLR_PMA_EOC Clear interrupt due to PMA EOC 0x0 : no flag 0x1 : clear interrupt flag [4:2] Reserved [1] INT_CLR_EPT_DET Clear interrupt due to End Power Transfer 0x0 : no flag 0x1 : clear interrupt flag [0] INT_CLR_CHG_START_DET Clear interrupt due to Charging start 0x0 : no flag 0x1 : clear interrupt flag	0x00	R/W

Please set an initial value into Reserved bits.

Clear Interrupt register 2 (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial value	R/W
INTCLR2	0x15	[7:2] Reserved [1] INT_CLR_ERR_POSSET_CLR Clear interrupt due to POSSET Error (During start-up) 0x0 : no flag 0x1 : clear interrupt flag [0] INT_CLR_ERR_POSSET Clear interrupt due to Charging Start (During start-up) 0x0 : no flag 0x1 : clear interrupt flag	0x00	R/W

Please set an initial value into Reserved bits.

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16.4 Forced Interrupt Generation Register.

This register can force generation of an interrupt caused by any of the events. Interrupt is generated by writing 1 in each bit. After writing 1, please always write 0. This function can be used for software debug checks.

Forced Interrupt Generation register 1 (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial value	R/W
INTFORCE1	0x1E	[7:6] Reserved [5] INT_FORCE15 0x0 : no flag 0x1 : force interrupt flag [4:2] Reserved [1] INT_FORCE11 0x0 : no flag 0x1 : force interrupt flag [0] INT_FORCE10 0x0 : no flag 0x1 : force interrupt flag	0x00	R/W

Please set an initial value into Reserved bits.

Forced Interrupt Generation register 2 (For Qi and PMA)

INTFORCE2	0x1F	[7:2] Reserved [1] INT_FORCE21 0x0 : no flag 0x1 : force interrupt flag [0] INT_FORCE20 0x0 : no flag 0x1 : force interrupt flag	0x00	R/W

Please set an initial value into Reserved bits.

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17. Received Power monitor register

This register is the value of Received Power Packet to TX or the value of the Received Power calculated internally by the BD57015GWL.

Received power monitor register (Only for Qi)

Register Name	Address	Bit[7:0]	Initial value	R/W
RP16VAL_B0	0x16	[7:0] RP_VAL[15:8] Received Power Value (Upper 8bits)	0x00	R
RP16VAL_B1	0x17	[7:0] RP_VAL[7:0] Received Power Value (Lower 8bits)	0x00	R

During the Qi BPP mode, only 0x16 is used as Received Power Packet.

18. Charge Frequency monitor register

It can monitor the Carrier Frequency from TX. However it may not correctly report the Carrier Frequency when the rectified voltage waveform is disturbed.

Calculation Method :
RP_FREQ = 8192 ÷ ((Received Frequency value) ÷ 64) [kHz]
(Calculate Received Frequency Value using Decimal number.)

Charge Frequency Monitor register (Only for Qi)

Register Name	Address	Bit[7:0]	Initial value	R/W
RPFREQ_B0	0x18	[7:5] Reserved [4:0] RP_FREQ[12:8] Received Frequency Value (Upper 5bits)	0x00	R
RPFREQ_B1	0x19	[7:0] RP_FREQ[7:0] Received Frequency Value (Lower 8bits)	0x00	R

Reserved reads “0”

19. Control Error Packet monitor register

In Qi mode, the received power can be controlled by sending the Control Error Packet (CE) from RX to TX. The value of the CE sent by RX is reported in this register.

CE Monitor register (Only for Qi)

Register Name	Address	Bit[7:0]	Initial value	R/W
CE_VAL	0x1A	[7:0] CE_VAL[7:0] Control Error Packet Value	0x00	R

20. Signal Strength Packet monitor register

In Qi mode, the RX sends the Signal Strength packet to TX during start-up. This register can report the value by the RX.

SS Monitor register (Only for Qi)

Register Name	Address	Bit[7:0]	Initial value	R/W
SS_VAL	0x1B	[7:0] SS_VAL[7:0] Signal Strength Packet Value	0x00	R

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21. GPIO

BD57015GWL is equipped with 3 GPIO pins. These are bidirectional and can be used either to monitor input or to output data. It is necessary to set the output mode in the GPIO I/O switching register before use.

21.1 GPIO Input register

This register reports the input condition of GPIO. If the read value is 1, the input condition of each pin is high. If it is 0, the input condition is Low.

GPIO Input register (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial value	R/W
GPODIN	0x70	[7:3] Reserved [2] GPIO3_DAT_IN GPIO3 pin input condition [1] GPIO2_DAT_IN GPIO2 pin input condition [0] GPIO1_DAT_IN GPIO1 pin input condition	XX	R

Reserved bits read “0”

21.2 GPIO Output Register

This register sets the output condition of GPIO. When setting 1, the output of GPIO is H, and when setting 0, the output is L.

GPIO Output register (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial value	R/W
GPODOUT	0x71	[7:3] Reserved [2] GPIO3_DAT_OUT GPIO3 pin Output value setting 0x0 : output L 0x1 : output H [1] GPIO2_DAT_OUT GPIO2 pin Output value setting 0x0 : output L 0x1 : output H [0] GPIO1_DAT_OUT GPIO1 pin Output value setting 0x0 : output L 0x1 : output H	0x00	R/W

Please set an initial value into Reserved bits.

21.3 GPIO I/O switching register

It can set the pin direction of GPIO. When setting 1, it will be in output mode, and when setting 0, it will be in the input mode. By default all GPIO are inputs.

GPIO I/O switching register (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial Value	R/W
GPODIR	0x72	[7:3] Reserved [2] GPIO3_DIR GPIO3 pin Input / Output setting 0x0 : input mode 0x1 : output mode [1] GPIO2_DIR GPIO2 pin Input / Output setting 0x0 : input mode 0x1 : output mode [0] GPIO1_DIR GPIO1 pin Input / Output setting 0x0 : input mode 0x1 : output mode	0x00	R/W

Please set an initial value into Reserved bits.

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21.4 GPIO Pull Up/Down Resistance Control Register

This register controls whether the Pull up or Pull down resistances on the GPIO pins are connected or disconnected internally. When setting 1, it will connect the pull up or pull down resistance and when setting 0, it will disconnect pull up or pull down resistance.

GPIO Pull Up/Down Resistance Control register (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial value	R/W
GPOPUL	0x73	[7] Reserved [6] GPIO3_PD GPIO3 Pull down resistance setting 0x0 : Disconnected 0x1 : Connected [5] GPIO2_PD GPIO2 Pull down resistance setting 0x0 : Disconnected 0x1 : Connected [4] GPIO1_PD GPIO1 Pull down resistance setting 0x0 : Disconnected 0x1 : Connected [3] Reserved [2] GPIO3_PU GPIO3 Pull up resistance setting 0x0 : Disconnected 0x1 : Connected [1] GPIO2_PU GPIO2 Pull up resistance setting 0x0 : Disconnected 0x1 : Connected [0] GPIO1_PU GPIO1 Pull up resistance setting 0x0 : Disconnected 0x1 : Connected	0x70	R/W

Please set an initial value into Reserved bits.

21.5 GPIO Function Selection register

This register sets the function of the GPIO. Always set 0 for normal use.

GPIO Function Selection register (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial value	R/W
GPOFUNC	0x74	[7:3] Reserved [2] GPIO3_FUNC_SEL GPIO3 pin function setting 0x0 : output the value set with GPIO Output register(0x71) 0x1 : output the internal monitor signal set with GPIO3 Internal Signal Monitor Selection register(0x77) [1] GPIO2_FUNC_SEL GPIO2 pin function setting 0x0 : output the value set with GPIO Output register(0x71) 0x1 : output the internal monitor signal set with GPIO2 Internal Signal Monitor Selection register(0x76) [0] GPIO1_FUNC_SEL GPIO1 pin function setting 0x0 : output the value set with GPIO Output register(0x71) 0x1 : output the internal monitor signal set with GPIO1 Internal Signal Monitor Selection register(0x75)	0x00	R/W

Please set an initial value into Reserved bits.

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21.6 GPIO Internal Signal Monitor Selection Register

Always set to 0 for normal use.

GPIO1 Internal Signal Monitor Selection register (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial value	R/W
GPOSEL1	0x75	[7:6] Reserved [5:0] GPIO1_DAT_SEL GPIO1 Internal monitor selection	0x00	R/W

Please set an initial value into Reserved bits.

GPIO2 Internal Signal Monitor Selection register (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial value	R/W
GPOSEL2	0x76	[7:6] Reserved [5:0] GPIO2_DAT_SEL GPIO2 Internal monitor selection	0x00	R/W

Please set an initial value into Reserved bits.

GPIO3 Internal Signal Monitor Selection register (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial value	R/W
GPOSEL3	0x77	[7:6] Reserved [5:0] GPIO3_DAT_SEL GPIO3 Internal monitor selection	0x00	R/W

Please set an initial value into Reserved bits.

22. REVISION Register

It contains the chip revision and the vendor ID of LSI. These bits are hardwired.

REVISION register (For Qi and PMA)

Register Name	Address	Bit[7:0]	Initial value	R/W
CHIP_ID	0x00	[7:4] CHIP_NO[3:0] Vendor ID [3:0] REV[3:0] Chip Revision	0x18	R

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23. Qi ID register

It contains the Manufacture Code and compliant version / device ID used in the Qi mode.

Qi Major version & Minor Version register (Only for Qi)

Register Name	Address	Bit[7:0]	Initial value	R/W
RX_ID_B0	0xA0	[7:4] MAJOR_VER[3:0] Based on the Major Version of the Qi standard [3:0] MINOR_VER[3:0] Based on the Minor Version of the Qi standard	0x12	R

Qi Manufacture Code Register (Only for Qi)

Register Name	Address	Bit[7:0]	Initial value	R/W
RX_ID_B1	0xA1	[7:0] MNFCT_CODE[15:8] Manufacture Code (Identification packet B1)	0x00	R/W
RX_ID_B2	0xA2	[7:0] MNFCT_CODE[7:0] Manufacture Code (Identification packet B2)	0x27	R/W

The code of 0x0027 is the Manufacture Code assigned to ROHM by WPC.
Please do not set the code other than 0x0027.

Qi Device ID Register (Only for Qi)

Register Name	Address	Bit[7:0]	Initial value	R/W
RX_ID_B3	0xA3	[7] Reserved [6:0] DEVICE_ID[30:24] Device ID[30:24] (Identification packet B3)	XX	R/W
RX_ID_B4	0xA4	[7:0] DEVICE_ID[23:16] Device ID[23:16] (Identification packet B4)	XX	R
RX_ID_B5	0xA5	[7:0] DEVICE_ID[15:8] Device ID[15:8] (Identification packet B5)	XX	R
RX_ID_B6	0xA6	[7:0] DEVICE_ID[7:0] Device ID[7:0] (Identification packet B6)	XX	R

Please set “0” to Reserved bits.

24. PMA ID register

It contains the OUI and RX Serial Number specified by IEEE and used in PMA standard. The PMA Manufacture Code register and the PMA RX Model Number register will be enabled by setting bit0 of PMA ID Write Enable setting register to 1. In that case, the written value will be used as PMA ID.

PMA Manufacture Code register (Only for PMA)

Register Name	Address	Bit[7:0]	Initial value	R/W
MAC_ID_3	0x80	[7:0] MAC_EXT_ID[23:16] Serial Number [23:16]	XX	R/W
MAC_ID_2	0x81	[7:0] MAC_EXT_ID[15:8] Serial Number [15:8]	XX	R/W
MAC_ID_1	0x82	[7:0] MAC_EXT_ID[7:0] Serial Number [7:0]	XX	R/W

PMA RX Model Number register (Only for PMA)

Register Name	Address	Bit[7:0]	Initial value	R/W
MAC_OUI_3	0x83	[7:0] MAC_OUI[23:16] OUI [23:16]	XX	R/W
MAC_OUI_2	0x84	[7:0] MAC_OUI[15:8] OUI [15:8]	XX	R/W
MAC_OUI_1	0x85	[7:0] MAC_OUI[7:0] OUI [7:0]	XX	R/W

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PMA ID Write Enable setting register (Only for PMA)

Register Name	Address	Bit[7:0]	Initial value	R/W
MAC_OUI_ID _EN	0x8F	[7:1] Reserved [0] MAC_OUI_EN Enable the register value of 0x80 to 0x85. 0x0 : Disable 0x01 : Enable	0x08	R/W

Please set an initial value into Reserved bits.

25. QI CONFIG register

The parameter of FSK defined in Qi spec can be configured with the register below.

Qi CONFIG register (Only for Qi)

Register Name	Address	Bit[7:0]	Initial value	R/W
RX_CONF_B4	0xAB	[7:5] Reserved [4] NEG Request for proceeding to the Negotiation phase 0x0 : No request 0x1 : Request sent [3] FSK POL Polarity of FSK of Tx 0x0 : positive (frequency modulation to higher frequency) 0x1 : negative (frequency modulation to lower frequency) [2] Reserved [1:0] FSK_DEPTH Modulation depth of FSK of Tx 0x0 : Minimum depth 0x3 : Maximum depth	BPP mode 0x00 EPP Mode 0x1B	R/W

Please set an initial value into Reserved bits.
Initial value is selected automatically according to the mode set with Qi Power Mode setting register(0x0E:EPP_MODE).

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26. Command Interface

26.1 Command Interface

The BD57015GWL uses I^2C bus method to communicate with host CPU. Most registers of the BD57015GWL can be written in or read out. BD57015GWL has Slave Address of 0x44(7bit). A Select Address is necessary after a Slave Address for read or write action. The format of the I^2C bus method slave mode is shown below.

MSB LSB		MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	Data	A	Data	A	P

S: Start Condition
Slave Address: Send a total of 8 bit data, put bit of the read mode (H") or write mode (L") after the slave address (7bit) that was set in the ADDR. (MSB first)
A: Add acknowledge bit in each byte in the acknowledged data sent/received.
If the data was sent/received correctly, this acknowledge bit will be "L".
If "H" was sent/received, it means that it didn't acknowledge the data.
Select Address: Use 1 byte to select the register address in BD57015GWL (MSB first)
Data: Byte data, Data sent/received (MSB first)
P: Stop Condition

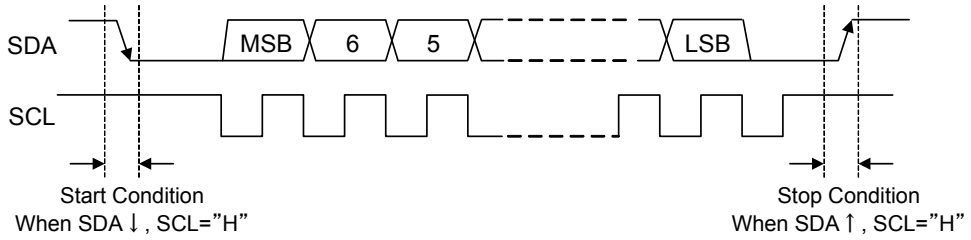

Figure 14. Command Interface

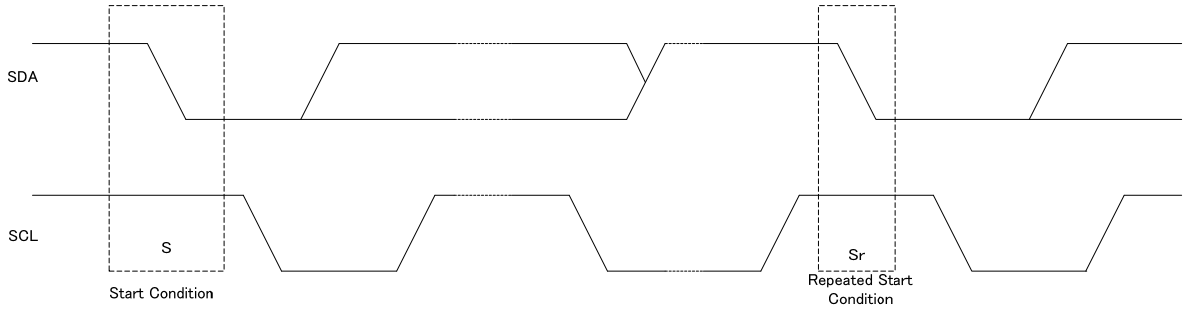

Figure 15. Repeated Start Condition

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26.2 Data Format

Write format

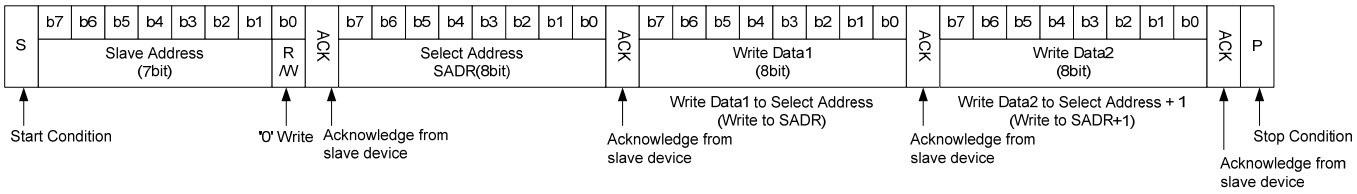

Figure 16. Write Data Format

Read format (In case of reading from the Select Address for 0x00)

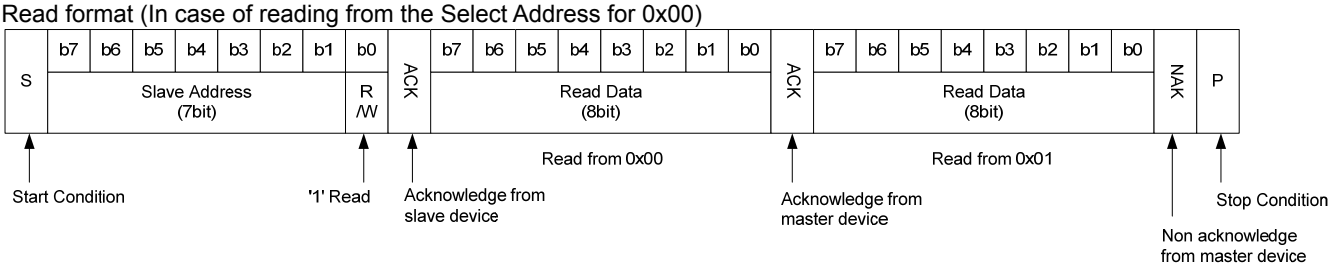

Figure 17. Read Data Format

Read Data from specified Select Address

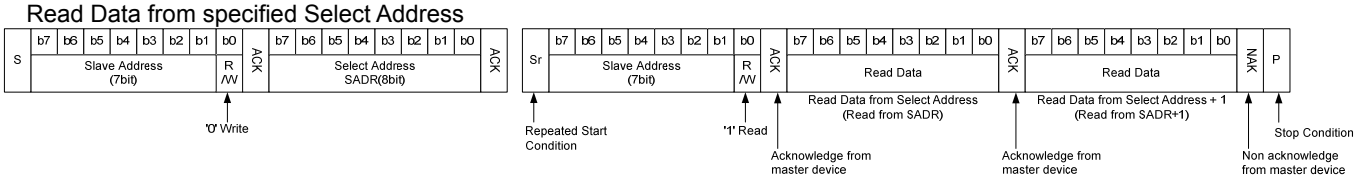

Figure 18. Read Data from specified Select Address (1)

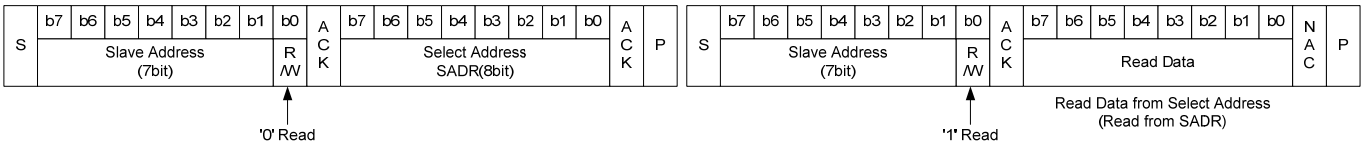

Figure 19. Read Data from specified Select Address (2)

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26.3 Control Signal Specification

Electric Specification/ Timing of bus line or I/O stage

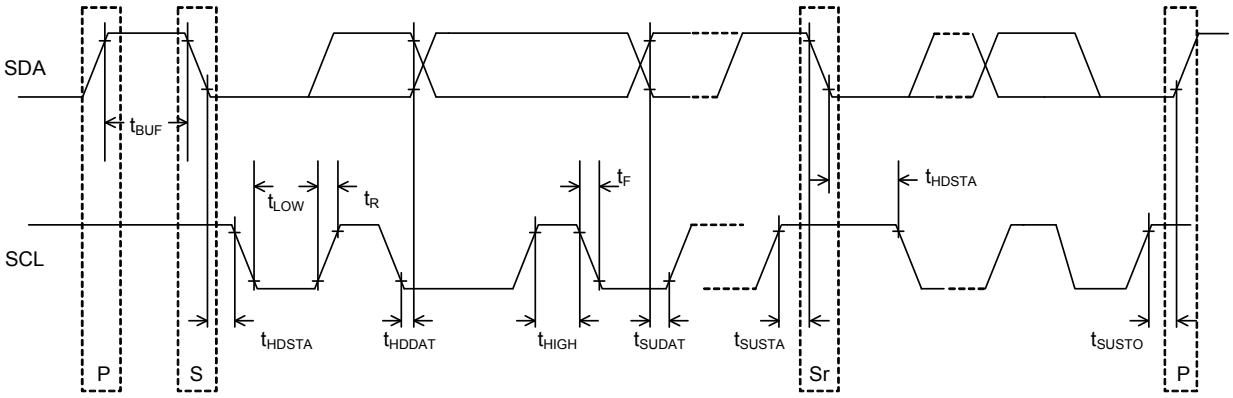

Figure 20 Timing Chart

Table 8-1. SDA/SCL bus line feature (unless otherwise specified Ta=25°C, VCC=3.0V)

Parameter		Symbol	High Speed Mode		Unit
			Min	Max	
1	SCL Clock Frequency	f_{SCL}	0	400	kHz
2	Bus free time between “Stop” condition and “Start” condition	t_{BUF}	1.3	—	μs
3	Hold Time (Re-transmit) “Start” condition. After this period, The first clock pulse is being generated.	t_{HDSTA}	0.6	—	μs
4	LOW condition holding time of SCL clock	t_{LOW}	1.3	—	μs
5	HIGH condition holding time of SCL clock	t_{HIGH}	0.6	—	μs
6	Set-up time of Re-transmit “Start” condition	t_{SUSTA}	0.6	—	μs
7	Data hold time	t_{HDDAT}	0(NOTE 1)	—	μs
8	Data set-up time	t_{SUDAT}	100	—	ns
9	Start-up time of SDA/SCL signal	t_R	20+0.1Cb	300	ns
10	Fall time of SDA/SCL signal	t_F	20+0.1Cb	300	ns
11	Set-up time of “stop” condition	t_{SUSTO}	0.6	—	μs
12	Load Capacity of each bus line	Cb	—	400	pF

All the values written above are values that correspond to $V_{IH\ min}$/$V_{IL\ max}$ level.

(NOTE 1) The transmitter internally provides the hold time in Minimum 300ns (in the $V_{IH\ min\ of\ SCL\ signal}$) for the SDA signal in order to exceed the unfixed area terminal when SCL stops.

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27. Register Map

Name	Addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Init	R/W
CHIP_ID	00	CHIP_NO[3]	CHIP_NO[2]	CHIP_NO[1]	CHIP_NO[0]	REV[3]	REV[2]	REV[1]	REV[0]	18	R
FOD1_SET	01	FOD1_REG_EN	FOD1_POLARITY	Reserved	FOD1[4]	FOD1[3]	FOD1[2]	FOD1[1]	FOD1[0]	00	R/W
FOD1_STATE	02	FOD1_SHORT_DET	FOD1_ADC_VAL[3]	FOD1_ADC_VAL[2]	FOD1_ADC_VAL[1]	FOD1_ADC_VAL[0]	FOD1_OPEN_DET	Reserved		00	R
FOD2_SET	03	FOD2_REG_EN	Reserved	FOD2[5]	FOD2[4]	FOD2[3]	FOD2[2]	FOD2[1]	FOD2[0]	07	R/W
FOD2_STATE	04	FOD2_SHORT_DET	FOD2_ADC_VAL[3]	FOD2_ADC_VAL[2]	FOD2_ADC_VAL[1]	FOD2_ADC_VAL[0]	FOD2_OPEN_DET	Reserved		00	R
FOD3_H	05	FOD3_H[7]	FOD3_H[6]	FOD3_H[5]	FOD3_H[4]	FOD3_H[3]	FOD3_H[2]	FOD3_H[1]	FOD3_H[0]	25	R/W
FOD3_L	06	FOD3_L[7]	FOD3_L[6]	FOD3_L[5]	FOD3_L[4]	FOD3_L[3]	FOD3_L[2]	FOD3_L[1]	FOD3_L[0]	55	R/W
RCOIL_SET	07	Reserved				RCOIL[3]	RCOIL[2]	RCOIL[1]	RCOIL[0]	05	R/W
OUTSET_SET	08	OUTSET_REG_EN	Reserved				OUTSET[2]	OUTSET[1]	OUTSET[0]	01	R/W
OUTSET_STATE	09	OUTSET_SHORT_DET	OUTSET_ADC_VAL[2]	OUTSET_ADC_VAL[1]	OUTSET_ADC_VAL[0]	OUTSET_OPEN_DET	OUTSET_OUTPUT[2]	OUTSET_OUTPUT[1]	OUTSET_OUTPUT[0]	00	R
ILIM_SET	0A	ILIM_REG_EN	Reserved	ILIM_SET_VAL[5]	ILIM_SET_VAL[4]	ILIM_SET_VAL[3]	ILIM_SET_VAL[2]	ILIM_SET_VAL[1]	ILIM_SET_VAL[0]	0F	R/W
ILIM_STATE	0B	ILIM_SHORT_DET	ILIM_ADC_VAL[2]	ILIM_ADC_VAL[1]	ILIM_ADC_VAL[0]	ILIM_OPEN_DET	Reserved			00	R
NTC_SET	0C	Reserved	NTC_EN	Reserved		NTC_TH[3]	NTC_TH[2]	NTC_TH[1]	NTC_TH[0]	44	R/W
NTC_STATE	0D	Reserved							ABNORMAL THRM DET	00	R
EPP_MODE	0E	EPP_MODE_SET[7]	EPP_MODE_SET[6]	EPP_MODE_SET[5]	EPP_MODE_SET[4]	EPP_MODE_SET[3]	EPP_MODE_SET[2]	EPP_MODE_SET[1]	EPP_MODE_SET[0]	10	R/W
MONI_MODE	0F	Reserved							EPP_MODE	00	R
INTEN1	10	Reserved		INT_EN_PMA_EOC	Reserved			INT_EN_EPT_DET	INT_EN_CHG_START_DET	00	R/W
INTEN2	11	Reserved						INT_EN_ERR_POSSET_CLR	INT_EN_ERR_POSSET	00	R/W
INTSTAT1	12	Reserved		INT_PMA_EOC	Reserved			INT_EPT_DET	INT_CHG_START_DET	00	R
INTSTAT2	13	Reserved						INT_ERR_POSSET_CLR	INT_ERR_POSSET	00	R
INTCLR1	14	Reserved		INT_CLR_PMA_EOC	Reserved			INT_CLR_EPT_DET	INT_CLR_CHG_START_DET	00	R/W
INTCLR2	15	Reserved						INT_CLR_ERR_POSSET_CLR	INT_CLR_ERR_POSSET	00	R/W
RP16VAL_B0	16	RP_VAL[15]	RP_VAL[14]	RP_VAL[13]	RP_VAL[12]	RP_VAL[11]	RP_VAL[10]	RP_VAL[9]	RP_VAL[8]	00	R
RP16VAL_B1	17	RP_VAL[7]	RP_VAL[6]	RP_VAL[5]	RP_VAL[4]	RP_VAL[3]	RP_VAL[2]	RP_VAL[1]	RP_VAL[0]	00	R
RPFREQ_B0	18	Reserved			RP_FREQ[12]	RP_FREQ[11]	RP_FREQ[10]	RP_FREQ[9]	RP_FREQ[8]	00	R
RPFREQ_B1	19	RP_FREQ[7]	RP_FREQ[6]	RP_FREQ[5]	RP_FREQ[4]	RP_FREQ[3]	RP_FREQ[2]	RP_FREQ[1]	RP_FREQ[0]	00	R
CE_VAL	1A	CE_VAL[7]	CE_VAL[6]	CE_VAL[5]	CE_VAL[4]	CE_VAL[3]	CE_VAL[2]	CE_VAL[1]	CE_VAL[0]	00	R
SS_VAL	1B	SS_VAL[7]	SS_VAL[6]	SS_VAL[5]	SS_VAL[4]	SS_VAL[3]	SS_VAL[2]	SS_VAL[1]	SS_VAL[0]	00	R
EPT_CODE	1C	EPT_CODE[7]	EPT_CODE[6]	EPT_CODE[5]	EPT_CODE[4]	EPT_CODE[3]	EPT_CODE[2]	EPT_CODE[1]	EPT_CODE[0]	FF	R
EOC_WR	1D	EOC_CODE[7]	EOC_CODE[6]	EOC_CODE[5]	EOC_CODE[4]	EOC_CODE[3]	EOC_CODE[2]	EOC_CODE[1]	EOC_CODE[0]	00	R
INT_FORCE1	1E	Reserved		INT_FORCE15	Reserved			INT_FORCE11	INT_FORCE10	00	R/W
INT_FORCE2	1F	Reserved						INT_FORCE21	INT_FORCE20	00	R/W

Do not use “Reserved”. When it is necessary to access Reserved bits, please write in an initial value by all means.

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Name	Addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Init	R/W
	20	Reserved								00	-
ALIGN_DET_EN	21	Reserved							ALIGN_DET_EN_WAKEUP	00	R/W
	22	Reserved								00	-
	23	Reserved								70	-
POS_GAP_LV_SET	24	Reserved				POS_GAP_LV_SET[3]	POS_GAP_LV_SET[2]	POS_GAP_LV_SET[1]	POS_GAP_LV_SET[0]	00	R/W
	25	Reserved								00	-
	26	Reserved								00	-
	27	Reserved								00	-
	28	Reserved								00	-
	29	Reserved								00	-
	2A	Reserved								00	-
	2B	Reserved								00	-
	2C	Reserved								0A	-
	2D	Reserved								02	-
	2E	Reserved								0A	-
	2F	Reserved								0A	-
	30	Reserved								0A	-
	31	Reserved								0A	-
	32	Reserved								00	-
	33	Reserved								00	-
	34	Reserved								00	-
	35	Reserved								00	-
	36	Reserved								04	-
FOD_S_PCKT_EN	37	Reserved	SEL_FOD_DATA_FUSE	Reserved					FOD_PCKT_EN	41	R/W
	38	Reserved								22	-
	39	Reserved								00	-
FOD_S_PCKT1_1	3A	FOD_PCKT_B1[7]	FOD_PCKT_B1[6]	FOD_PCKT_B1[5]	FOD_PCKT_B1[4]	FOD_PCKT_B1[3]	FOD_PCKT_B1[2]	FOD_PCKT_B1[1]	FOD_PCKT_B1[0]	00	R/W
	3B	Reserved								00	-
	3C	Reserved								00	-
	3D	Reserved								00	-
	3E	Reserved								00	-
	3F	Reserved								00	-
	40	Reserved								00	-
IDET_DUMP_I	41	IDET_DUMP_I[7]	IDET_DUMP_I[6]	IDET_DUMP_I[5]	IDET_DUMP_I[4]	IDET_DUMP_I[3]	IDET_DUMP_I[2]	IDET_DUMP_I[1]	IDET_DUMP_I[0]	C0	R/W
	42	Reserved								00	-
	43	Reserved								00	-
	44	Reserved								80	-
	45	Reserved								00	-
	46	Reserved								FF	-
	47	Reserved								03	-
	48	Reserved								00	-
	49	Reserved								01	-
	4A	Reserved								0F	-
	4B	Reserved								03	-
IDET_STATE	4C	Reserved				IDET_STATE[3]	IDET_STATE[2]	IDET_STATE[1]	IDET_STATE[0]	01	R
	4D	Reserved								00	-
DUMP_T	4E	DUMP_T[7]	DUMP_T[6]	DUMP_T[5]	DUMP_T[4]	DUMP_T[3]	DUMP_T[2]	DUMP_T[1]	DUMP_T[0]	00	R/W
	4F	Reserved								00	-

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Name	Addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Init	R/W
	50	Reserved								00	-
T_DP_OFFSET_QI_1	51	T_DP_OFFSET_QI_1[7]	T_DP_OFFSET_QI_1[6]	T_DP_OFFSET_QI_1[5]	T_DP_OFFSET_QI_1[4]	T_DP_OFFSET_QI_1[3]	T_DP_OFFSET_QI_1[2]	T_DP_OFFSET_QI_1[1]	T_DP_OFFSET_QI_1[0]	00	R/W
T_DP_OFFSET_QI_2	52	T_DP_OFFSET_QI_2[7]	T_DP_OFFSET_QI_2[6]	T_DP_OFFSET_QI_2[5]	T_DP_OFFSET_QI_2[4]	T_DP_OFFSET_QI_2[3]	T_DP_OFFSET_QI_2[2]	T_DP_OFFSET_QI_2[1]	T_DP_OFFSET_QI_2[0]	00	R/W
	53	Reserved								00	-
	54	Reserved								00	-
T_DP_I_THRD_QI	55	Reserved		T_DP_I_THRD_QI[5]	T_DP_I_THRD_QI[4]	T_DP_I_THRD_QI[3]	T_DP_I_THRD_QI[2]	T_DP_I_THRD_QI[1]	T_DP_I_THRD_QI[0]	00	R/W
	56	Reserved								00	-
	57	Reserved								00	-
	58	Reserved								07	-
	59	Reserved								00	-
	5A	Reserved								00	-
	5B	Reserved								00	-
	5C	Reserved								00	-
CALIB_LL_DP_SET	5D	CALIB_LL_DP_SET[7]	CALIB_LL_DP_SET[6]	CALIB_LL_DP_SET[5]	CALIB_LL_DP_SET[4]	CALIB_LL_DP_SET[3]	CALIB_LL_DP_SET[2]	CALIB_LL_DP_SET[1]	CALIB_LL_DP_SET[0]	00	R/W
	5E	Reserved								00	-
	5F	Reserved								00	-
	60	Reserved								00	-
	61	Reserved								00	-
	62	Reserved								00	-
	63	Reserved								00	-
	64	Reserved								00	-
	65	Reserved								00	-
	66	Reserved								00	-
	67	Reserved								00	-
	68	Reserved								00	-
	69	Reserved								00	-
	6A	Reserved								00	-
	6B	Reserved								00	-
	6C	Reserved								00	-
	6D	Reserved								00	-
	6E	Reserved								00	-
	6F	Reserved								00	-
GPODIN	70	Reserved					GPIO3_DAT_IN	GPIO2_DAT_IN	GPIO1_DAT_IN	XX	R
GPODOUT	71	Reserved					GPIO3_DAT_OUT	GPIO2_DAT_OUT	GPIO1_DAT_OUT	00	R/W
GPODIR	72	Reserved					GPIO3_DIR	GPIO2_DIR	GPIO1_DIR	00	R/W
GPOPUL	73	Reserved	GPIO3_PD	GPIO2_PD	GPIO1_PD	Reserved	GPIO3_PU	GPIO2_PU	GPIO1_PU	70	R/W
GPOFUNC	74	Reserved					GPIO3_FUNC_SEL	GPIO2_FUNC_SEL	GPIO1_FUNC_SEL	00	R/W
GPOSEL1	75	Reserved		GPIO1_DAT_SEL[5]	GPIO1_DAT_SEL[4]	GPIO1_DAT_SEL[3]	GPIO1_DAT_SEL[2]	GPIO1_DAT_SEL[1]	GPIO1_DAT_SEL[0]	00	R/W
GPOSEL2	76	Reserved		GPIO2_DAT_SEL[5]	GPIO2_DAT_SEL[4]	GPIO2_DAT_SEL[3]	GPIO2_DAT_SEL[2]	GPIO2_DAT_SEL[1]	GPIO2_DAT_SEL[0]	00	R/W
GPOSEL3	77	Reserved		GPIO3_DAT_SEL[5]	GPIO3_DAT_SEL[4]	GPIO3_DAT_SEL[3]	GPIO3_DAT_SEL[2]	GPIO3_DAT_SEL[1]	GPIO3_DAT_SEL[0]	00	R/W
	78	Reserved								00	-
	79	Reserved								00	-
	7A	Reserved								00	-
	7B	Reserved								00	-
	7C	Reserved								00	-
	7D	Reserved								00	-
	7E	Reserved								00	-
	7F	Reserved								00	-

Do not use “Reserved”. When it is necessary to access Reserved bits, please write in an initial value by all means.

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Name	Addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Init	R/W
MAC_ID_3	80	MAC_EXT_ID[23]	MAC_EXT_ID[22]	MAC_EXT_ID[21]	MAC_EXT_ID[20]	MAC_EXT_ID[19]	MAC_EXT_ID[18]	MAC_EXT_ID[17]	MAC_EXT_ID[16]	XX	R/W
MAC_ID_2	81	MAC_EXT_ID[15]	MAC_EXT_ID[14]	MAC_EXT_ID[13]	MAC_EXT_ID[12]	MAC_EXT_ID[11]	MAC_EXT_ID[10]	MAC_EXT_ID[9]	MAC_EXT_ID[8]	XX	R/W
MAC_ID_1	82	MAC_EXT_ID[7]	MAC_EXT_ID[6]	MAC_EXT_ID[5]	MAC_EXT_ID[4]	MAC_EXT_ID[3]	MAC_EXT_ID[2]	MAC_EXT_ID[1]	MAC_EXT_ID[0]	XX	R/W
MAC_OUI_3	83	MAC_OUI [23]	MAC_OUI [22]	MAC_OUI [21]	MAC_OUI [20]	MAC_OUI [19]	MAC_OUI [18]	MAC_OUI [17]	MAC_OUI [16]	XX	R/W
MAC_OUI_2	84	MAC_OUI [15]	MAC_OUI [14]	MAC_OUI [13]	MAC_OUI [12]	MAC_OUI [11]	MAC_OUI [10]	MAC_OUI[9]	MAC_OUI[8]	XX	R/W
MAC_OUI_1	85	MAC_OUI[7]	MAC_OUI[6]	MAC_OUI[5]	MAC_OUI[4]	MAC_OUI[3]	MAC_OUI[2]	MAC_OUI[1]	MAC_OUI[0]	XX	R/W
EOC_MASK	86	Reserved				MASK_NOLOAD	MASK_FULL	Reserved		0C	R/W
	87	Reserved								21	-
	88	Reserved								00	-
	89	Reserved								00	-
	8A	Reserved								00	-
	8B	Reserved								00	-
	8C	Reserved								6C	-
MODE_STATUS	8D	Reserved	PMA_MODE	QI_MODE	Reserved					00	R
	8E	Reserved								00	-
MAC_OUI_ID_EN	8F	Reserved							MAC_OUI_EN	08	R/W
	90	Reserved								XX	-
	91	Reserved								00	-
	92	Reserved								00	-
	93	Reserved								00	-
	94	Reserved								00	-
	95	Reserved								XX	-
	96	Reserved								XX	-
	97	Reserved								00	-
	98	Reserved								00	-
	99	Reserved								00	-
	9A	Reserved								00	-
	9B	Reserved								00	-
	9C	Reserved								XX	-
	9D	Reserved								XX	-
	9E	Reserved								XX	-
	9F	Reserved								XX	-
RX_ID_B0	A0	MAJOR_VER [3]	MAJOR_VER [2]	MAJOR_VER [1]	MAJOR_VER [0]	MINOR_VER [3]	MINOR_VER [2]	MINOR_VER [1]	MINOR_VER [0]	12	R
RX_ID_B1	A1	MNFCT_CODE[15]	MNFCT_CODE[14]	MNFCT_CODE[13]	MNFCT_CODE[12]	MNFCT_CODE[11]	MNFCT_CODE[10]	MNFCT_CODE[9]	MNFCT_CODE[8]	00	R/W
RX_ID_B2	A2	MNFCT_CODE[7]	MNFCT_CODE[6]	MNFCT_CODE[5]	MNFCT_CODE[4]	MNFCT_CODE[3]	MNFCT_CODE[2]	MNFCT_CODE[1]	MNFCT_CODE[0]	27	R/W
RX_ID_B3	A3	Reserved	DEVICE_ID [30]	DEVICE_ID [29]	DEVICE_ID [28]	DEVICE_ID [27]	DEVICE_ID [26]	DEVICE_ID [25]	DEVICE_ID [24]	XX	R/W
RX_ID_B4	A4	DEVICE_ID [23]	DEVICE_ID [22]	DEVICE_ID [21]	DEVICE_ID [20]	DEVICE_ID [19]	DEVICE_ID [18]	DEVICE_ID [17]	DEVICE_ID [16]	XX	R
RX_ID_B5	A5	DEVICE_ID [15]	DEVICE_ID [14]	DEVICE_ID [13]	DEVICE_ID [12]	DEVICE_ID [11]	DEVICE_ID [10]	DEVICE_ID [9]	DEVICE_ID [8]	XX	R
RX_ID_B6	A6	DEVICE_ID [7]	DEVICE_ID [6]	DEVICE_ID [5]	DEVICE_ID [4]	DEVICE_ID [3]	DEVICE_ID [2]	DEVICE_ID [1]	DEVICE_ID [0]	XX	R
	A7	Reserved								0A	-
	A8	Reserved								00	-
	A9	Reserved								00	-
	AA	Reserved								00	-
RX_CONF_B4	AB	Reserved			NEG	FSK_POL	Reserved	FSK_DEPTH[1]	FSK_DEPTH [0]	BPP: 00 EPP: 1B	R/W
	AC	Reserved								00	-
	AD	Reserved								18	-
	AE	Reserved								00	-
	AF	Reserved								00	-

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Name	Addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Init	R/W
	B0	Reserved								00	-
	B1	Reserved								00	-
	B2	Reserved								00	-
	B3	Reserved								0A	-
	B4	Reserved								00	-
	B5	Reserved								00	-
	B6	Reserved								00	-
	B7	Reserved								00	-
	B8	Reserved								00	-
	B9	Reserved								00	-
	BA	Reserved								00	-
	BB	Reserved								00	-
	BC	Reserved								00	-
	BD	Reserved								00	-
	BE	Reserved								0F	-
	BF	Reserved								FC	-
	C0	Reserved								00	-
	C1	Reserved								00	-
	C2	Reserved								00	-
	C3	Reserved								00	-
	C4	Reserved								00	-
ADC_RECT_H	C5	Reserved						ADC_RECT [9]	ADC_RECT [8]	00	R
ADC_RECT_L	C6	ADC_RECT [7]	ADC_RECT [6]	ADC_RECT [5]	ADC_RECT [4]	ADC_RECT [3]	ADC_RECT [2]	ADC_RECT [1]	ADC_RECT [0]	00	R
	C7	Reserved								00	-
	C8	Reserved								00	-
	C9	Reserved								00	-
	CA	Reserved								00	-
	CB	Reserved								00	-
	CC	Reserved								00	-
	CD	Reserved								00	-
	CE	Reserved								00	-
	CF	Reserved								00	-
	D0	Reserved								00	-
	D1	Reserved								00	-
	D2	Reserved								00	-
	D3	Reserved								00	-
	D4	Reserved								00	-
	D5	Reserved								00	-
	D6	Reserved								00	-
	D7	Reserved								00	-
	D8	Reserved								00	-
	D9	Reserved								00	-
	DA	Reserved								00	-
	DB	Reserved								00	-
	DC	Reserved								00	-
	DD	Reserved								05	-
	DE	Reserved								C5	-
	DF	Reserved								00	-

Do not use “Reserved”. When it is necessary to access Reserved bits, please write in an initial value by all means.

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Name	Addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Init	R/W
	E0	Reserved								00	-
	E1	Reserved								00	-
	E2	Reserved								00	-
	E3	Reserved								00	-
	E4	Reserved								00	-
	E5	Reserved								00	-
	E6	Reserved								00	-
	E7	Reserved								00	-
	E8	Reserved								40	-
	E9	Reserved								87	-
	EA	Reserved								00	-
	EB	Reserved								00	-
	EC	Reserved								00	-
	ED	Reserved								00	-
	EE	Reserved								00	-
	EF	Reserved								00	-
	F0	Reserved								00	-
	F1	Reserved								00	-
	F2	Reserved								00	-
	F3	Reserved								00	-
	F4	Reserved								00	-
	F5	Reserved								00	-
	F6	Reserved								00	-
	F7	Reserved								00	-
	F8	Reserved								00	-
	F9	Reserved								00	-
	FA	Reserved								00	-
	FB	Reserved								00	-
	FC	Reserved								00	-
	FD	Reserved								00	-
	FE	Reserved								00	-
	FF	Reserved								00	-

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28. Application Circuit Example

28.1 Recommended Circuit Diagram

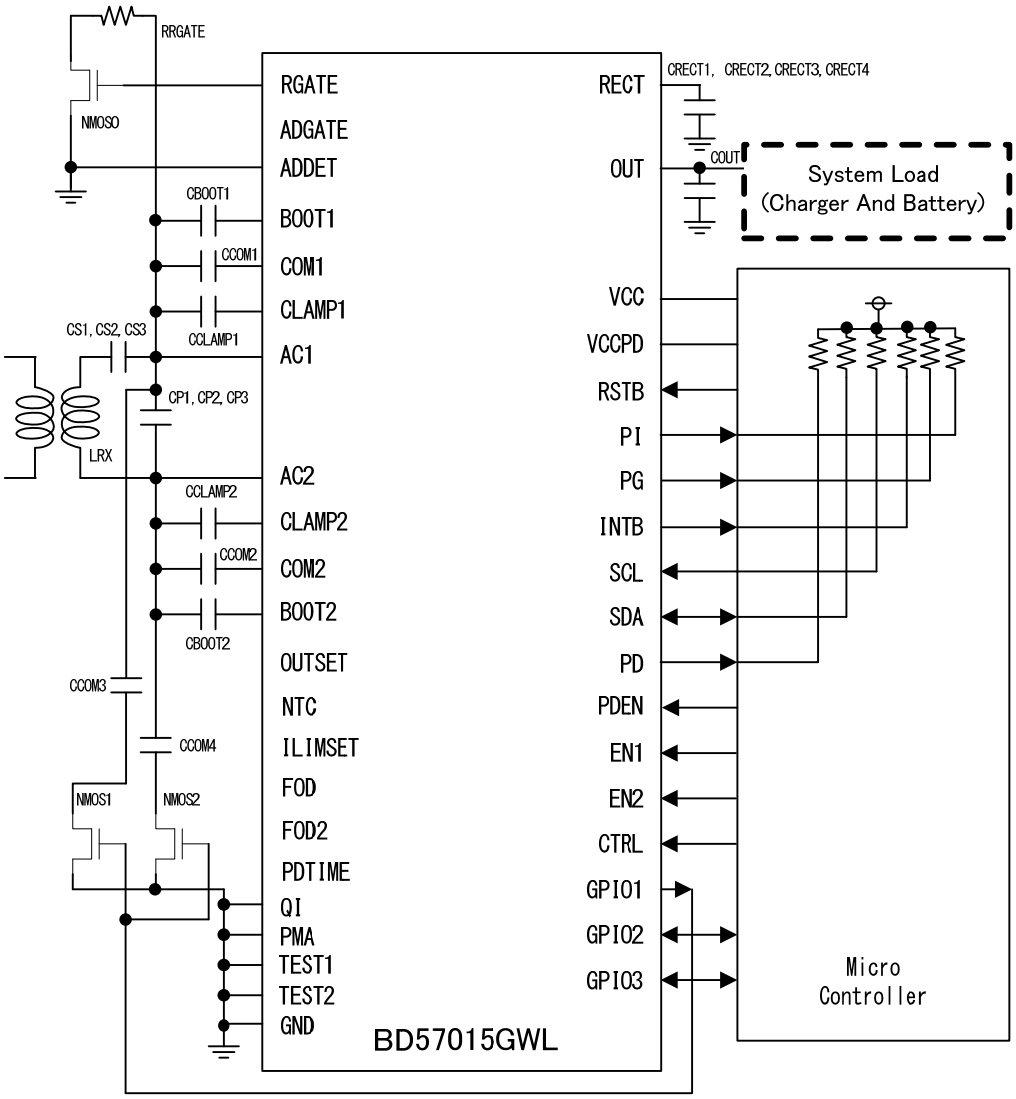

Figure 21. Representative Application Circuit Diagram

28.2 Parts List

Part Name	Informative Value	Unit	Informative Part	Maker
LRX	8.0	μH	760 308 102 207	WURTH ELEKTRONIK Co.,Ltd
CS1	0.1	μF	GRM Series	MURATA Co.,Ltd.
CS2	0.082	μF	GRM Series	MURATA Co.,Ltd.
CS3	0.082	μF	GRM Series	MURATA Co.,Ltd.
CP1	2200	pF	GRM Series	MURATA Co.,Ltd.
CP2	820	pF	GRM Series	MURATA Co.,Ltd.
CP3	-	pF	GRM Series	MURATA Co.,Ltd.
CBOOT1, CBOOT2	0.01	μF	GRM Series	MURATA Co.,Ltd.
CCOM1, CCOM2	0.047	μF	GRM Series	MURATA Co.,Ltd.
CCOM3, CCOM4	0.01	μF	GRM Series	MURATA Co.,Ltd.
CCLAMP1, CCLAMP2	0.1	μF	GRM Series	MURATA Co.,Ltd.
CRECT1	10	μF	GRM Series	MURATA Co.,Ltd.
CRECT2	10	μF	GRM Series	MURATA Co.,Ltd.
CRECT3	10	μF	GRM Series	MURATA Co.,Ltd.
COUT1	2.2	μF	GRM Series	MURATA Co.,Ltd.
RRGATE	3.9	Ω	MCR10 Series	ROHM Co.,Ltd.
NMOS0	-	-	RTF025N03	ROHM Co.,Ltd.
NMOS1, NMOS2	-	-	RTF025N03	ROHM Co.,Ltd.

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29. Operation Sequence

29.1 PMA Operation Sequence

The Operation Sequence in the PMA Mode is shown below.

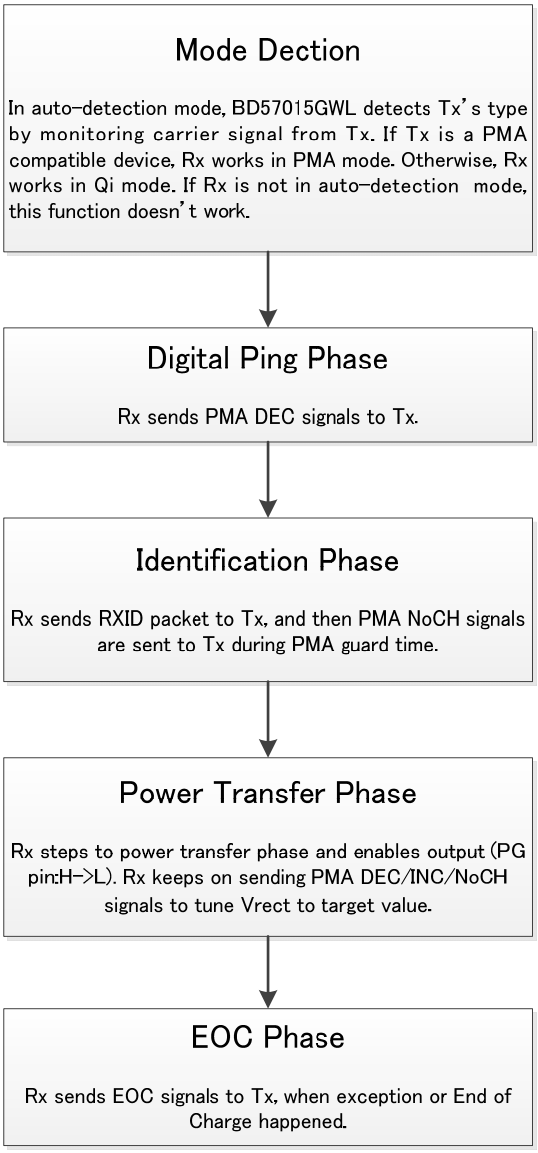

Figure 22. PMA Operation Sequence

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29.2.1 Qi Operation Sequence

The Operation Sequence in the Qi Mode is shown below.

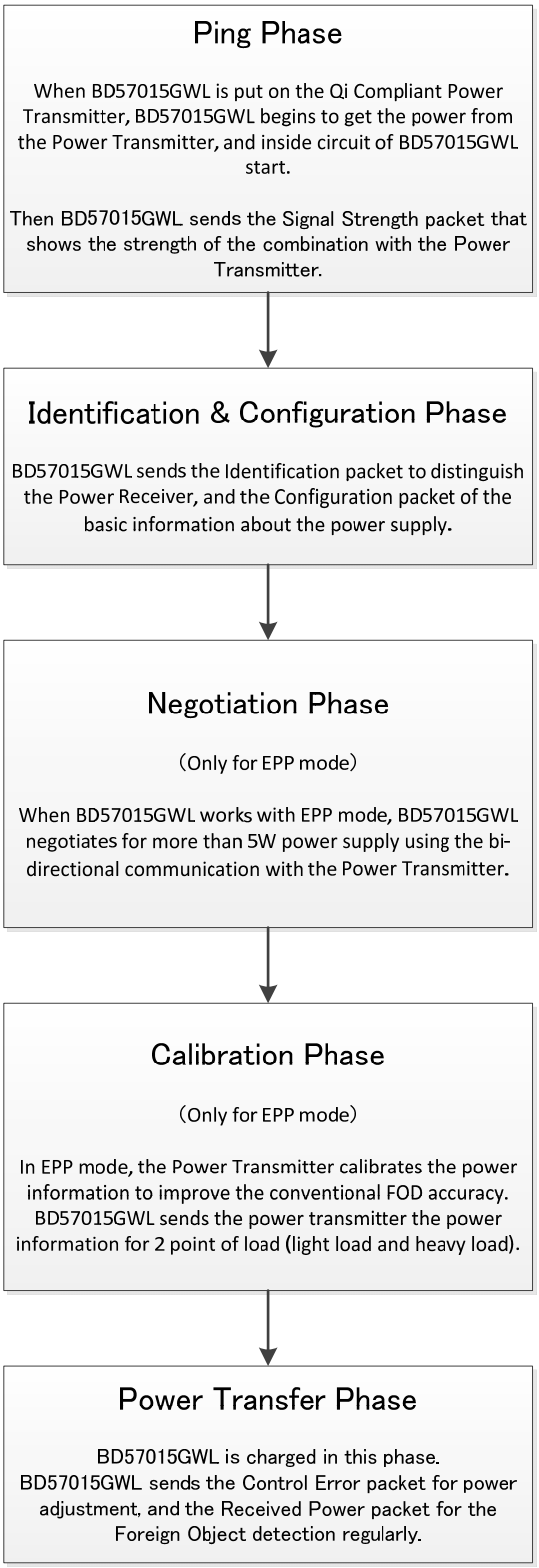

Figure 23. Qi Operation Sequence

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29.2.2 Qi EPP Configuration setting (Informative)

The following setup is necessary to operate BD57015GWL in the Qi EPP mode.
(ILIMSET, FOD, FOD2 and OUTSET pins open)

29.2.2.1 Block Diagram

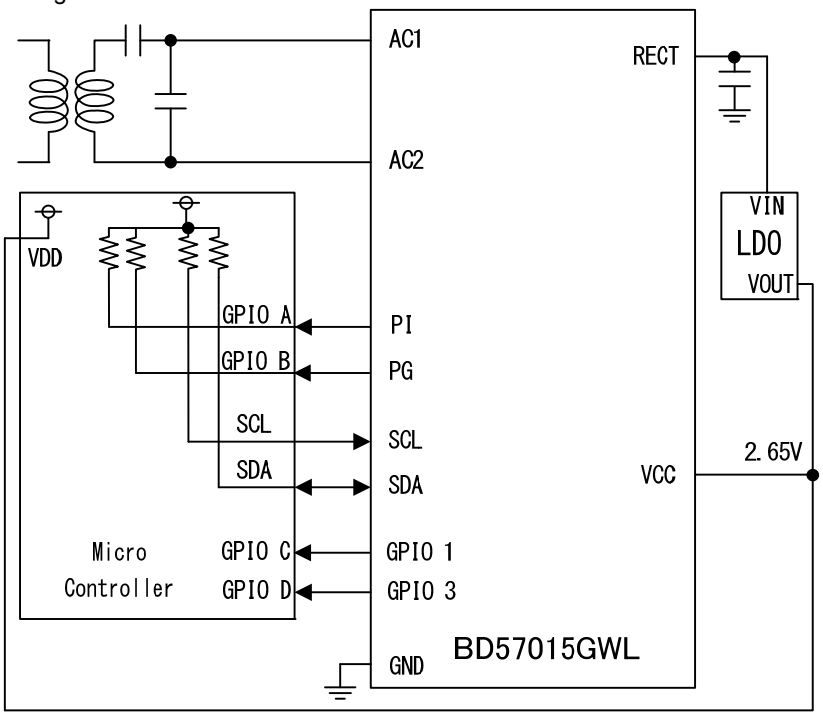

Figure 24. Connection of MicroController and BD57015GWL

29.2.2.2 Connection between MicroController and BD57015GWL

MicroController side	BD57015GWL side
GPIOA (IN)	PI (OUT) (Power Indicator : Polling)
GPIOB (IN)	PG (OUT) (Power Good : Polling)
VDD	VDD
GPIOC (IN)	GPIO1 (OUT) (In Qi mode : IDET015 : polling)
GPIOD (IN)	GPIO3 (OUT) (In Qi mode : inversion signal of PG : polling)
SCL (OUT)	SCL (IN)
SDA (I/O)	SDA (I/O)

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29.2.2.3 Qi EPP settingFlow

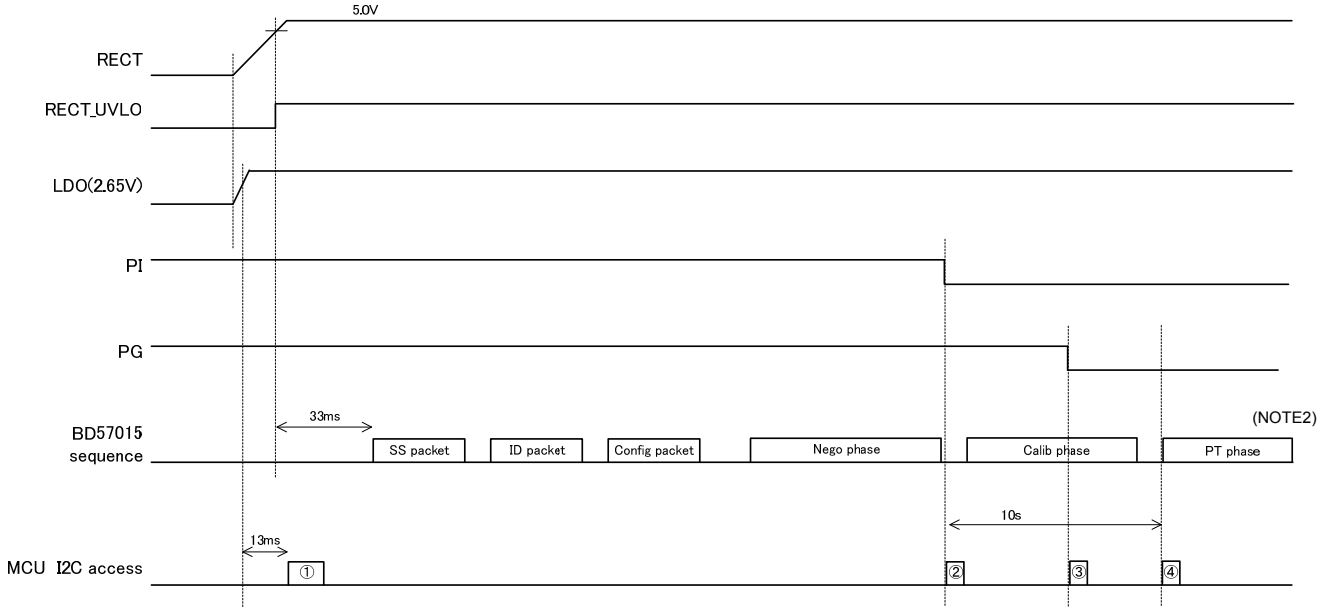

Figure 25. Qi EPP setting flow

① After RECT starts to rise and the Power-On Reset of the microcontroller (around 13 ms(NOTE1))
Within 33 ms from BD57015GWL to the start of SS, set Register “1” of 29.2.2.4 Register setting

② If PI=L is detected, set Register “2” of 29.2.2.4.

③ If PG=L is detected, set Register “3” of 29.2.2.4.

④ If PI=L is detected, after that 10 s, set Register “4” of 29.2.2.4.

(NOTE1) The timing of Power-On Reset is different depend on microcontroller.
13 ms shown here is an informative value when the microcontroller is ML610Q112 (LAPIS Semiconductor Co.,Ltd.).
(NOTE2) The meanings of SS, ID, Conf, Nego, Calib,and PT are as follows.

SS	= Signal Strength
ID	= Identification
Conf	= Configuration
Nego	= Negotiation
Calib	= Calibration
PT	= Power Transfer

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29.2.2.4 Register setting for EPP

Register “1” setting

0x0E = 0x11 ; EPP_MODE	Set EPP (CAUTION : Write it before the other registers)
0x01 = 0x85 ; FOD1_SET	Adjust the Received Power (NOTE1) (NOTE2)
0x03 = 0x83 ; FOD2_SET	Adjust the Received Power (NOTE1) (NOTE2)
0x05 = 0x25 ; FOD3_H	Adjust the Received Power (NOTE1) (NOTE2)
0x06 = 0x55 ; FOD3_L	Adjust the Received Power (NOTE1) (NOTE2)
0x07 = 0x05 ; RCOIL_SET	Adjust the Received Power (NOTE1) (NOTE2)
0x08 = 0x01 ; OUTSET_SET	Set the Output Voltage of the LDO to 5V (Informative value). (NOTE1) (NOTE2)
0x0A = 0x93 ; ILIM_SET	Set the threshold of the overcurrent protection to 1200mA. (Informative value)
0x37 = 0x01 ; FOD_S_PCKT_EN	Execute the output setting of the Q value packet..
0x3A = 0x37 ; FOD_S_PCKT1_1	Set the Q value. (NOTE1)
0x41 = 0xC0 ; IDET_DUMP_I	Adjust the Received Power (NOTE1) (NOTE2)
0x51 = 0x00 ;T_DP_OFFSET_QI_1	Adjust the Received Power (NOTE1) (NOTE2)
0x52 = 0x00 ;T_DP_OFFSET_QI_2	Adjust the Received Power (NOTE1) (NOTE2)
0x5D = 0xE4 ; CALIB_LL_DP_SET	Adjust the Received Power (NOTE1) (NOTE2)
0x72 = 0x07 ; GPIODIR	Set the GPIO1,3 of BD57015GWL.
0x73 = 0x70 ; GPIOPUL	Set the GPIO1,3 of BD57015GWL.
0x74 = 0x05 ; GPOFUNC	Set the GPIO1,3 of BD57015GWL.
0x75 = 0x00 ; GPO_DAT_SEL1	Set the GPIO1 of BD57015GWL.
0x77 = 0x2F ; GPIO_DAT_SEL3	Set the GPIO3 of BD57015GWL. (In 0x2F and Qi mode, set it to output the inversion signal of PG.)
0xAB = 0x13 ; RX_CONF_B4	Set the Polarity of FSK.

Register “2” setting

0x08 = 0x86 ; OUTSET_SET	Set the Ouput Voltage of the LDO to 10V (Informative value). (NOTE1) (NOTE3)
0x01 = 0x8C ; FOD1_SET	Set to Light Load during Calibration of the EPP mode. (NOTE1) (NOTE3)
0x05 = 0xE5 ; FOD3_H	Set to Light Load during Calibration of the EPP mode. (NOTE1) (NOTE3)
0x0E = 0x01 ; EPP_MODE	Set EPP
0x41 = 0xF0 ; IDET_DUMP_I	Set to Light Load during Calibration of the EPP mode. (NOTE1) (NOTE3)
0x75 = 0x03 ; GPIO_DAT_SEL1	Set the GPIO1 of BD57015GWL. (In 0x03 and Qi mode, set it to output IDET015.)

Register “3” setting (Only for PI=L and PG=L)

0x01 = 0x92 ; FOD1_SET	Adjust Received Power (NOTE1) (NOTE3)
0x03 = 0x85 ; FOD2_SET	Adjust Received Power (NOTE1) (NOTE3)
0x06 = 0x59 ; FOD3_L	Adjust Received Power (NOTE1) (NOTE3)
0x51 = 0x80 ;T_DP_OFFSET_QI_1	Adjust Received Power (NOTE1) (NOTE3)
0x52 = 0x28 ;T_DP_OFFSET_QI_2	Adjust Received Power (NOTE1) (NOTE3)

Register “4” setting (Only for PI=L and PG=L)

0x51 = 0x00 ;T_DP_OFFSET_QI_1	Adjust Received Power (NOTE1)
0x52 = 0x00 ;T_DP_OFFSET_QI_2	Adjust Received Power (NOTE1)

(NOTE1) The most suitable values to write in every set are different. The value is an example.
(NOTE2) Please write in the set point in the BPP mode.
(NOTE3) Please write in the set point in the EPP mode.

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30. Access Sequence for Serial Interface

The relationship between VCC, RSTB and Serial Interface are described below.

Please set “H” to RSTB ~10us after rise of VCC.

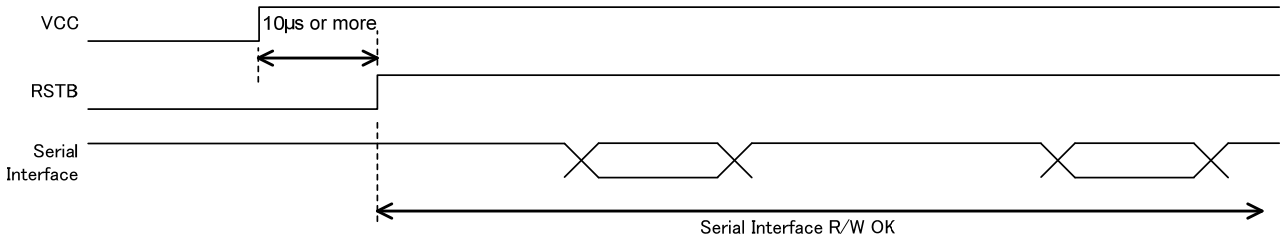

Figure 26. Serial Interface access sequence 1

Please allow ~10 μs or more rise time of VCC when RSTB pin is set to OPEN.

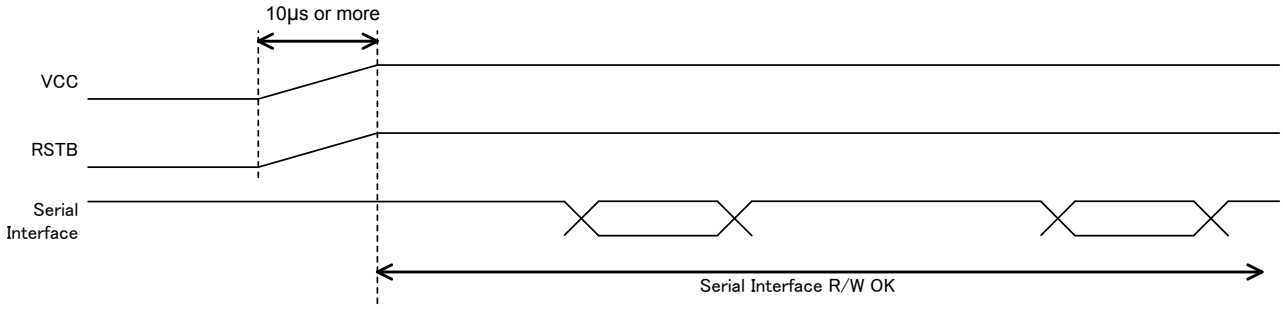

Figure 27. Serial Interface access sequence 2

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31. Characteristic data (Informative)

This section shows the characteristic data using WÜRTH 760 308 102 207 coil.

31.1 Qi mode

31.1.1 Startup waveform

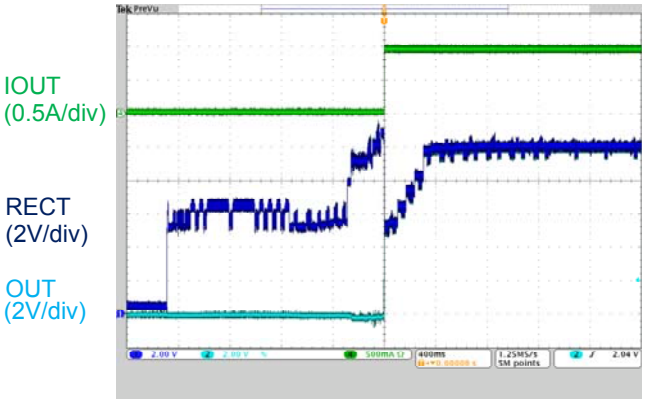

Figure 28. EPP mode: OUT=10V,
TX=ROHM BD57020MWV (MP A1)

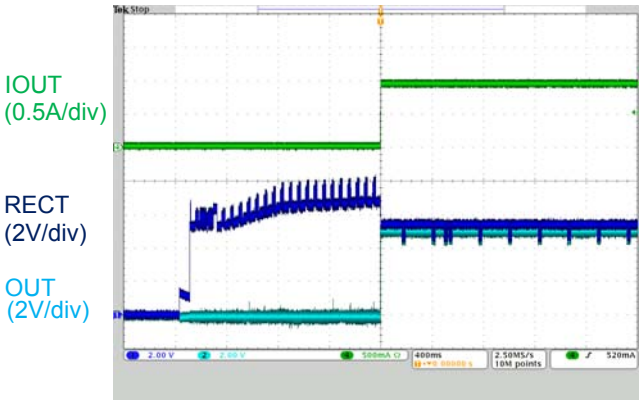

Figure 29. BPP mode: OUT=5V,
TX=ROHM BD57021MWV (LP A11)

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31.1.2 Load step

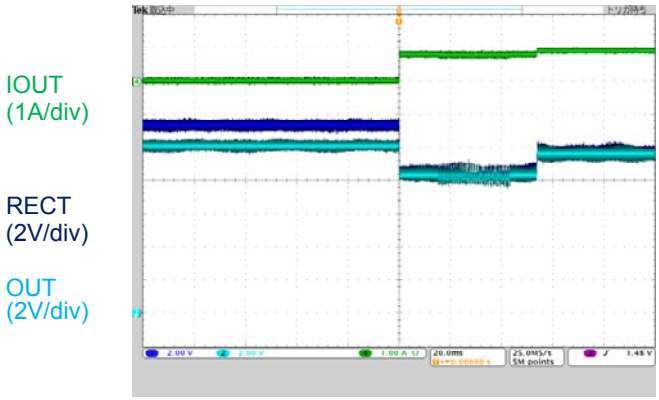

Figure 30. EPP mode: OUT=10V,
0A to 1A, TX=ROHM BD57020MWV (MP A1)

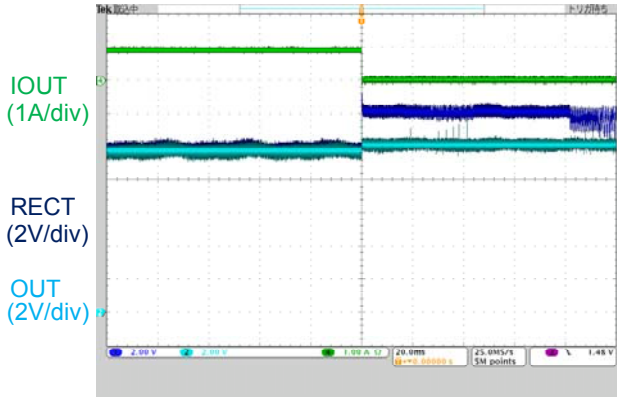

Figure 31. EPP mode: OUT=10V,
1A to 0A, TX=ROHM BD57020MWV (MP A1)

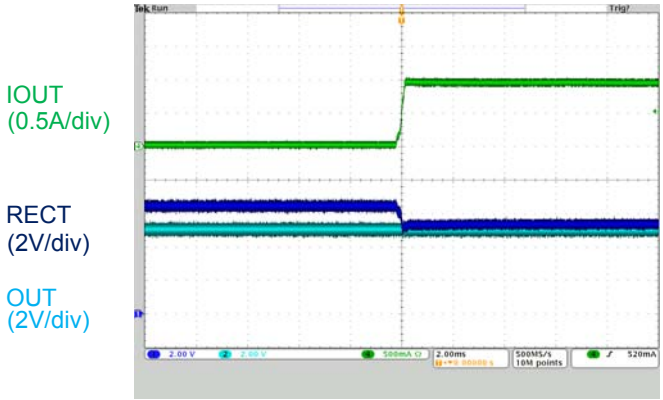

Figure 32. BPP mode: OUT=5V,
0A to 1A, TX=ROHM BD57021MWV (LP A11)

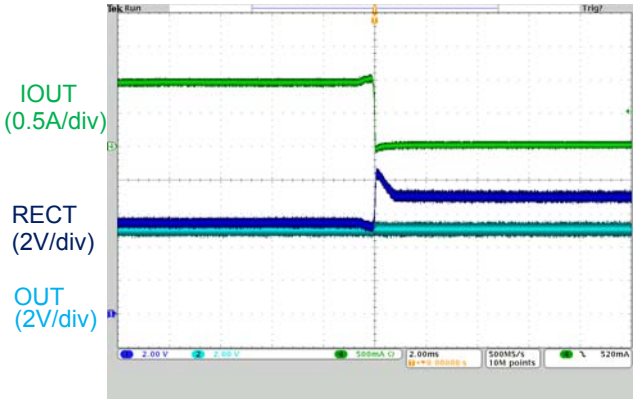

Figure 33. BPP mode: OUT=5V,
1A to 0A, TX=ROHM BD57021MWV (LP A11)

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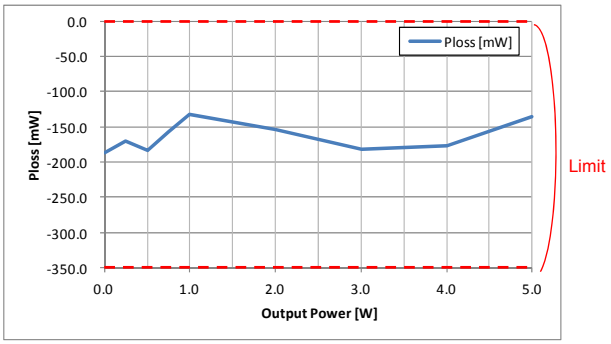
31.1.3 Received Power



(Measurement condition)
TX = AVID FOD Reference Board
Rx side thickness = 1.3mm (Acrylic board)
Coil position = Center
Battery on Rx = None

Figure 34. Ploss vs Output Power
BPP mode: OUT=5V

31.1.4 VRECT, VOUT with respect to IOUT

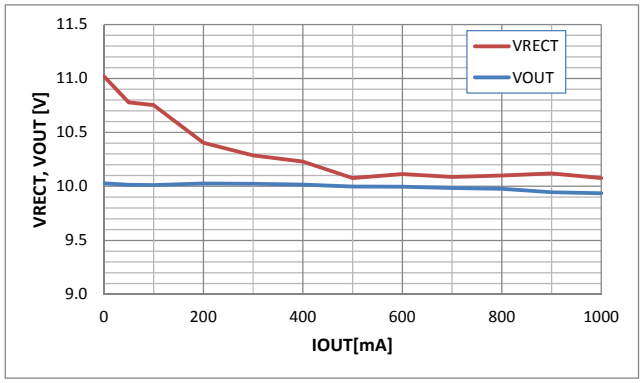


Figure 35. VRECT, VOUT vs IOUT
EPP mode: OUT=10V

(Measurement condition)
TX = ROHM BD57020MWV (MP A1)
RX side thickness = 1.3mm (Acrylic board)
Coil position = Center
Battery on Rx = None

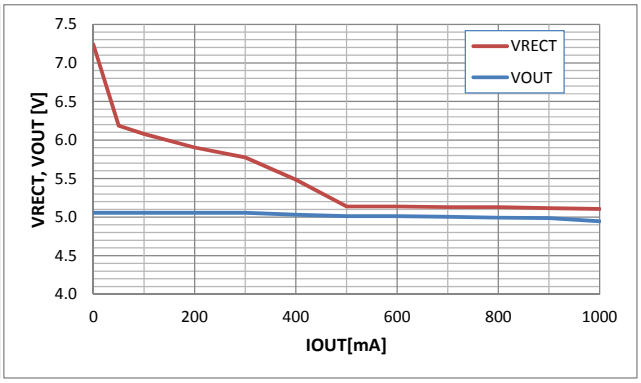


Figure 36. VRECT, VOUT vs IOUT
BPP mode: OUT=5V

(Measurement condition)
TX = ROHM BD57021MWV (LP A11)
RX side thickness = 1.3mm (Acrylic board)
Coil position = Center
Battery on Rx = None

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31.1.5 System Efficiency Performance

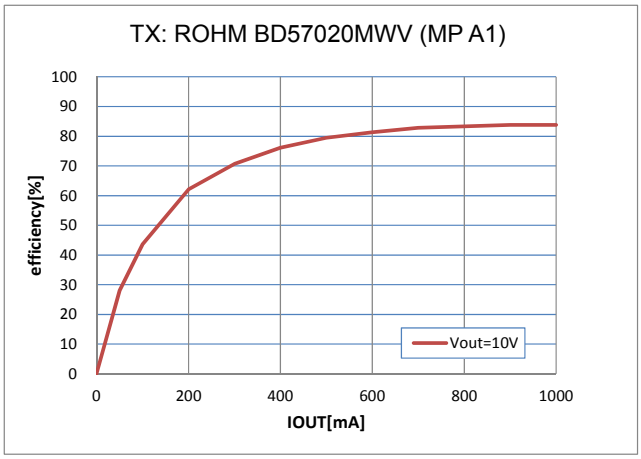

Figure 37(a). Efficiency vs IOUT using MP A1 EPP mode

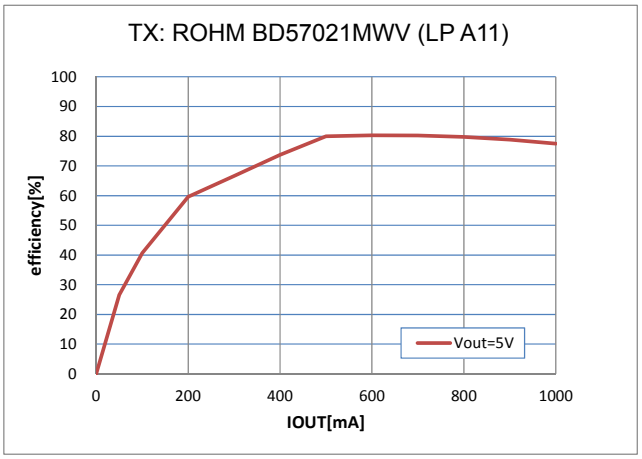

Figure 37(b). Efficiency vs IOUT using LP A11 BPP mode

(Measurement condition)
Tx = ROHM BD57020/21MWV (MP A1/LP A11)
Rx side thickness = 1.3mm (Acrylic board)
Coil position = Center
Battery on Rx = None

$$\eta = \frac{Vout \times Iout}{Vin \times Iin}[\%]$$

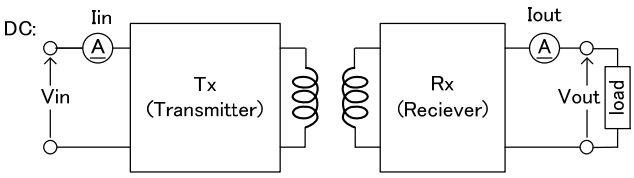

Figure 38. Measurement circuit

31.1.6 System Thermal Performance

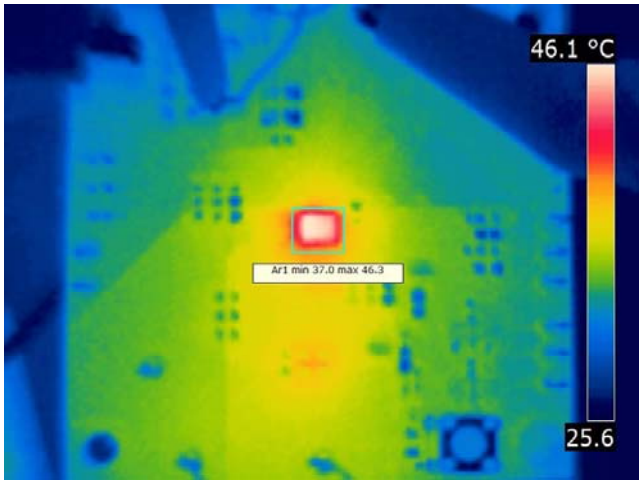

Figure 39. Temperature measured by Thermal Imager FLIR-E49001
EPP mode: OUT=10V, 1A

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31.1.7 Completion of Negotiation and LDO output

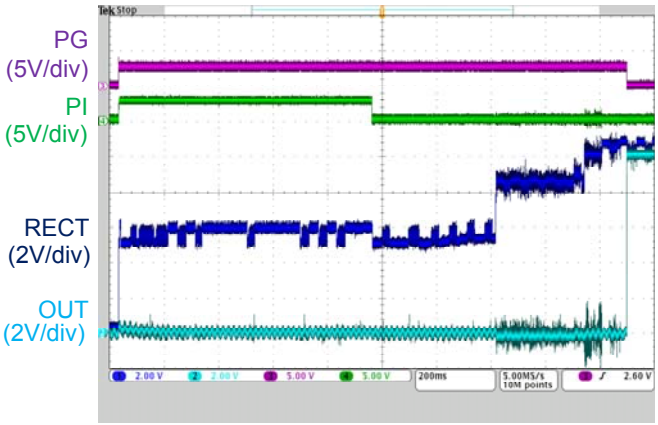

Figure 40. PI pin and OUT pin behavior

"PI" pin turns "L" after the Negotiation phase.

"PG" pin turns "L" after OUT enable.

31.1.8 End Power Transfer

31.1.8.1 Charge Complete (0x01)

"EN1" pin is changed from "L" to "H" to send this EPT.

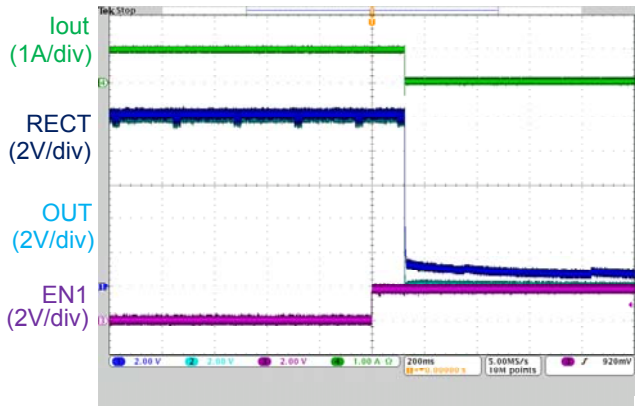

Figure 41. EN1 pin behavior

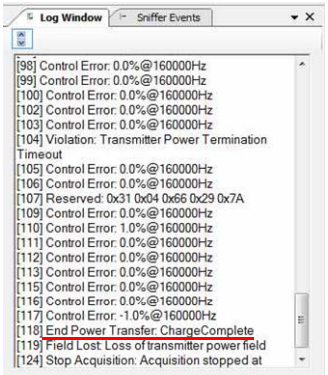

Figure 42. Log File :EPT: Charge Complete

31.1.8.2 Over Temperature (0x03)

"CTRL" pin is changed from "L" to "H" to send this EPT.

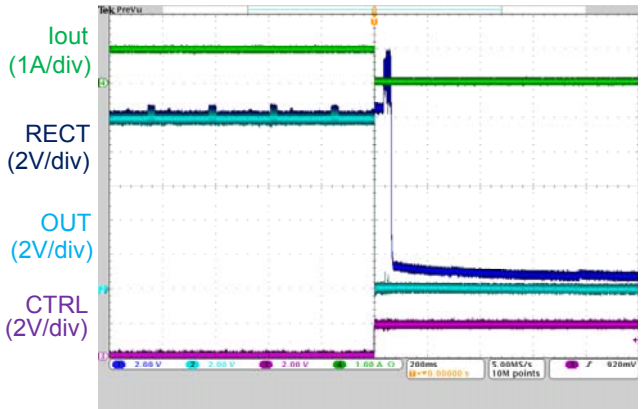

Figure 43. CTRL pin behavior

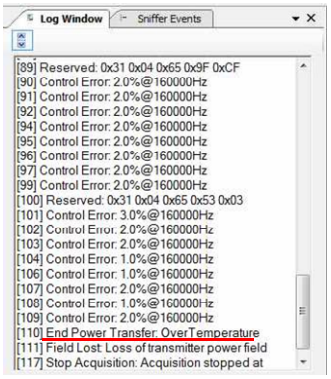

Figure 44. Log File :EPT: Over Temperature

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31.1.8.3 Unknown (0x00)

"ADDET" pin is changed from 0V to 5V to send this EPT.

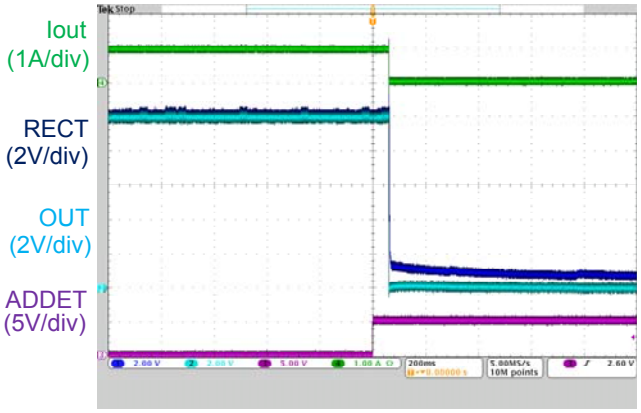


Figure 45. ADDET pin behavior

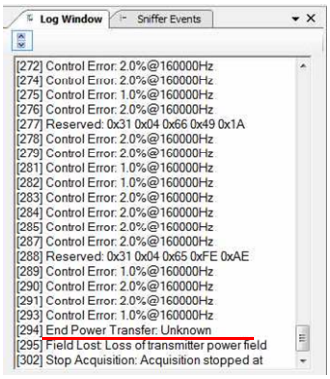
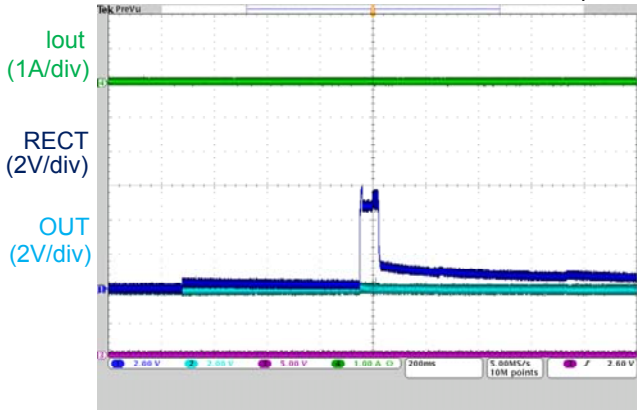


Figure 46. Log File :EPT: Unknown

31.1.8.4 Internal Fault (0x02)

"OUTSET", "ILIMSET", "FOD", or "FOD2" pin is shorted to GND to send this EPT.



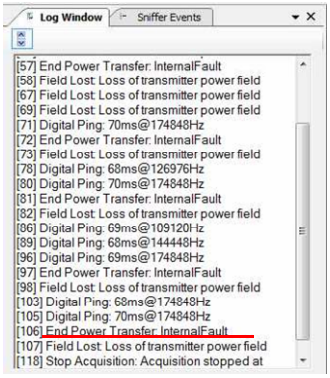


Figure 47. OUTSET, ILIMSET, FOD, or FOD2 pin behavior Figure 48. Log File :EPT: Internal Fault

31.1.9 OUT Voltage vs Temp

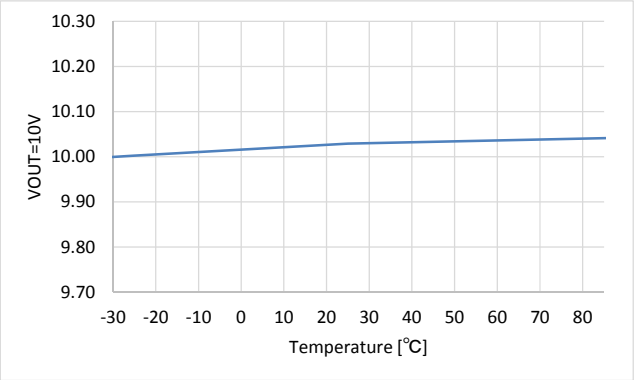


Figure 49. VOUT=10V [V] vs Temperature. [°C]

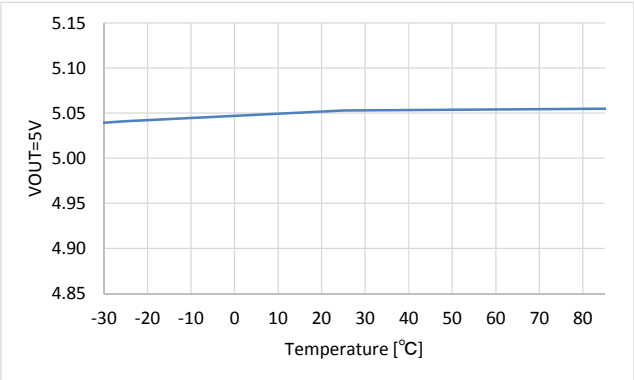


Figure 50. VOUT=5V [V] vs Temperature. [°C]

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32. Instructions in the wireless power supply system

When developing a product for the Qi / PMA certification, a compliance test for each standard is required for every product. When a compliance test is PASSED it does not guarantee all potential products will pass.

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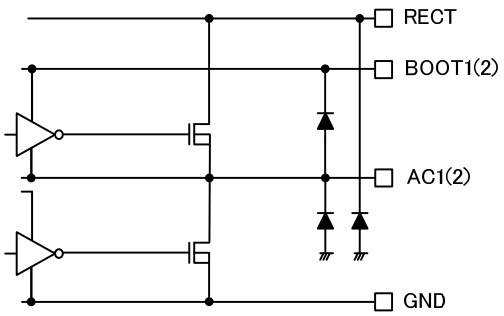
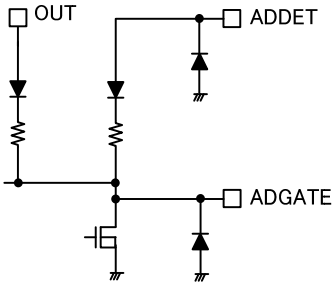
Input/ Output Equivalence Circuit

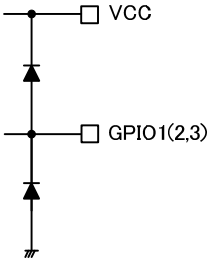
RECT, AC1(2), BOOT1(2), GND pin



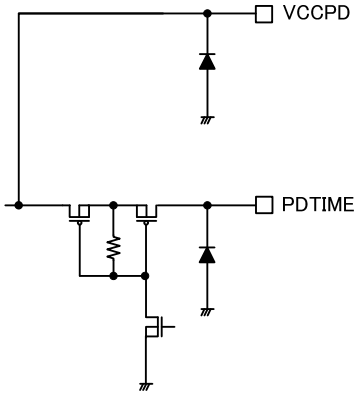
ADDET, ADGATE pin



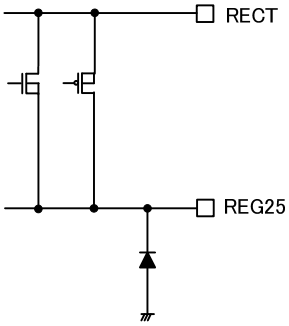
VCC,GPIO1(2,3) pin



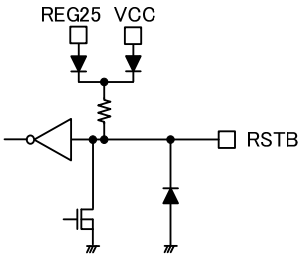
VCCPD,PDTIME pin



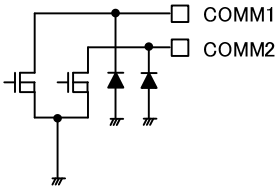
REG25 pin



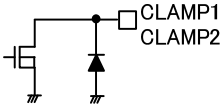
RSTB pin



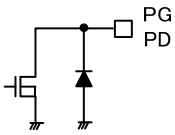
COM1, COM2 pin



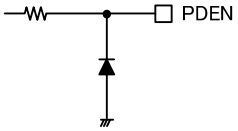
CLAMP1, CLAMP2 pin



PG,PD pin



PDEN pin



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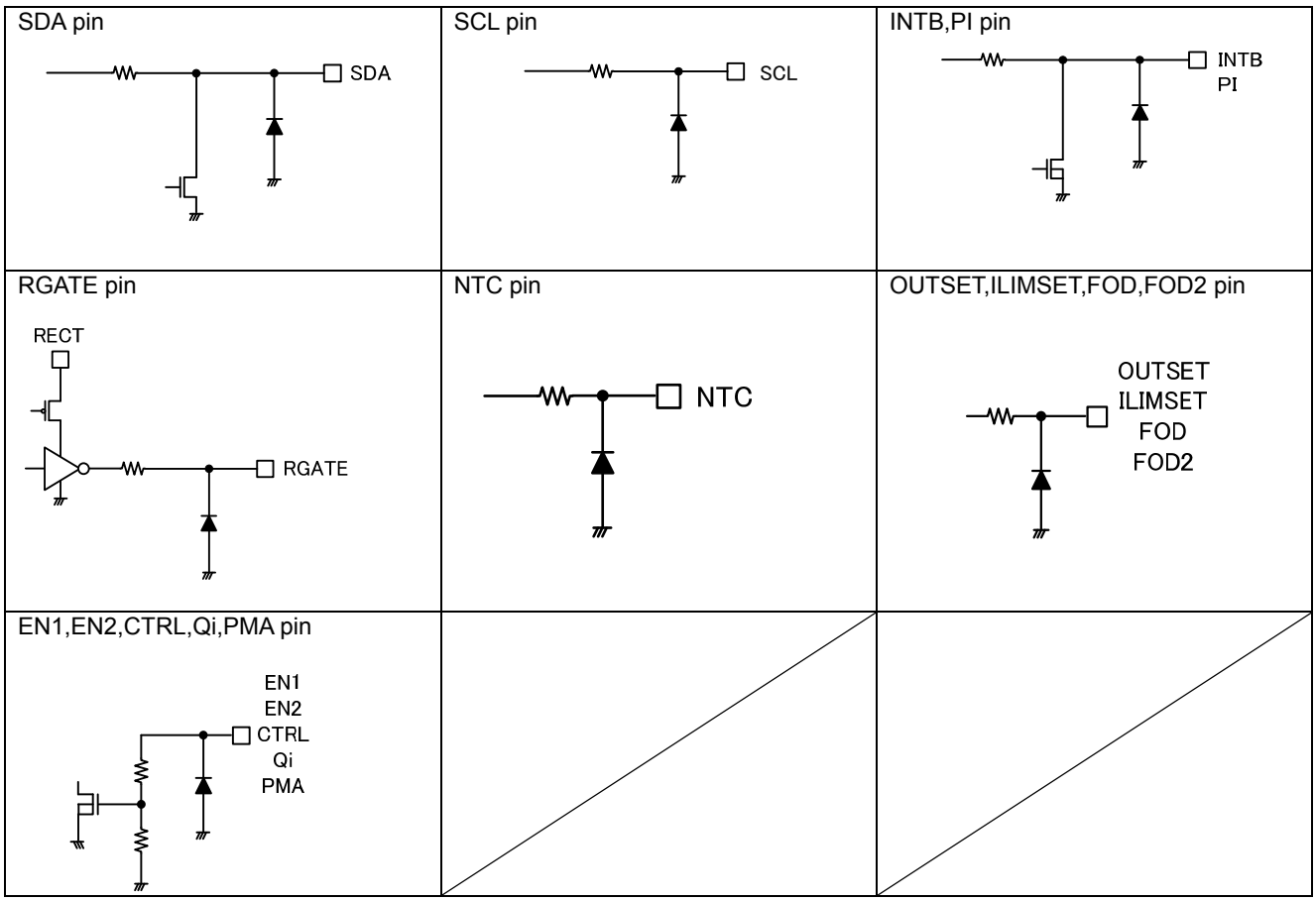
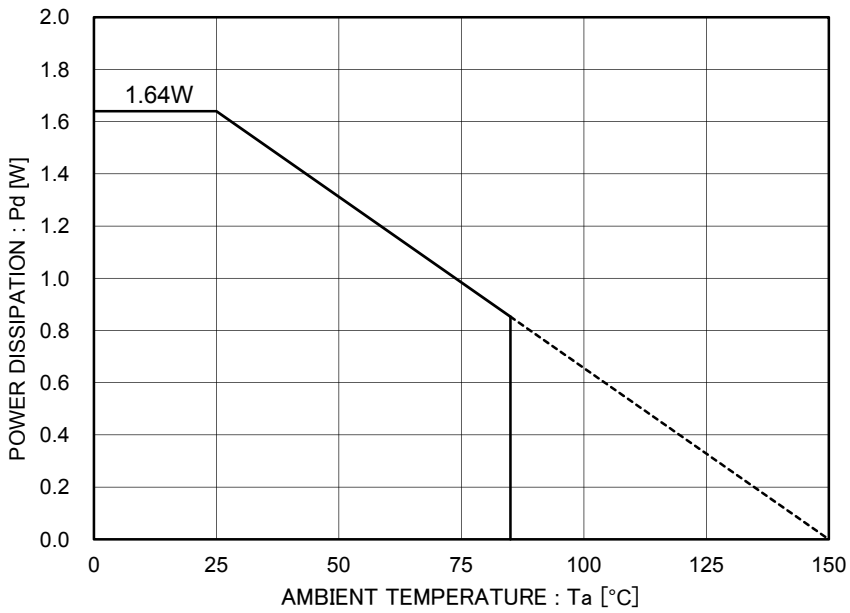


Thermal/Heat loss
(UCSP50L4C Package)
Please allow a sufficient margin by taking into account the permissible power dissipation (Pd) in actual operating conditions.



* 54mm x 62mm x 1.6mm Glass Epoxy Board

Figure 51. Power Dissipation Curve (Pd-Ta Curve)

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Operation Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However only for AC1, AC2, COM1, COM2, CLAMP1, and CLAMP2 pins these pins is inapplicable.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

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Operational Notes – continued

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

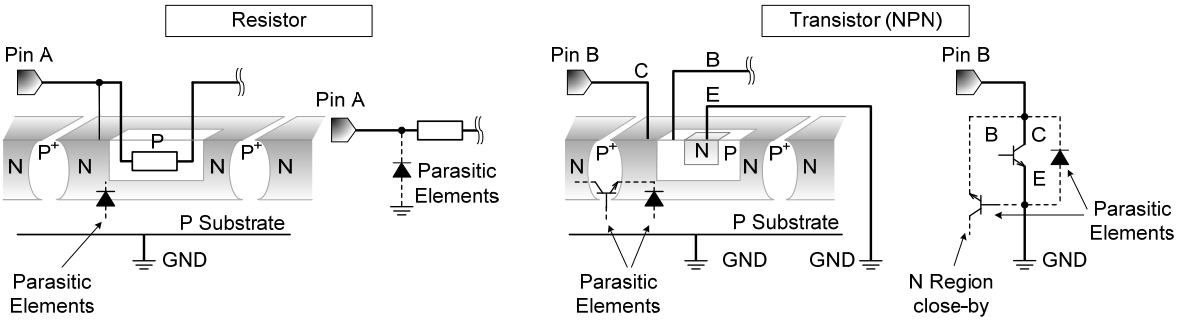

Figure 52. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

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Operational Notes – continued

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. The IC should be powered down and turned ON again to resume normal operation because the TSD circuit keeps the outputs at the OFF state even if the TJ falls below the TSD threshold.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

17. Disturbance light

In a device where a portion of silicon is exposed to light such as in a WL-CSP, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

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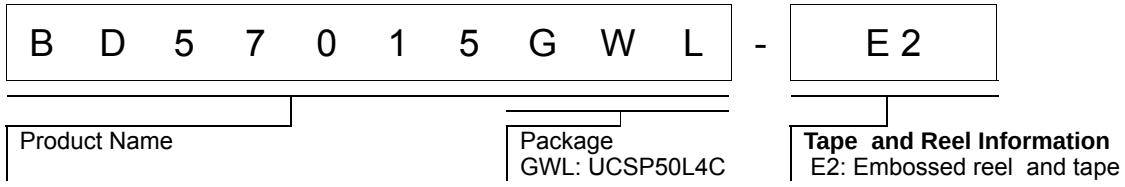
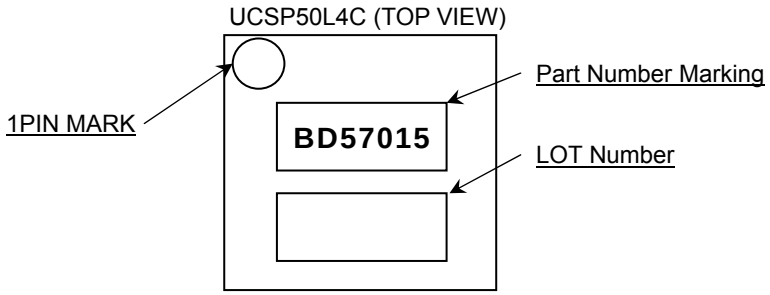
Ordering Information



Marking Diagram



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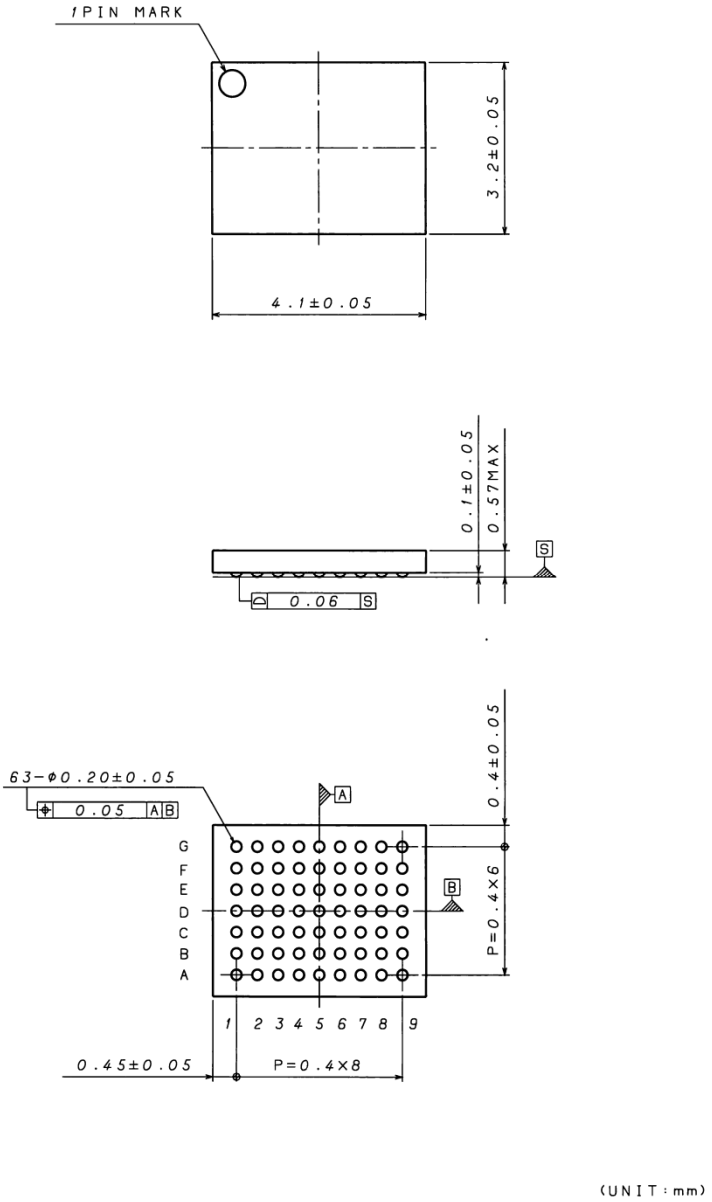
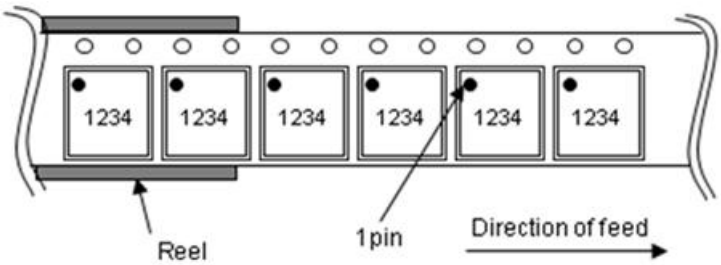
Package Name



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2,500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



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Revision History

Date	Revision.	Page	Modification Content
30.Mar.2016	001	-	New Release
6.Mar.2017	002	1,7,9,10, 19,29,34, 38,41, 46 to 49, 51 to 54	The terms “Low Power” and “Medium Power” have been replaced in the current Qi specification by the terms “BPP(Baseline Power Profile)” and “EPP(Extended Power Profile)”. In addition the registor name of address 0x0E have been changed from “MID_MODE” to “EPP_MODE”.
		3	Regarding the Conditions of “OUT Terminal Output Voltage 1” for LDO Block, VOUT value have been corrected “7.0V” from “5.0V”.
		14	If ILIMSET pin is shorted to GND, BD57015GWL send NoCh signal repeatedly, then the charging is not started in PMA mode.
		15	If FOD and FOD2 pin is shorted to GND, BD57015GWL send NoCh signal repeatedly, then the charging is not started in PMA mode.
		18	Update of the description of register for FOD function and additional EPP setting.
		21	If OUTSET pin is shorted to GND, BD57015GWL send NoCh signal repeatedly, then the charging is not started in PMA mode.
		-	Correction of typo.

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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