

## 1. General description

PTN36001 is a small, low power SuperSpeed USB 3.0 redriver IC that enhances signal quality by performing receive equalization on the deteriorated input signal followed by transmit de-emphasis maximizing system link performance for mobile applications. With its superior differential signal conditioning and enhancement capability, the device delivers significant flexibility and performance scaling for various systems with different PCB trace and cable channel conditions.

PTN36001 is a dual-channel device that supports data signaling rate of 5 Gbit/s through each channel. The data flow of one channel is facing the USB host, and another channel is facing the USB peripheral or device. Each channel consists of a high-speed Transmit (Tx) differential lane and a high-speed Receive (Rx) differential lane.

PTN36001 is powered from a 1.8 V supply and is available in a small X2QFN12 package (1.25 mm × 2.1 mm × 0.35 mm) with 0.4 mm pitch.

## 2. Features and benefits

- Supports USB 3.0 specification (SuperSpeed only)
- Compliant to SuperSpeed USB 3.0 standard
- Support of two channels
- Two control pins to select optimized signal conditions
  - ◆ Receive equalization on each channel to recover from InterSymbol Interference (ISI) and high-frequency losses, with provision to choose equalization gain settings per channel
  - ◆ Transmit de-emphasis on each channel delivers pre-compensation suited to channel conditions
  - ◆ Output swing adjustment
- Integrated termination resistors provide impedance matching on both transmit and receive sides
- Automatic receiver termination detection
- Low active power: 200 mW/111 mA (typical) for  $V_{DD} = 1.8$  V



- Power-saving states:
  - ◆ 5.4 mW/3 mA (typical) when in U2/U3 states
  - ◆ 3.6 mW/2 mA (typical) when no connection detected
  - ◆ 10.8  $\mu$ W/6  $\mu$ A (typical) when in Deep power-saving state
- Excellent differential and common return loss performance
  - ◆ 10 dB differential and 10 dB common-mode return loss for 10 MHz to 1250 MHz
- Flow-through pinout to ease PCB layout and minimize crosstalk effects
- Hot Plug capable
- Power supply:  $V_{DD} = 1.8$  V (typical)
- Compliant with JESD 78 Class II
- Very thin X2QFN12 package: 1.25 mm  $\times$  2.1 mm  $\times$  0.35 mm, 0.4 mm pitch
- ESD protection exceeds 7000 V HBM per JDS-001-2012 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Operating temperature range: 0 °C to 85 °C

### 3. Applications

- Laptops, tablets
- Active cables
- Notebook/netbook/nettop platforms
- Docking stations and AIO platforms
- USB 3.0 peripherals such as flat panel display, consumer/storage devices, printers or USB 3.0 capable hubs/repeaters

### 4. System context diagrams

[Figure 1](#) illustrates PTN36001 usage.

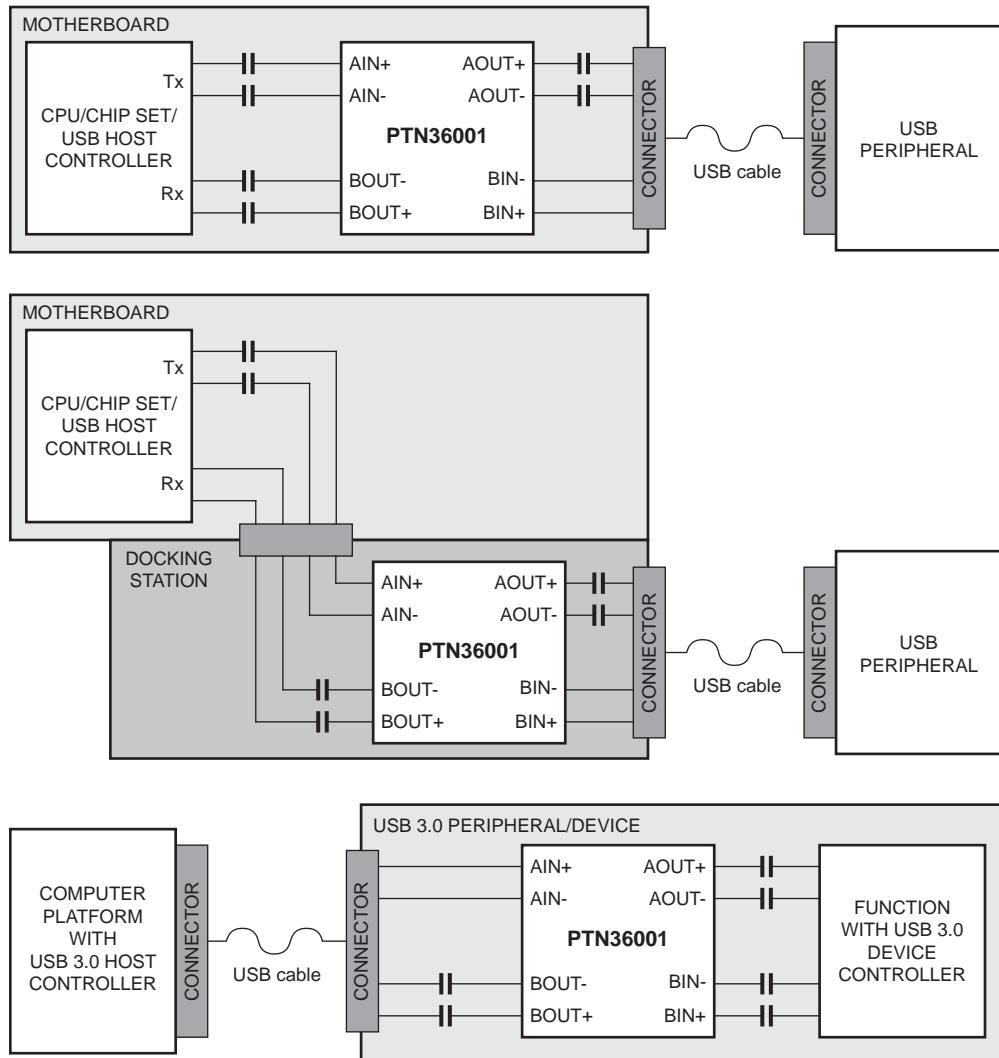


Fig 1. PTN36001 context diagrams

## 5. Ordering information

Table 1. Ordering information

| Type number | Topside marking | Package |  |  | Version   |
|-------------|-----------------|---------|--|--|-----------|
|             |                 | Name    | Description  |  |           |
| PTN36001HX  | 001             | X2QFN12 | plastic, super thin quad flat package; no leads; 12 terminals; body $1.25 \times 2.10 \times 0.35$ mm; 0.4 mm lead pitch |  | SOT1408-1 |

### 5.1 Ordering options

Table 2. Ordering options

| Type number | Orderable part number | Package | Packing method                     | Minimum order quantity | Temperature                              |
|-------------|-----------------------|---------|------------------------------------|------------------------|--|
| PTN36001HX  | PTN36001HXZ           | X2QFN12 | REEL 7" Q1/T1<br>*STANDARD MARK DP | 6000                   | $T_{amb} = 0^{\circ}C$ to $+85^{\circ}C$ |

## 6. Block diagram

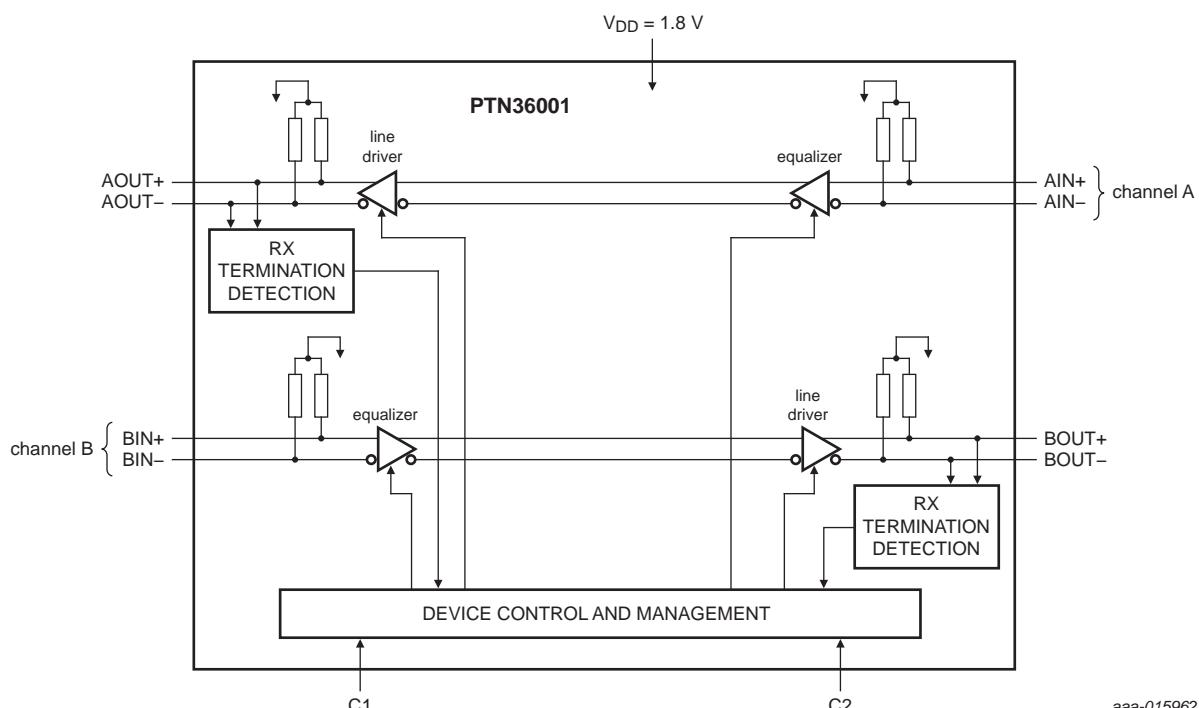


Fig 2. Block diagram of PTN36001

## 7. Pinning information

### 7.1 Pinning

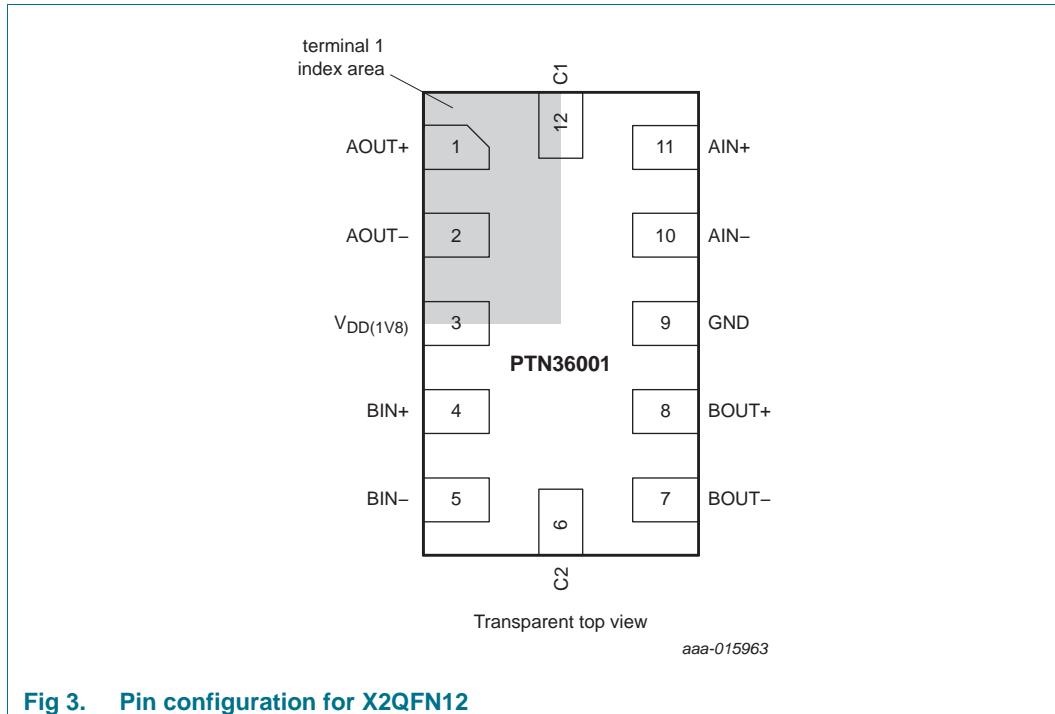


Fig 3. Pin configuration for X2QFN12

### 7.2 Pin description

Table 3. Pin description

| Symbol                                   | Pin | Type                             | Description  |
|--|-----|----------------------------------|--|
| <b>Configuration and control signals</b> |     |                                  |  |
| C1                                       | 12  | Ternary input                    | C1 controls traces on the left side (as shown in <a href="#">Figure 2</a> ) of the redriver — AOUT-/AOUT+ and BIN-/BIN+.<br>C1 controls setting of AOUT+/AOUT- output swing and de-emphasis and BIN-/BIN+ equalization.  |
| C2                                       | 6   | Ternary input                    | C2 controls traces on the right side (as shown in <a href="#">Figure 2</a> ) of the redriver — BOUT-/BOUT+ and AIN-/AIN+.<br>C2 controls setting of BOUT+/BOUT- output swing and de-emphasis and AIN-/AIN+ equalization. |
| <b>High-speed differential signals</b>   |     |                                  |  |
| AIN+                                     | 11  | self-biasing differential input  | Differential signal from SuperSpeed USB 3.0 transmitter. AIN+ makes a differential pair with AIN-. The input to this pin must be AC-coupled externally.  |
| AIN-                                     | 10  | self-biasing differential input  | Differential signal from SuperSpeed USB 3.0 transmitter. AIN- makes a differential pair with AIN+. The input to this pin must be AC-coupled externally.  |
| AOUT+                                    | 1   | self-biasing differential output | Differential signal to SuperSpeed USB 3.0 receiver. AOUT+ makes a differential pair with AOUT-. The output of this pin must be AC-coupled externally.  |

**Table 3. Pin description ...continued**

| Symbol                   | Pin | Type                             | Description   |
|--------------------------|-----|----------------------------------|---|
| AOUT–                    | 2   | self-biasing differential output | Differential signal to SuperSpeed USB 3.0 receiver. AOUT– makes a differential pair with AOUT+. The output of this pin must be AC-coupled externally.   |
| BIN+                     | 4   | self-biasing differential input  | Differential signal from SuperSpeed USB 3.0 transmitter. BIN+ makes a differential pair with BIN–. The input to this pin must be AC-coupled externally. |
| BIN–                     | 5   | self-biasing differential input  | Differential signal from SuperSpeed USB 3.0 transmitter. BIN– makes a differential pair with BIN+. The input to this pin must be AC-coupled externally. |
| BOUT+                    | 8   | self-biasing differential output | Differential signal to SuperSpeed USB 3.0 receiver. BOUT+ makes a differential pair with BOUT–. The output of this pin must be AC-coupled externally.   |
| BOUT–                    | 7   | self-biasing differential output | Differential signal to SuperSpeed USB 3.0 receiver. BOUT– makes a differential pair with BOUT+. The output of this pin must be AC-coupled externally.   |
| <b>Power supply</b>      |     |                                  |   |
| V <sub>DD(1V8)</sub>     | 3   | power                            | 1.8 V supply. A 0201 or 0402 size 0.1 $\mu$ F de-coupling capacitor is highly recommended to be placed as close as possible on this pin to GND.         |
| <b>Ground connection</b> |     |                                  |   |
| GND                      | 9   | power                            | Ground.   |

## 8. Functional description

Refer to [Figure 2 “Block diagram of PTN36001”](#).

PTN36001 is a SuperSpeed USB 3.0 redriver meant to be used for signal integrity enhancement on mobile platforms – laptops, tablets, notebooks, hub, A/V displays and peripheral devices, for example. With its high fidelity differential signal conditioning capability and wide configurability, this chip is flexible and versatile enough for use under a variety of system environments. PTN36001 implements ternary control IO logic on C1 and C2 control pins to detect HIGH (connected to VDD), LOW (connected to GND) or left unconnected condition (OPEN).

The following sections describe the individual block functions and capabilities of the device in more detail.

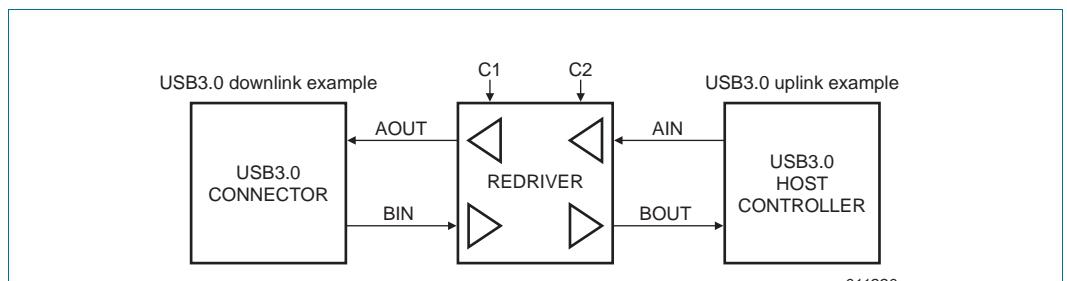
### 8.1 C1 control pin

C1 controls signal traces on the left side (as shown in [Figure 2](#)) of the redriver. It controls the transmit de-emphasis and output swing of AOUT-/AOUT+ channel. It also controls the receive equalization of BIN-/BIN+ channel.

When C1 = HIGH, the left side of the redriver is optimized to drive long trace length of the left Link.

When C1 = OPEN, the left side of the redriver is optimized to drive medium trace length of the left Link.

When C1 = LOW, the left side of the redriver is optimized to drive short trace length of the left Link.



**Fig 4. C1 controls traces on left side of the redriver**

**Table 4. C1 pin controls long/medium/short traces**

| State | Channel type | Pin C1 state | Channel A         |                   |                   |
|-------|--------------|--------------|-------------------|-------------------|-------------------|
|       |              |              | EQ <sup>[1]</sup> | DE <sup>[2]</sup> | OS <sup>[3]</sup> |
| HIGH  | Long         | HIGH         | 9 dB              | -5 dB             | 1.1 V             |
| OPEN  | Medium       | OPEN         | 6 dB              | -3 dB             | 1.0 V             |
| LOW   | Short        | LOW          | 3 dB              | 0 dB              | 0.9 V             |

[1] EQ is the internal input receiver equalization gain at 2.5 GHz.

[2] DE is the internal output signal de-emphasis gain.

[3] OS is the internal transmit output differential voltage swing.

## 8.2 C2 control pin

C2 controls signal traces on the right side with functionality similar to C1.

**Table 5. C2 pin controls long/medium/short traces**

| State | Channel type | Pin C2 state | Channel A         | Channel B         |                   |
|-------|--------------|--------------|-------------------|-------------------|-------------------|
|       |              |              | EQ <sup>[1]</sup> | DE <sup>[2]</sup> | OS <sup>[3]</sup> |
| HIGH  | Long         | HIGH         | 9 dB              | -5 dB             | 1.1 V             |
| OPEN  | Medium       | OPEN         | 6 dB              | -3 dB             | 1.0 V             |
| LOW   | Short        | LOW          | 3 dB              | 0 dB              | 0.9 V             |

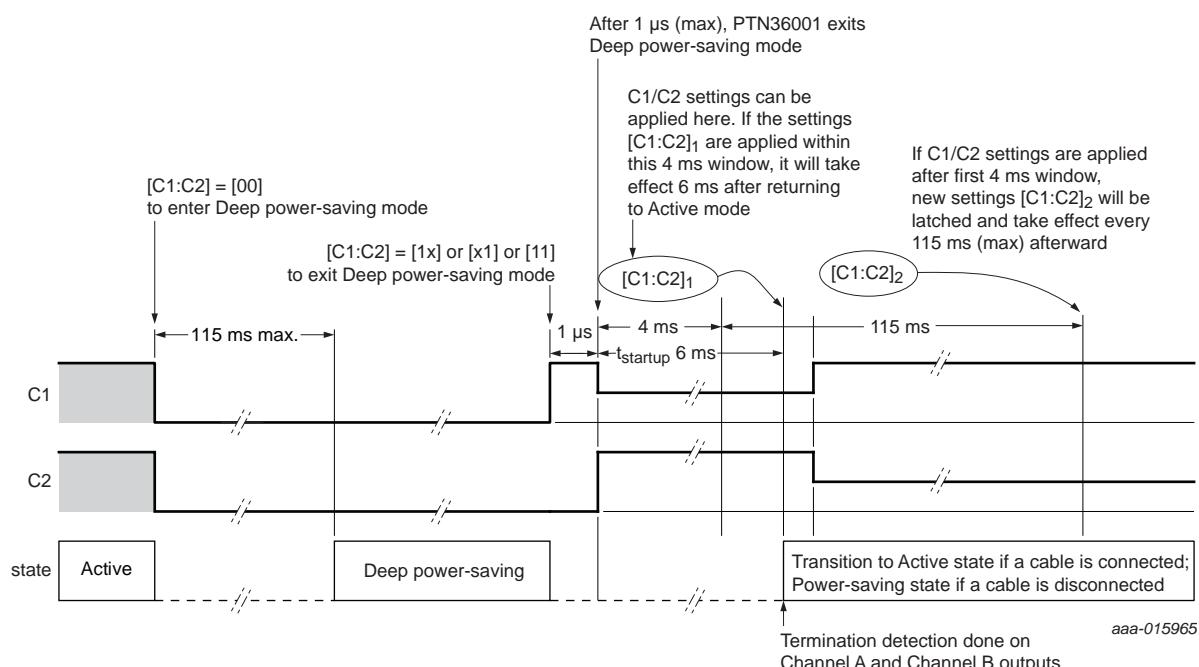
[1] EQ is the internal input receiver equalization gain at 2.5 GHz.

[2] DE is the internal output signal de-emphasis gain.

[3] OS is the internal transmit output differential voltage swing.

## 8.3 Deep power-saving mode entry and exit using C1 and C2 pins

C1 and C2 pins can be controlled by GPIOs from the on-board processor. When C1 and C2 pins are both pulled LOW, it will take up to 115 ms ( $t_{sHL}$ ) for internal logic to sample C1 and C2 pin states, and place the PTN36001 in Deep Power-saving mode. To exit from Deep Power-saving mode, the processor GPIOs should pull up C1 and/or C2 pins to HIGH, and PTN36001 will return back to normal active mode in 1  $\mu$ s. In order for C1/C2 settings to take effect 6 ms ( $t_{SLH}$ ) after PTN36001 returns back to Active mode, C1/C2 settings should be applied within the first 4 ms window. If settings are applied outside this 4 ms window, new C1 and C2 values will be latched and take effect every 115 ms ( $t_{rcfg}$ ). Refer to [Figure 5](#) for Deep Power-saving entry and exit control timing.



**Fig 5. Deep power-saving entry and exit control timing**

## 8.4 C1 and C2 overall control table

Table 6. C1 and C2 control table

| C1   | C2   | EQ                     |           | DE        |           | OS        |           | CE <sup>[1]</sup> |
|------|------|------------------------|-----------|-----------|-----------|-----------|-----------|-------------------|
|      |      | Channel A              | Channel B | Channel A | Channel B | Channel A | Channel B |                   |
| HIGH | HIGH | 9 dB                   | 9 dB      | -5 dB     | -5 dB     | 1.1 V     | 1.1 V     | 1                 |
| HIGH | OPEN | 6 dB                   | 9 dB      | -5 dB     | -3 dB     | 1.1 V     | 1.0 V     | 1                 |
| HIGH | LOW  | 3 dB                   | 9 dB      | -5 dB     | 0 dB      | 1.1 V     | 0.9 V     | 1                 |
| OPEN | HIGH | 9 dB                   | 6 dB      | -3 dB     | -5 dB     | 1.0 V     | 1.1 V     | 1                 |
| OPEN | OPEN | 6 dB                   | 6 dB      | -3 dB     | -3 dB     | 1.0 V     | 1.0 V     | 1                 |
| OPEN | LOW  | 3 dB                   | 6 dB      | -3 dB     | 0 dB      | 1.0 V     | 0.9 V     | 1                 |
| LOW  | HIGH | 9 dB                   | 3 dB      | 0 dB      | -5 dB     | 0.9 V     | 1.1 V     | 1                 |
| LOW  | OPEN | 6 dB                   | 3 dB      | 0 dB      | -3 dB     | 0.9 V     | 1.0 V     | 1                 |
| LOW  | LOW  | Deep power-saving mode |           |           |           |           |           | 0                 |

[1] CE is the internal chip enable signal.

## 8.5 Transmit de-emphasis

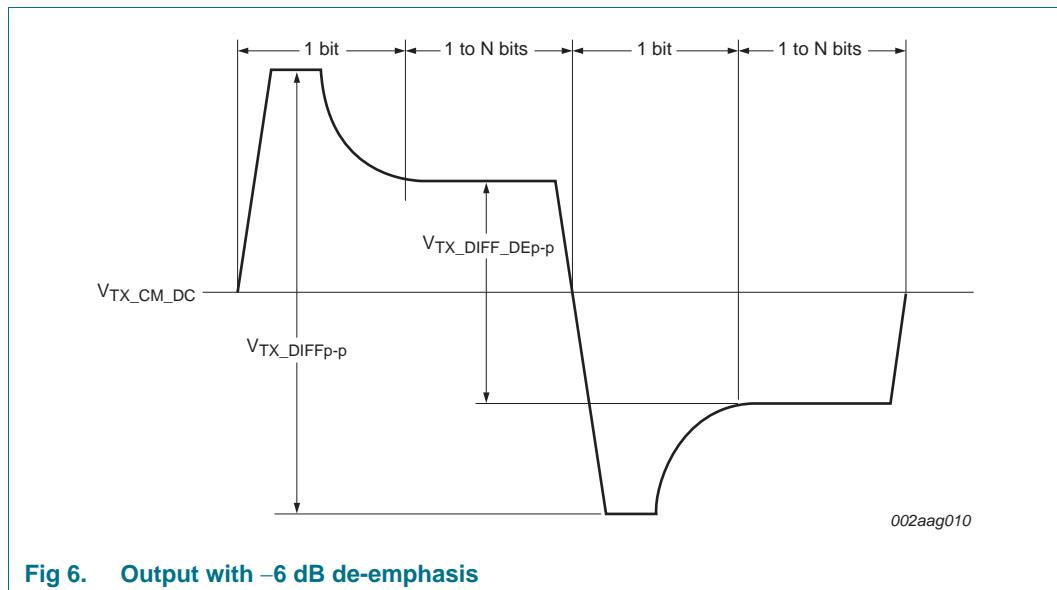


Fig 6. Output with -6 dB de-emphasis

## 8.6 Device states and power management

PTN36001 has implemented an advanced power management scheme that operates in tune with USB 3.0 bus electrical condition. Although the device does not decode USB power management commands (related to USB 3.0 U1/U2/U3 transitions) exchanged between USB 3.0 host and peripheral/device, it relies on bus electrical conditions and control pins/register settings to decide to be in one of the following states:

- **Active state** wherein device is fully operational, USB data is transported on channels A and B. In this state, USB connection exists and the Receive Termination indication remains active. But there is no need for Receive Termination detection.
- **Power-saving state** wherein the channels A and B are kept enabled. In this state, squelching, detection and/or Receive termination detection circuitry are active. Based on USB connection, there are two possibilities:
  - No USB connection.
  - When USB connection exists and when the link is in USB 3.0 U2/U3 mode.
- **Deep power-saving state** wherein both channels' TX and RX terminations are placed in OPEN condition, and the device achieves the most power saving. To enter deep power saving mode, an external GPIO controller can pull down C1 and C2 pins to ground at any time. Please refer to [Section 8.3](#) for Deep power-saving entry and exit control timing information.

As an example of utilizing deep power saving mode to achieve maximum power saving when USB3.0 interface is not active in a device such as a smart phone, the system can use the following scheme as a design guideline to implement the deep power saving mode.

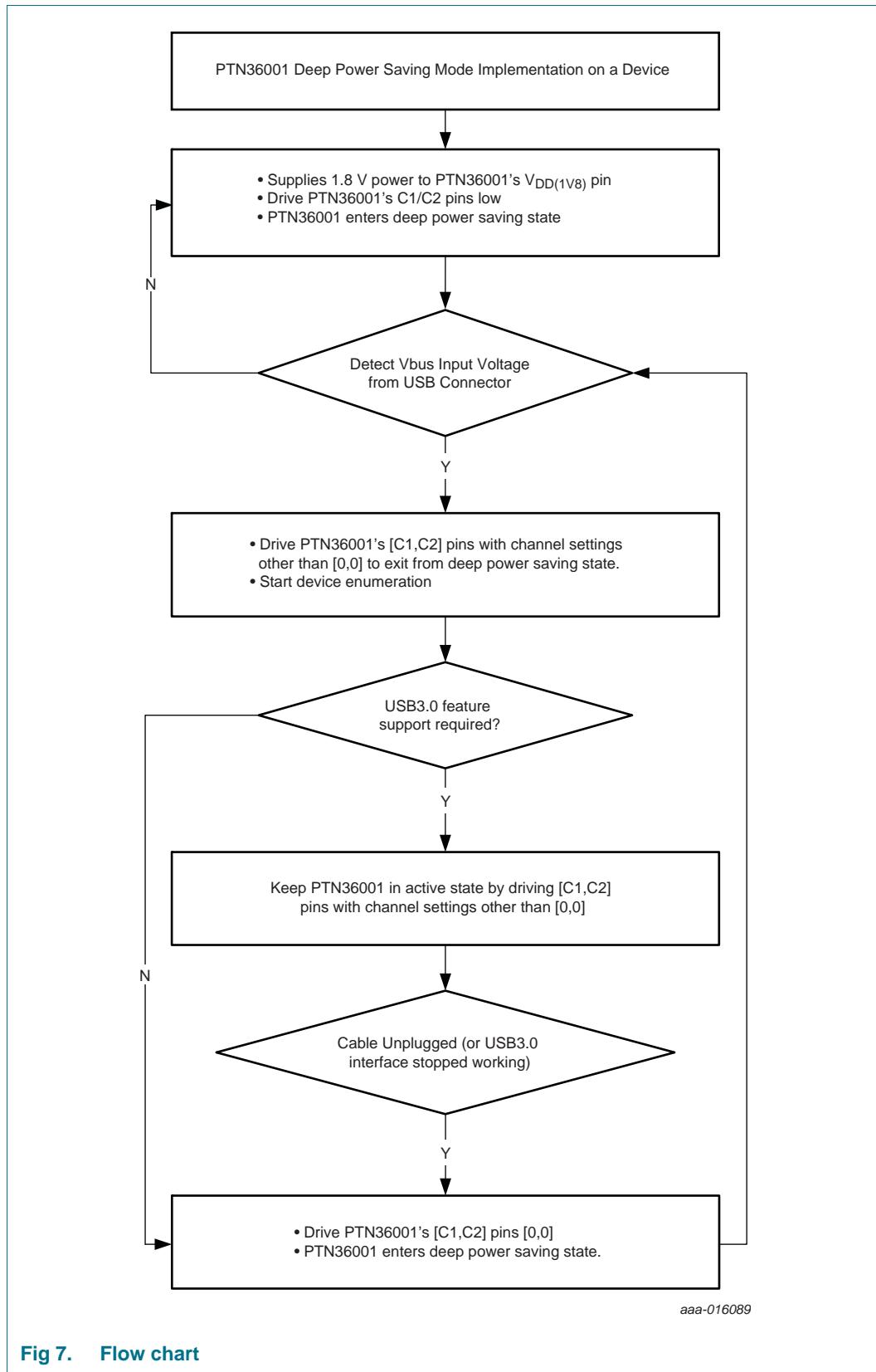


Fig 7. Flow chart

- **Off state:** When PTN36001 is not being powered (i.e.,  $V_{DD1V8} = 0$  V), special steps should be done to prevent back-current issues on C1/C2 pins when these pins' states are not low. C1/C2 pins can be controlled through two different ways.
  - a. pull-up/pull-down resistors - make sure these pull-up resistors'  $V_{DD}$  is the same power source as to power PTN36001. When power to PTN36001 is off, power to these pull-up resistors will be off as well.
  - b. external processor's GPIO - if PTN36001 is turned off when the external processor's power stays on, processor should configure these GPIOs connected to C1/C2 pins as output low ( $< 0.4$  V) or tri-state mode (configure GPIOs as input mode). This will make sure no current will be flowing into PTN36001 through C1/C2 pins.

The Receive termination detection circuitry is implemented as part of a transmitter and detects whether a load device with equivalent DC impedance  $Z_{RX\_DC}$  is present.

## 9. Limiting values

**Table 7. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol        | Parameter                       | Conditions | Min      | Max                 | Unit |
|---------------|---------------------------------|------------|----------|---------------------|------|
| $V_{DD(1V8)}$ | supply voltage (1.8 V)          |            | [1] -0.3 | +2.5                | V    |
| $V_I$         | input voltage                   |            | [1] -0.3 | $V_{DD(1V8)} + 0.5$ | V    |
| $T_{stg}$     | storage temperature             |            | -65      | +150                | °C   |
| $V_{ESD}$     | electrostatic discharge voltage | HBM        | [2] -    | 7000                | V    |
|               |                                 | CDM        | [3] -    | 1000                | V    |

[1] All voltage values (except differential voltages) are with respect to network ground terminal.

[2] Human Body Model: ANSI/ESDA/JEDEC JDS-001-2012 (Revision of ANSI/ESDA/JEDEC JS-001-2011), ESDA/JEDEC Joint standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA; JEDEC Solid State Technology Association, Arlington, VA, USA.

[3] Charged Device Model; JESD22-C101E December 2009 (Revision of JESD22-C101D, October 2008), standard for ESD sensitivity testing, Charged Device Model - Component level; JEDEC Solid State Technology Association, Arlington, VA, USA.

## 10. Recommended operating conditions

**Table 8. Operating conditions**

| Symbol        | Parameter              | Conditions                              | Min  | Typ           | Max                 | Unit |
|---------------|------------------------|---|------|---------------|---------------------|------|
| $V_{DD(1V8)}$ | supply voltage (1.8 V) | 1.8 V supply option                     | 1.7  | 1.8           | 1.9                 | V    |
| $V_I$         | input voltage          | control and configuration pins (C1, C2) | -0.3 | $V_{DD(1V8)}$ | $V_{DD(1V8)} + 0.3$ | V    |
| $T_{amb}$     | ambient temperature    | operating in free air                   | 0    | -             | +85                 | °C   |

## 11. Characteristics

### 11.1 Device characteristics

Table 9. Device characteristics

| Symbol                      | Parameter  | Conditions   | Min | Typ | Max | Unit                 |
|-----------------------------|--|--|-----|-----|-----|----------------------|
| $t_{\text{startup}}$        | start-up time  | between supply voltage within operating range (90 % of $V_{\text{DD}}$ ) until automatic receiver termination detection  | -   | -   | 6   | ms                   |
| $t_{\text{s(LH)}}$          | LOW to HIGH settling time                                  | disable to enable; enable time from 'Deep power-saving mode' ( $C1 = C2 = \text{LOW}$ ) to active modes change; device is supplied with valid supply voltage                               | -   | -   | 6   | ms                   |
| $t_{\text{s(HL)}}$          | HIGH to LOW settling time                                  | enable to disable; disable time from active modes to 'Deep power-saving mode' ( $C1 = C2 = \text{LOW}$ ) change until Deep power-saving mode; device is supplied with valid supply voltage | -   | -   | 115 | ms                   |
| $t_{\text{rcfg}}$           | reconfiguration time                                       | any configuration pin change (from one setting to another setting) to specified operating characteristics; device is supplied with valid supply voltage                                    | -   | -   | 115 | ms                   |
| $t_{\text{PD(dif)}}$        | differential propagation delay                             | between 50 % level at input and output; see <a href="#">Figure 8</a>   | -   | -   | 0.5 | ns                   |
| $t_{\text{idle}}$           | idle time  | default wait time to wait before getting into Power-saving state   | -   | 300 | 400 | ms                   |
| $t_{\text{d(pwrsave-act)}}$ | delay time from power-save to active                       | time for exiting from Power-saving state and get into Active state; see <a href="#">Figure 10</a>  | -   | -   | 115 | $\mu\text{s}$        |
| $t_{\text{d(act-idle)}}$    | delay time from active to idle                             | reaction time for squelch detection circuit; see <a href="#">Figure 9</a>  | -   | 9   | 14  | ns                   |
| $t_{\text{d(idle-act)}}$    | delay time from idle to active                             | reaction time for squelch detection circuit; see <a href="#">Figure 9</a>  | -   | 5   | 11  | ns                   |
| $R_{\text{th(j-a)}}$        | thermal resistance from junction to ambient                | JEDEC still air test environment; value is based on simulation under JEDEC still air test environment with 2S2P(4L) JEDEC PCB  | -   | 92  | -   | $^{\circ}\text{C/W}$ |
| $\Psi_{\text{jt}}$          | junction to top of case thermal characterization parameter | to case top; at ambient temperature of 85 $^{\circ}\text{C}$ ; value is based on simulation under JEDEC still air test environment with 2S2P(4L) JEDEC PCB                                 | -   | 0.5 | -   | $^{\circ}\text{C/W}$ |
| $I_{\text{DD}}$             | supply current   | Active state; $C1 = C2 = \text{OPEN}$ ; Rx equalization gain = 6 dB; Tx output signal swing = 1000 mV (differential peak-to-peak value); Tx de-emphasis = -3.1 dB                          | -   | 111 | -   | mA                   |
|                             |  | U2/U3 Power-saving state   | -   | 3   | -   | mA                   |
|                             |  | no USB connection state  | -   | 2   | -   | mA                   |
|                             |  | Deep power-saving state; $C1 = C2 = \text{LOW}$  | -   | 6   | -   | $\mu\text{A}$        |

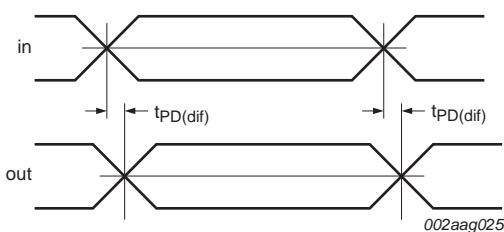


Fig 8. Propagation delay

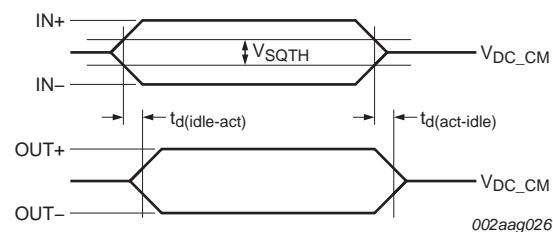


Fig 9. LFPS electrical idle transitions in U0/U1 modes

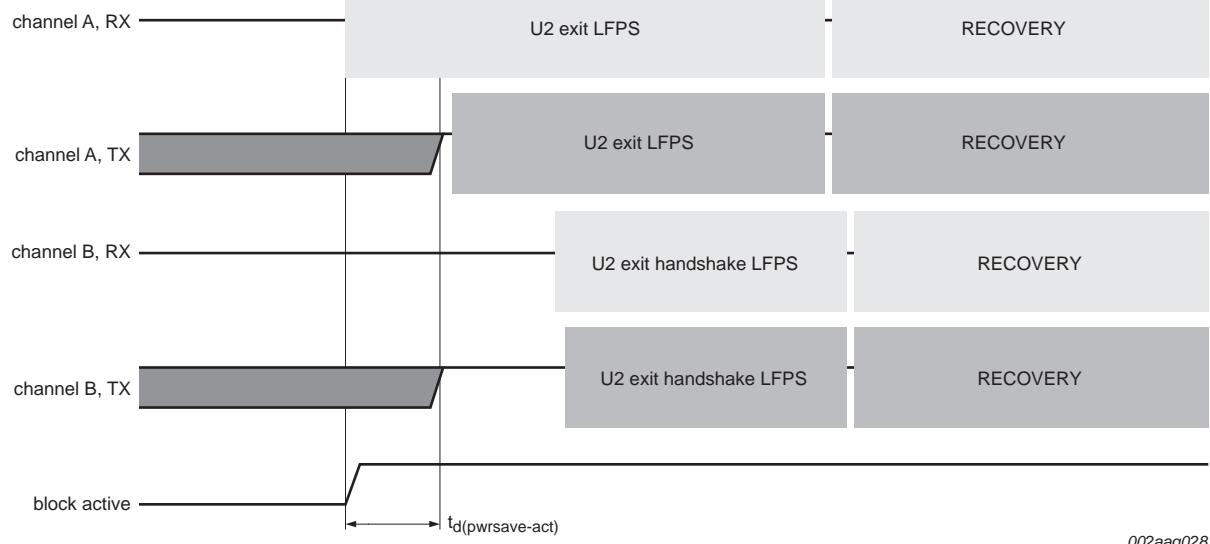


Fig 10. U2/U3 exit behavior

## 11.2 Receiver AC/DC characteristics

**Table 10. Receiver AC/DC characteristics**

| Symbol              | Parameter                                  | Conditions   | Min | Typ | Max  | Unit      |
|---------------------|--|--|-----|-----|------|-----------|
| $Z_{RX\_DC}$        | receiver DC common-mode impedance          |  | 18  | -   | 30   | $\Omega$  |
| $Z_{RX\_DIFF\_DC}$  | DC differential impedance                  | RX pair  | 72  | -   | 120  | $\Omega$  |
| $Z_{RX\_HIGH\_IMP}$ | common-mode input impedance                | DC common-mode input impedance when output of redriver is not terminated | 25  | -   | -    | $k\Omega$ |
| $V_{RX(dif)(p-p)}$  | peak-to-peak differential receiver voltage |  | 100 | -   | 1200 | $mV$      |
| $V_{RX\_DC\_CM}$    | RX DC common mode voltage                  |  | -   | 1.8 | -    | $V$       |
| $V_{RX\_CM\_AC\_P}$ | RX AC common-mode voltage                  | peak   | -   | -   | 150  | $mV$      |
| $V_{th(i)}$         | input threshold voltage                    | differential peak-to-peak value  | 75  | -   | 150  | $mV$      |
| $RL_{DD11,RX}$      | RX differential mode return loss           | 10 MHz to 1250 MHz   | -   | 10  | -    | $dB$      |
|                     |  | 1250 MHz to 2500 MHz   | -   | 8   | -    | $dB$      |
|                     |  | 2500 MHz to 3000 MHz   | -   | 7   | -    | $dB$      |
| $RL_{CC11,RX}$      | RX common mode return loss                 | 10 MHz to 1250 MHz   | -   | 10  | -    | $dB$      |
|                     |  | 1250 MHz to 2500 MHz   | -   | 7   | -    | $dB$      |
|                     |  | 2500 MHz to 3000 MHz   | -   | 6   | -    | $dB$      |

### 11.3 Transmitter AC/DC characteristics

Table 11. Transmitter AC/DC characteristics

| Symbol                    | Parameter  | Conditions   | Min  | Typ  | Max           | Unit      |
|---------------------------|--|--|------|------|---------------|-----------|
| $Z_{TX\_DC}$              | transmitter DC common-mode impedance                         |  | 18   | -    | 30            | $\Omega$  |
| $Z_{TX\_DIFF\_DC}$        | DC differential impedance                                    |  | 72   | -    | 120           | $\Omega$  |
| $V_{TX\_DIFFp\_p}$        | differential peak-to-peak output voltage                     | $R_L = 100 \Omega$   |      |      |               |           |
|                           |  | OS = short channel   | 800  | 900  | 1000          | mV        |
|                           |  | OS = medium channel  | 900  | 1000 | 1100          | mV        |
|                           |  | OS = long channel  | 1000 | 1100 | 1200          | mV        |
| $V_{TX\_DC\_CM}$          | transmitter DC common-mode voltage                           |  | -    | 1.3  | $V_{DD(1V8)}$ | V         |
| $V_{TX\_CM\_ACpp\_ACTIV}$ | TX AC common-mode peak-to-peak output voltage (active state) | device input fed with differential signal                          | -    | -    | 100           | mV        |
| $V_{TX\_IDL\_DIFF\_ACpp}$ | electrical idle differential peak-to-peak output voltage     | when link is in electrical idle                                    | -    | -    | 10            | mV        |
| $t_{W(deemp)TX}$          | transmitter de-emphasis pulse width                          |  | 160  | 175  | 200           | ps        |
| $V_{TX\_RCV\_DETECT}$     | voltage change allowed during receiver detection             | positive voltage swing to sense the receiver termination detection | -    | -    | 600           | mV        |
| $R_{TX\_RCV\_DETECT}$     | TX receiver termination detect charging resistance           | output resistor of the transmitter when it does RX detection       | -    | 3.1  | -             | $k\Omega$ |
| $t_{r(tx)}$               | transmit rise time   | measured using 20 % and 80 % levels; see <a href="#">Figure 11</a> | 40   | 55   | 75            | ps        |
| $t_{f(tx)}$               | transmit fall time   | measured using 80 % and 20 % levels; see <a href="#">Figure 11</a> | 40   | 55   | 75            | ps        |
| $t_{(r-f)tx}$             | difference between transmit rise and fall time               | measured using 20 % and 80 % levels                                | -    | -    | 20            | ps        |
| $RL_{DD11,TX}$            | TX differential mode return loss                             | 10 MHz to 1250 MHz   | -    | 10   | -             | dB        |
|                           |  | 1250 MHz to 2500 MHz   | -    | 7    | -             | dB        |
|                           |  | 2500 MHz to 3000 MHz   | -    | 6    | -             | dB        |
| $RL_{CC11,TX}$            | TX common mode return loss                                   | 10 MHz to 1250 MHz   | -    | 10   | -             | dB        |
|                           |  | 1250 MHz to 2500 MHz   | -    | 7    | -             | dB        |
|                           |  | 2500 MHz to 3000 MHz   | -    | 6    | -             | dB        |

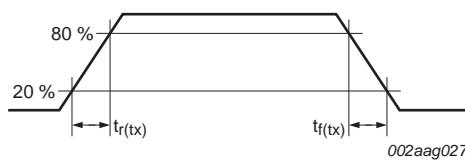


Fig 11. Output rise and fall times

## 11.4 Jitter performance

[Table 12](#) provides jitter performance of PTN36001 under a specific set of conditions that is illustrated by [Figure 8](#).

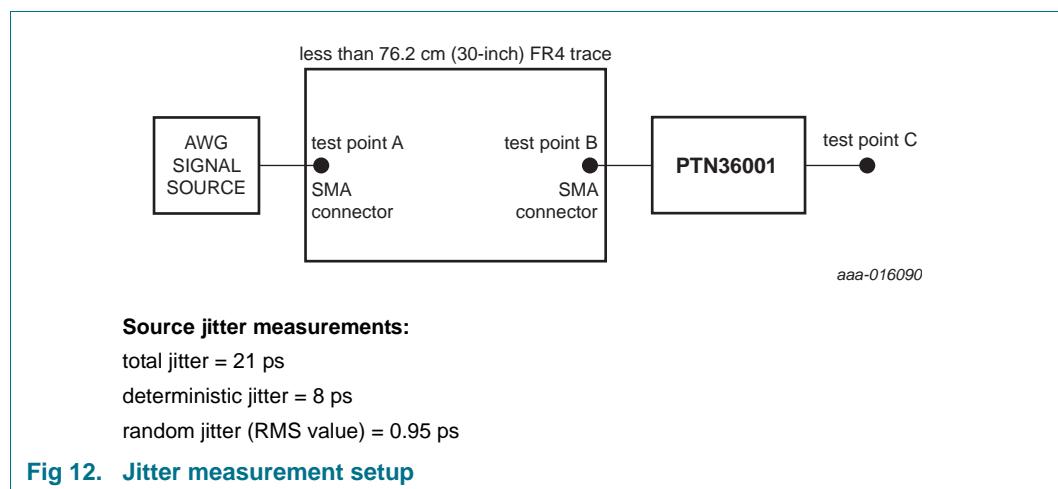
**Table 12. Jitter performance characteristics**

Unit Interval (UI) = 200 ps.

| Symbol                             | Parameter                              | Conditions                   | Min    | Typ | Max  | Unit |    |
|------------------------------------|--|------------------------------|--------|-----|------|------|----|
| $t_{\text{jit}(o)(p-p)}$           | peak-to-peak output jitter time        | total jitter at test point C | [1]    | -   | 0.19 | -    | UI |
| $t_{\text{jit}(\text{dtrm})(p-p)}$ | peak-to-peak deterministic jitter time |                              | [1]    | -   | 0.11 | -    | UI |
| $t_{\text{jit}(\text{rndm})(p-p)}$ | peak-to-peak random jitter time        |                              | [1][2] | -   | 0.08 | -    | UI |

[1] Measured at test point C with K28.5 pattern,  $V_{ID} = 1000$  mV (peak-to-peak), 5 Gbit/s; -3.1 dB de-emphasis from source.

[2] Random jitter calculated as 14.069 times the RMS random jitter for  $10^{-12}$  bit error rate.



## 11.5 Ternary control inputs C1 and C2

**Table 13. Ternary control inputs for C1 and C2 pins**

| Symbol                        | Parameter                   | Conditions   | Min                  | Typ      | Max                  | Unit          |
|-------------------------------|-----------------------------|--|----------------------|----------|----------------------|---------------|
| $V_{IH}$                      | HIGH-level input voltage    | Trigger level of the Schmitt Trigger buffer when input is going from LOW to HIGH | $0.70 \times V_{DD}$ | $V_{DD}$ | $V_{DD} + 0.3$       | V             |
| $V_{IL}$                      | LOW-level input voltage     | Trigger level of the Schmitt Trigger buffer when input is going from HIGH to LOW | -0.3                 | 0        | $0.30 \times V_{DD}$ | V             |
| $R_{pu(\text{ext})}$          | external pull-up resistor   | connected between $VDD1V8$ and setting pin; for detection of HIGH condition      | 0                    | -        | 30                   | k $\Omega$    |
| $R_{pd(\text{ext})}$          | external pull-down resistor | connected between setting pin and GND; for detection of LOW condition            | 0                    | -        | 30                   | k $\Omega$    |
| $Z_{\text{ext}(\text{OPEN})}$ | external impedance          | for detection of OPEN condition  | 250                  | -        | -                    | k $\Omega$    |
| $I_{IL}$                      | LOW-level input current     | setting pin is driven LOW by external GPIO                                       | -45                  | -        | -                    | $\mu\text{A}$ |

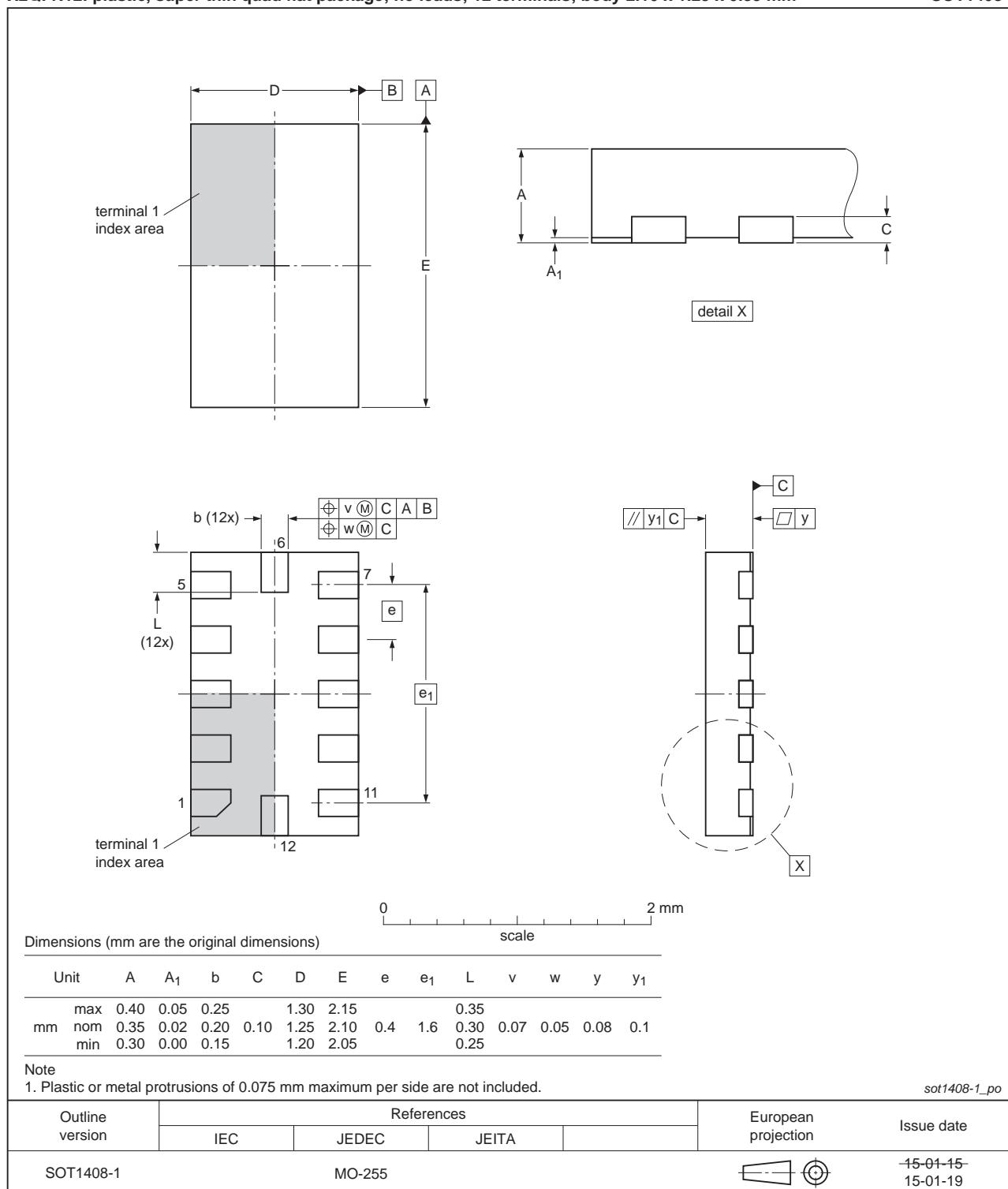
**Table 13. Ternary control inputs for C1 and C2 pins ...continued**

| Symbol           | Parameter                     | Conditions   | Min | Typ | Max | Unit       |
|------------------|-------------------------------|--|-----|-----|-----|------------|
| $I_{IH}$         | HIGH-level input current      | setting pin is driven HIGH (to 1.8 V) by external GPIO     | -   | -   | +45 | $\mu A$    |
| $I_{Lext(OPEN)}$ | external leakage current      | of external GPIO; for reliable detection of OPEN condition | -6  | -   | +6  | $\mu A$    |
| $C_{L(ext)}$     | external load capacitance     | on setting pin; for reliable detection of OPEN condition   | -   | -   | 150 | pF         |
| $R_{pu(int)}$    | internal pull-up resistance   | for detection of Ternary setting                           | -   | 50  | -   | k $\Omega$ |
| $R_{pd(int)}$    | internal pull-down resistance | for detection of Ternary setting                           | -   | 50  | -   | k $\Omega$ |

## 12. Package outline

**X2QFN12: plastic, super thin quad flat package; no leads; 12 terminals; body 2.10 x 1.25 x 0.35 mm**

SOT1408-1

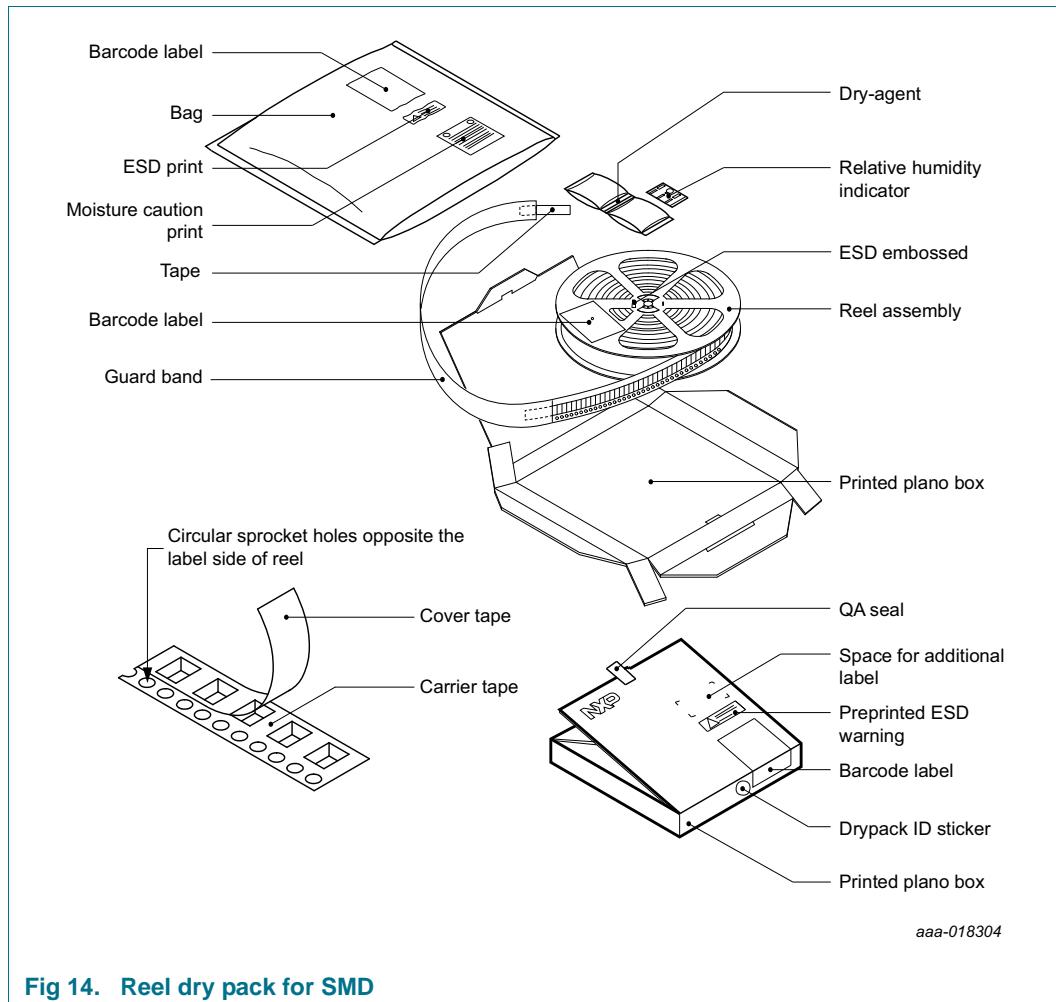


**Fig 13. Package outline SOT1408-1 (X2QFN12)**

## 13. Packing information

### 13.1 SOT1408-1 (X2QFN12); Reel dry pack, SMD, 7"; Q1/T1 standard product orientation; Orderable part number ending ,515 or Z; Ordering code (12NC) ending 515

#### 13.1.1 Packing method



**Table 14. Dimensions and quantities**

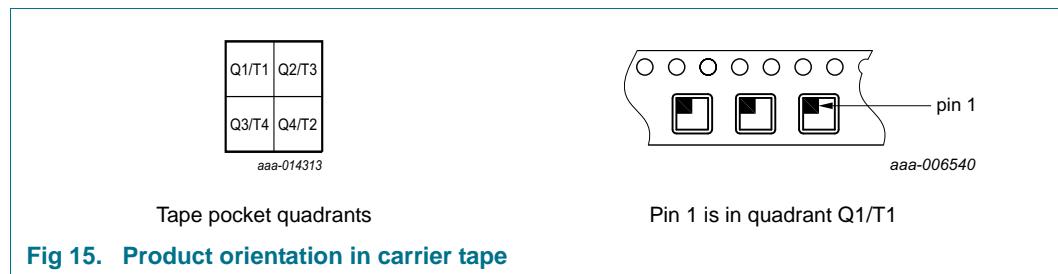
| Reel dimensions<br>d × w (mm) [1] | SPQ/PQ<br>(pcs) [2] | Reels<br>per box | Outer box dimensions<br>l × w × h (mm) |
|-----------------------------------|---------------------|------------------|--|
| 180 × 8                           | 6000                | 1                | 209 × 206 × 34                         |

[1] d = reel diameter; w = tape width.

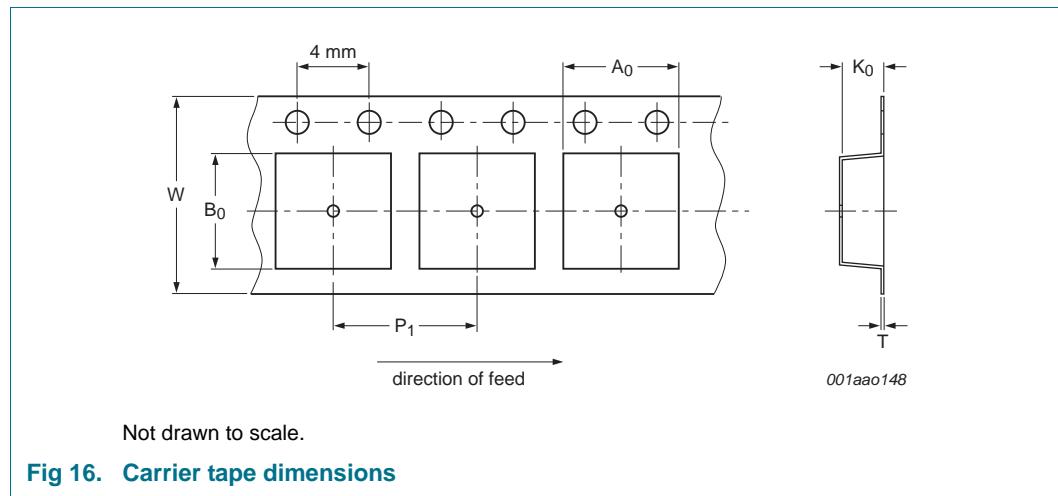
[2] Packing quantity dependent on specific product type.

View ordering and availability details at [NXP order portal](#), or contact your local NXP representative.

### 13.1.2 Product orientation

**Fig 15. Product orientation in carrier tape**

### 13.1.3 Carrier tape dimensions

**Fig 16. Carrier tape dimensions****Table 15. Carrier tape dimensions**

In accordance with IEC 60286-3.

| A <sub>0</sub> (mm) | B <sub>0</sub> (mm) | K <sub>0</sub> (mm) | T (mm)      | P <sub>1</sub> (mm) | W (mm)    |
|---------------------|---------------------|---------------------|-------------|---------------------|-----------|
| 1.55 ± 0.1          | 2.40 ± 0.1          | 0.5 ± 0.05          | 0.25 ± 0.05 | 4.0 ± 0.1           | 8.0 ± 0.3 |

## 13.1.4 Reel dimensions

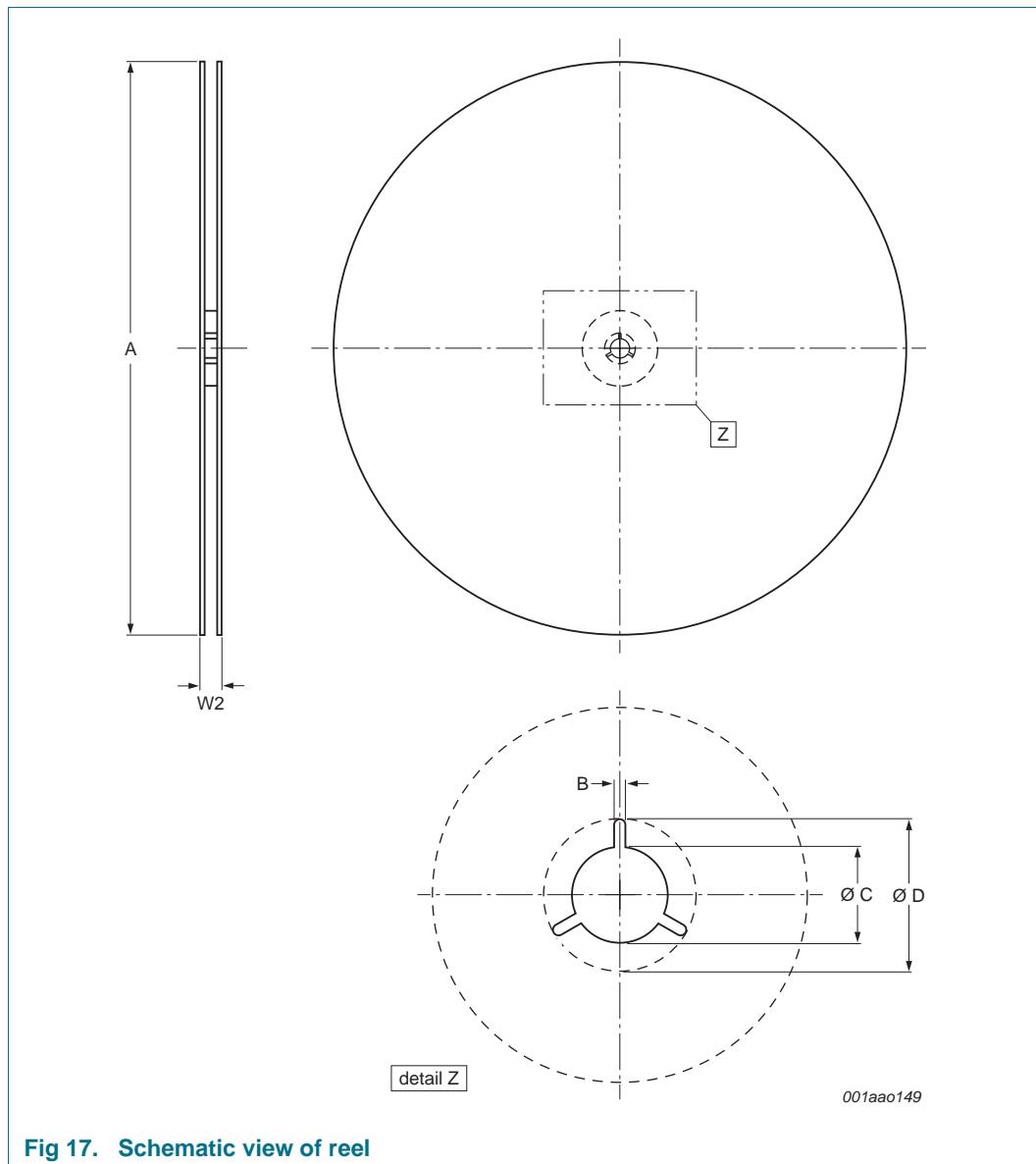


Fig 17. Schematic view of reel

**Table 16. Reel dimensions**  
In accordance with IEC 60286-3.

| A [nom] (mm) | W2 [max] (mm) | B [min] (mm) | C [min] (mm) | D [min] (mm) |
|--------------|---------------|--------------|--------------|--------------|
| 180          | 14.4          | 1.5          | 12.8         | 20.2         |

### 13.1.5 Barcode label

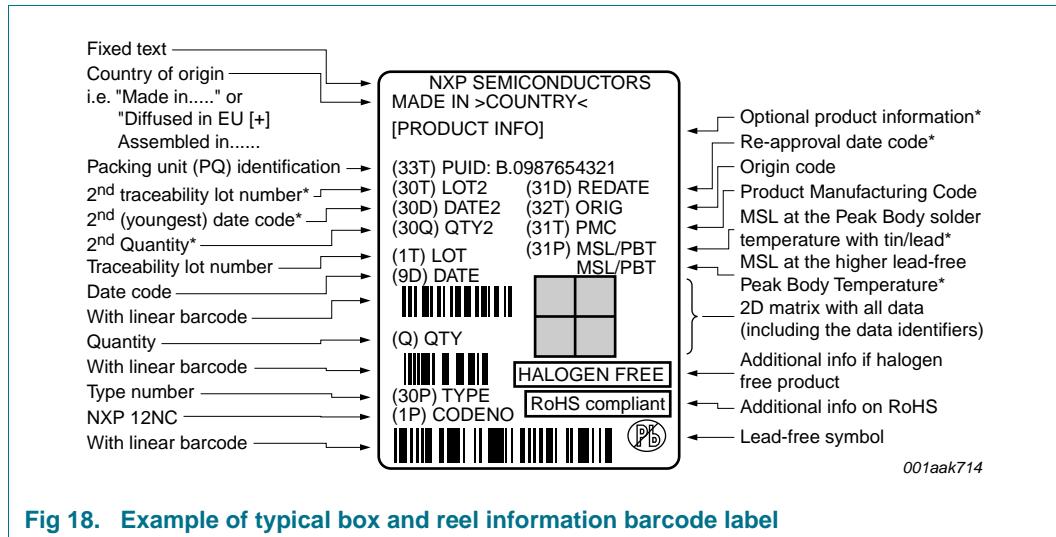


Fig 18. Example of typical box and reel information barcode label

Table 17. Barcode label dimensions

| Box barcode label<br>l × w (mm) | Reel barcode label<br>l × w (mm) |
|---------------------------------|----------------------------------|
| 100 × 75                        | 100 × 75                         |

## 14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note AN10365 “Surface mount reflow soldering description”.

### 14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 19](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 18](#) and [19](#)

**Table 18. SnPb eutectic process (from J-STD-020D)**

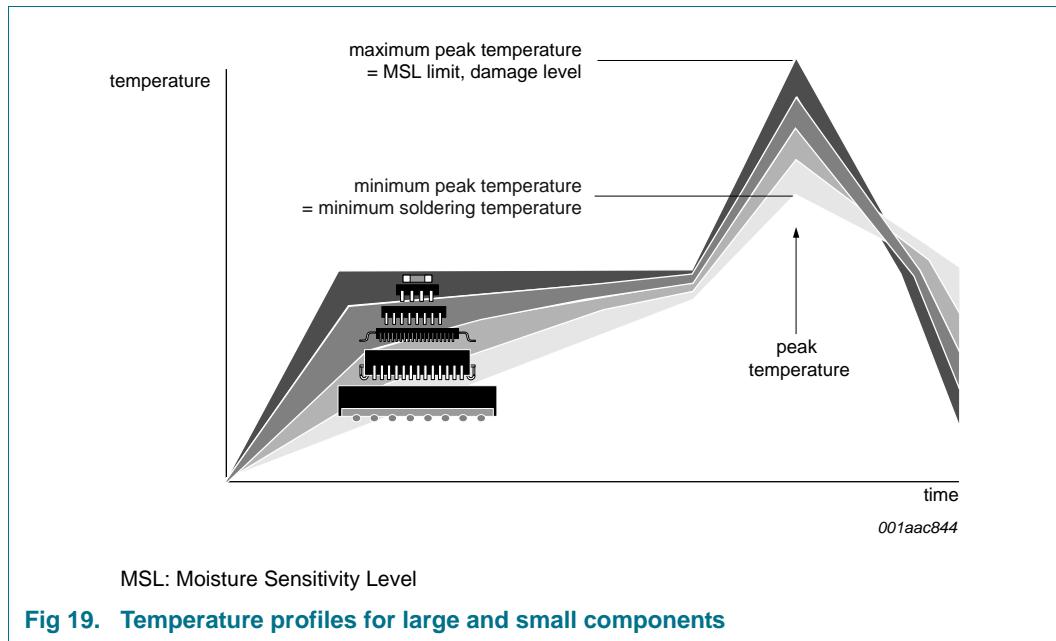
| Package thickness (mm) | Package reflow temperature (°C) |       |
|------------------------|---------------------------------|-------|
|                        | Volume (mm <sup>3</sup> )       |       |
|                        | < 350                           | ≥ 350 |
| < 2.5                  | 235                             | 220   |
| ≥ 2.5                  | 220                             | 220   |

**Table 19. Lead-free process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) |             |        |
|------------------------|---------------------------------|-------------|--------|
|                        | Volume (mm <sup>3</sup> )       |             |        |
|                        | < 350                           | 350 to 2000 | > 2000 |
| < 1.6                  | 260                             | 260         | 260    |
| 1.6 to 2.5             | 260                             | 250         | 245    |
| > 2.5                  | 250                             | 245         | 245    |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 19](#).



For further information on temperature profiles, refer to Application Note AN10365 "Surface mount reflow soldering description".

## 15. Abbreviations

**Table 20. Abbreviations**

| Acronym              | Description                             |
|----------------------|---|
| A/V                  | Audio/Video device                      |
| AIO                  | All In One computer platform            |
| CDM                  | Charged-Device Model                    |
| CMOS                 | Complementary Metal-Oxide Semiconductor |
| ESD                  | ElectroStatic Discharge                 |
| HBM                  | Human Body Model                        |
| I <sup>2</sup> C-bus | Inter-Integrated Circuit bus            |
| I/O                  | Input/Output                            |
| IC                   | Integrated Circuit                      |
| ISI                  | InterSymbol Interference                |
| LFPS                 | Low Frequency Periodic Signaling        |
| PCB                  | Printed-Circuit Board                   |
| RX                   | Receive (or Receiver)                   |
| SI                   | Signal Integrity                        |
| TX                   | Transmit (or Transmitter)               |
| USB                  | Universal Serial Bus                    |

## 16. Revision history

**Table 21. Revision history**

| Document ID    | Release date  | Data sheet status  | Change notice | Supersedes   |
|----------------|---|--------------------|---------------|--------------|
| PTN36001 v.1.1 | 20160816  | Product data sheet | -             | PTN36001 v.1 |
| Modifications: | <ul style="list-style-type: none"><li>Removed 500 piece MOQ</li></ul> |                    |               |              |
| PTN36001 v.1   | 20160413  | Product data sheet | -             | -            |

## 17. Legal information

### 17.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 17.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 17.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products** — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 18. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 19. Contents

|           |  |           |           |                            |           |
|-----------|--|-----------|-----------|----------------------------|-----------|
| <b>1</b>  | <b>General description</b>   | <b>1</b>  | 17.1      | Data sheet status          | 29        |
| <b>2</b>  | <b>Features and benefits</b>   | <b>1</b>  | 17.2      | Definitions                | 29        |
| <b>3</b>  | <b>Applications</b>  | <b>2</b>  | 17.3      | Disclaimers                | 29        |
| <b>4</b>  | <b>System context diagrams</b>   | <b>2</b>  | 17.4      | Trademarks                 | 30        |
| <b>5</b>  | <b>Ordering information</b>  | <b>4</b>  | <b>18</b> | <b>Contact information</b> | <b>30</b> |
| 5.1       | Ordering options   | 4         | <b>19</b> | <b>Contents</b>            | <b>31</b> |
| <b>6</b>  | <b>Block diagram</b>   | <b>4</b>  |           |                            |           |
| <b>7</b>  | <b>Pinning information</b>   | <b>5</b>  |           |                            |           |
| 7.1       | Pinning  | 5         |           |                            |           |
| 7.2       | Pin description  | 5         |           |                            |           |
| <b>8</b>  | <b>Functional description</b>  | <b>7</b>  |           |                            |           |
| 8.1       | C1 control pin   | 7         |           |                            |           |
| 8.2       | C2 control pin   | 8         |           |                            |           |
| 8.3       | Deep power-saving mode entry and exit using C1 and C2 pins   | 8         |           |                            |           |
| 8.4       | C1 and C2 overall control table  | 9         |           |                            |           |
| 8.5       | Transmit de-emphasis   | 9         |           |                            |           |
| 8.6       | Device states and power management   | 10        |           |                            |           |
| <b>9</b>  | <b>Limiting values</b>   | <b>13</b> |           |                            |           |
| <b>10</b> | <b>Recommended operating conditions</b>  | <b>13</b> |           |                            |           |
| <b>11</b> | <b>Characteristics</b>   | <b>14</b> |           |                            |           |
| 11.1      | Device characteristics   | 14        |           |                            |           |
| 11.2      | Receiver AC/DC characteristics   | 16        |           |                            |           |
| 11.3      | Transmitter AC/DC characteristics  | 17        |           |                            |           |
| 11.4      | Jitter performance   | 18        |           |                            |           |
| 11.5      | Ternary control inputs C1 and C2   | 18        |           |                            |           |
| <b>12</b> | <b>Package outline</b>   | <b>20</b> |           |                            |           |
| <b>13</b> | <b>Packing information</b>   | <b>21</b> |           |                            |           |
| 13.1      | SOT1408-1 (X2QFN12); Reel dry pack, SMD, 7"; Q1/T1 standard product orientation; Orderable part number ending ,515 or Z; Ordering code (12NC) ending 515 | 21        |           |                            |           |
| 13.1.1    | Packing method   | 21        |           |                            |           |
| 13.1.2    | Product orientation  | 22        |           |                            |           |
| 13.1.3    | Carrier tape dimensions  | 22        |           |                            |           |
| 13.1.4    | Reel dimensions  | 23        |           |                            |           |
| 13.1.5    | Barcode label  | 24        |           |                            |           |
| <b>14</b> | <b>Soldering of SMD packages</b>   | <b>25</b> |           |                            |           |
| 14.1      | Introduction to soldering  | 25        |           |                            |           |
| 14.2      | Wave and reflow soldering  | 25        |           |                            |           |
| 14.3      | Wave soldering   | 25        |           |                            |           |
| 14.4      | Reflow soldering   | 26        |           |                            |           |
| <b>15</b> | <b>Abbreviations</b>   | <b>27</b> |           |                            |           |
| <b>16</b> | <b>Revision history</b>  | <b>28</b> |           |                            |           |
| <b>17</b> | <b>Legal information</b>   | <b>29</b> |           |                            |           |

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2016.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 16 August 2016

Document identifier: PTN36001

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[NXP](#):

[PTN36001HXAZ](#) [PTN36001HXZ](#)