

Very low capacitance bidirectional ESD protection diode14 October 2016Product data sheet

1. General description

Very low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode designed to protect one signal line from the damage caused by ESD and other transients. The device is housed in a leadless ultra small DFN1006-2 (SOD882) Surface-Mounted Device (SMD) plastic package.

2. Features and benefits

- · Bidirectional ESD protection of one line
- Low diode capacitance C_d = 17 pF
- Rated peak pulse power: P_{PPM} = 290 W
- Ultra low leakage current I_{RM} < 1 nA
- ESD protection up to 30 kV
- IEC 61000-4-2; level 4 (ESD)
- IEC 61000-4-5 (surge); I_{PPM} = 7.8 A
- AEC-Q101 qualified

3. Applications

- · Computers and peripherals
- Audio and video equipment
- Cellular handsets and accessories
- Portable electronics
- Communication systems

4. Quick reference data

Table 1. Quick reference data							
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{RWM}	reverse standoff voltage	T _{amb} = 25 °C		-	-	12	V
C _d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C		-	17	25	pF

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5. Pinning information

Table 2.	Pinning in	ormation		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	К	cathode		
2	к	cathode		sym045
			Transparent top view	
			DFN1006-2 (SOD882)	

6. Ordering information

Table 3. Ordering information						
Type number	Package					
	Name	Description	Version			
PESD12VV1BL	DFN1006-2	DFN1006-2: leadless ultra small plastic package; 2 terminals	SOD882			

7. Marking

Table 4. Marking codes	
Type number	Marking code
PESD12VV1BL	MW

8. Limiting values

Table 5. Limiting values

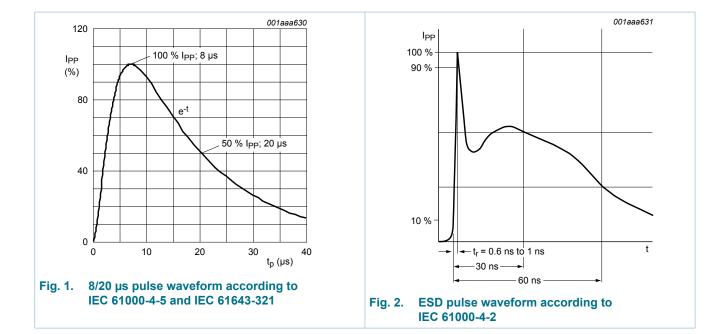
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Мах	Unit
P _{PPM}	rated peak pulse power		[1]	-	290	W
I _{PPM}	rated peak pulse current	t _p = 8/20 μs	[1]	-	7.8	А
Tj	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
ESD maximun	n ratings	·	·	·		
V _{ESD}	electrostatic discharge	IEC 61000-4-2; contact discharge	[2]	-	30	kV
	voltage	machine model		-	400	V
		human body model (MIL-STD-883)		-	10	kV

Device stressed with non-repetitive current pulses (8/20 µs exponential decay waveform according to IEC 61000-4-5 and IEC 61643-321).

[2] Device stressed with ten non-repetitive ESD pulses.

Very low capacitance bidirectional ESD protection diode



9. Characteristics

Table 6. Char	racteristics						
Symbol	Parameter	Conditions		Min	Тур	Мах	Unit
V _{RWM}	reverse standoff voltage	T _{amb} = 25 °C		-	-	12	V
V _{BR}	breakdown voltage	I _R = 5 mA; T _{amb} = 25 °C		14.6	15.7	16.8	V
I _{RM}	reverse leakage current	V _{RWM} = 12 V; T _{amb} = 25 °C		-	1	10	nA
C _d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C		-	17	25	pF
V _{CL}	clamping voltage	I _{PP} = 1 A; T _{amb} = 25 °C	[1]	-	-	22	V
		I _{PPM} = 7.8 A; T _{amb} = 25 °C	[1]	-	-	38	V
R _{dyn}	dynamic resistance	I _R = 10 A; T _{amb} = 25 °C	[2]	-	0.7	-	Ω

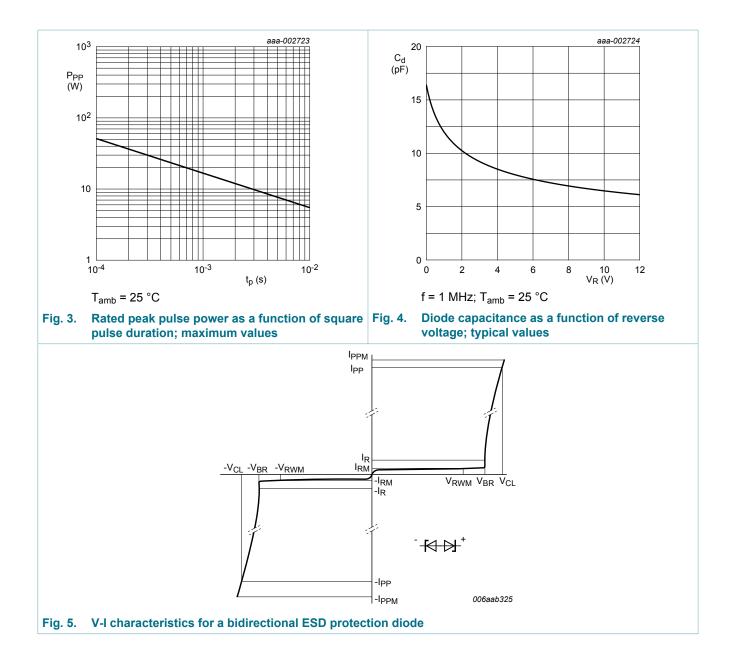
[1] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5 and IEC 61643-321.

[2] Non-repetitive current pulse, Transmission Line Pulse (TLP) t_p = 100 ns; square pulse; ANSI / ESD STM5.5.1-2008.

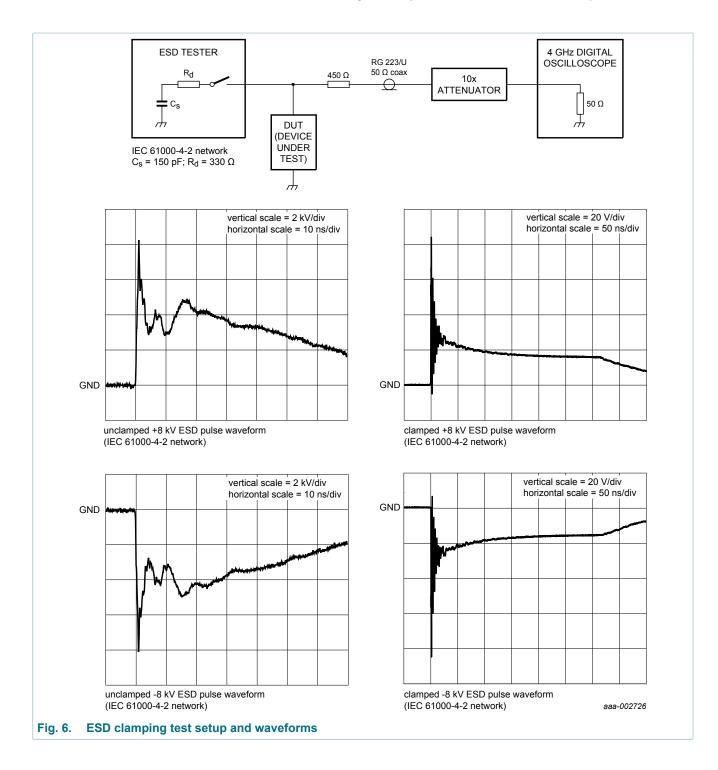
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Very low capacitance bidirectional ESD protection diode

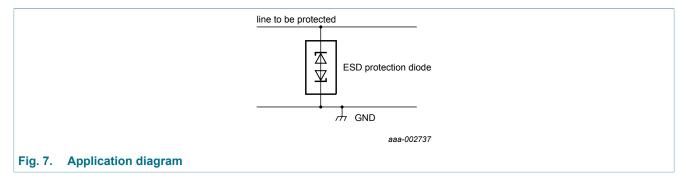


Very low capacitance bidirectional ESD protection diode



10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.



Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

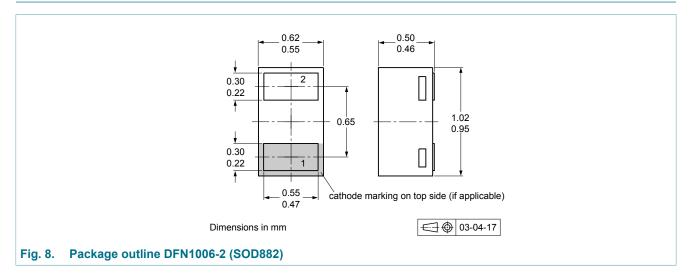
- 1. Place the device as close to the input terminal or connector as possible.
- 2. Minimize the path length between the device and the protected line.
- 3. Keep parallel signal paths to a minimum.
- 4. Avoid running protected conductors in parallel with unprotected conductors.
- 5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
- 6. Minimize the length of the transient return path to ground.
- 7. Avoid using shared transient return paths to a common ground point.
- 8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Test information

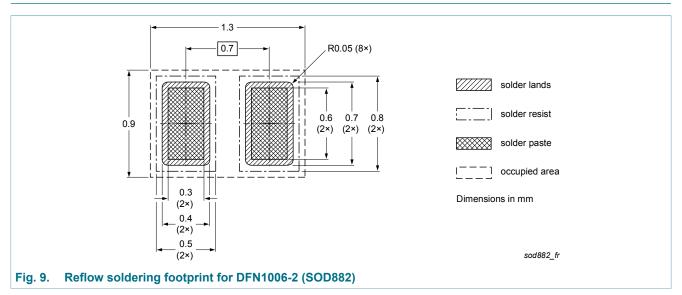
Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

12. Package outline



13. Soldering



14. Revision history

Table 7. Revision histo	ory						
Data sheet ID	Release date	Data sheet status	Change notice	Supersedes			
PESD12VV1BL v.3	20161014	Product data sheet	-	PESD12VV1BL v.2			
Modifications:	Deleted section "Page	Deleted section "Packing information"					
PESD12VV1BL v.2	20130318	Product data sheet	-	PESD12VV1BL v.1			
PESD12VV1BL v.1	20120403	Product data sheet	-	-			

Very low capacitance bidirectional ESD protection diode

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

 Please consult the most recently issued document before initiating or completing a design.

- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <u>http://www.nexperia</u>.com.

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Very low capacitance bidirectional ESD protection diode

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Very low capacitance bidirectional ESD protection diode

16. Contents

1.	General description	.1
2.	Features and benefits	. 1
3.	Applications	. 1
4.	Quick reference data	. 1
5.	Pinning information	2
6.	Ordering information	2
7.	Marking	.2
8.	Limiting values	. 2
9.	Characteristics	.3
10.	Application information	. 6
11.	Test information	. 6
12.	Package outline	. 7
13.	Soldering	. 7
14.	Revision history	8
15.	Legal information	. 9

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