NLAS1053

2:1 Mux/Demux Analog Switches

The NLAS1053 is an advanced CMOS analog switch fabricated with silicon gate CMOS technology. It achieves very high speed propagation delays and low ON resistances while maintaining CMOS low power dissipation. The device consists of a single 2:1 Mux/Demux (SPDT), similar to ON Semiconductor's NLAS4053 analog and digital voltages that may vary across the full power supply range (from V_{CC} to GND).

The inhibit and select input pins have over voltage protection that allows voltages above V_{CC} up to 7.0 V to be present without damage or disruption of operation of the part, regardless of the operating voltage.

Features

- High Speed: t_{PD} = 1 ns (Typ) at V_{CC} = 5.0 V
- Low Power Dissipation: I_{CC} = 2 μA (Max) at T_A = 25°C
- High Bandwidth, Improved Linearity, and Low RDS_{ON}
- INH Pin Allows a Both Channels 'OFF' Condition (With a High)
- $RDS_{ON} \cong 25\ \Omega$, Performance Very Similar to the NLAS4053
- Break Before Make Circuitry, Prevents Inadvertent Shorts
- Useful For Switching Video Frequencies Beyond 50 MHz
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; MM > 200 V, CDM > 1500 V
- Tiny US8 Package, Only 2.1 X 3.0 mm
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

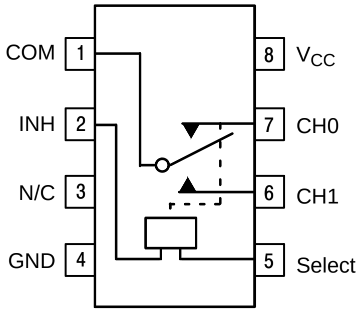

Figure 1. Pin Assignment

ON Semiconductor®

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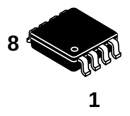
MARKING DIAGRAM



US8
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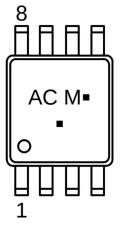
CASE 493



AC = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

INH	Select	Ch 0	Ch 1
H	X	OFF	OFF
L	L	ON	OFF
L	H	OFF	ON

ORDERING INFORMATION

Device	Package	Shipping†
NLAS1053USG	US8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Positive DC Supply Voltage	V_{CC}	–0.5 to +7.0	V
Digital Input Voltage (Select and Inhibit)	V_{IN}	$-0.5 \leq V \text{ is } \leq +7.0$	V
Analog Output Voltage (V_{CH} or V_{COM})	V_{IS}	$-0.5 \leq V \text{ is } \leq V_{CC} + 0.5$	V
DC Current, Into or Out of Any Pin	I_{IK}	50	mA
Storage Temperature Range	T_{STG}	–65 to +150	°C
Lead Temperature, 1 mm from Case for 10 Seconds	T_L	260	°C
Junction Temperature under Bias	T_J	+150	°C
Thermal Resistance	θ_{JA}	250	°C/W
Power Dissipation in Still Air at 85°C	P_D	250	mW
Moisture Sensitivity	MSL	Level 1	
Flammability Rating Oxygen Index: 30% − 35%	F_R	UL 94 V−0 @ 0.125 in	
ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	V_{ESD}	> 2000 200 N/A	V
Latchup Performance Above V_{CC} and Below GND at 85°C (Note 5)	$I_{Latchup}$	±300	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2−ounce copper trace with no air flow.
2. Tested to EIA/JESD22−A114−A.
3. Tested to EIA/JESD22−A115−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
Positive DC Supply Voltage	V_{CC}	2.0	5.5	V
Digital Input Voltage (Select and Inhibit)	V_{IN}	GND	5.5	V
Static or Dynamic Voltage Across an Off Switch	V_{IO}	GND	V_{CC}	V
Analog Input Voltage (CH, COM)	V_{IS}	GND	V_{CC}	V
Operating Temperature Range, All Package Types	T_A	–55	+125	°C
Input Rise or Fall Time (Enable Input) $V_{cc} = 3.3 \text{ V} \pm 0.3 \text{ V}$ $V_{cc} = 5.0 \text{ V} \pm 0.5 \text{ V}$	t_r, t_f	0 0	100 20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

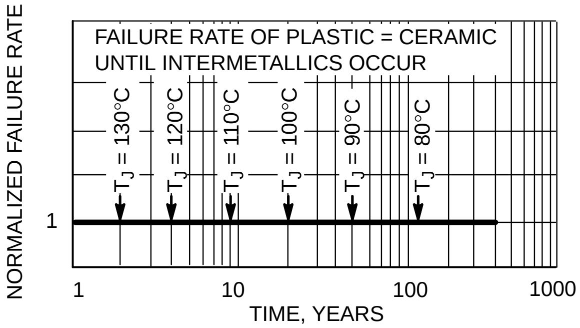


Figure 2. Failure Rate versus Time Junction Temperature

DC CHARACTERISTICS − Digital Section (Voltages Referenced to GND)

Parameter	Condition	Symbol	V_{CC}	Guaranteed Limit			Unit
				−55°C to 25°C	<85°C	<125°C	
Minimum High−Level Input Voltage, Select and Inhibit Inputs		V_{IH}	2.0 2.5 3.0 4.5 5.5	1.5 1.9 2.1 3.15 3.85	1.5 1.9 2.1 3.15 3.85	1.5 1.9 2.1 3.15 3.85	V
Maximum Low−Level Input Voltage, Select and Inhibit Inputs		V_{IL}	2.0 2.5 3.0 4.5 5.5	0.5 0.6 0.9 1.35 1.65	0.5 0.6 0.9 1.35 1.65	0.5 0.6 0.9 1.35 1.65	V
Maximum Input Leakage Current, Select and Inhibit Inputs	V_{IN} = 5.5 V or GND	I_{IN}	0 V to 5.5 V	±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	Select and Inhibit = V_{CC} or GND	I_{CC}	5.5	1.0	1.0	2.0	μA

DC ELECTRICAL CHARACTERISTICS − Analog Section

Parameter	Condition	Symbol	V_{CC}	Guaranteed Limit			Unit
				–55 to 25°C	< 85°C	< 125°C	
Maximum "ON" Resistance (Figures 17 − 23)	$V_{IN} = V_{IL}$ or V_{IH} V_{IS} = GND to V_{CC} $I_{IN}I \le 10.0$ mA	R_{ON}	2.5 3.0 4.5 5.5	70 40 20 16	85 46 28 22	105 52 34 28	Ω
ON Resistance Flatness (Figures 17 − 23)	$V_{IN} = V_{IL}$ or V_{IH} $I_{IN}I \le 10.0$ mA V_{IS} = 1V, 2V, 3.5V	R_{FLAT} (ON)	4.5	4	4	5	Ω
ON Resistance Match Between Channels	$V_{IN} = V_{IL}$ or V_{IH} $I_{IN}I \le 10.0$ mA V_{CH1} or V_{CH0} = 3.5 V	ΔR_{ON} (ON)	4.5	2	2	3	Ω
CH1 or CH0 Off Leakage Current (Figure 9)	$V_{IN} = V_{IL}$ or V_{IH} V_{CH1} or V_{CH0} = 1.0 V_{COM} 4.5 V	I_{CH0} I_{CH1}	5.5	1	10	100	nA
COM ON Leakage Current (Figure 9)	$V_{IN} = V_{IL}$ or V_{IH} V_{CH1} 1.0 V or 4.5 V with V_{CH0} floating or V_{CH1} 1.0 V or 4.5 V with V_{CH1} floating V_{COM} = 1.0 V or 4.5 V	$I_{COM(ON)}$	5.5	1	10	100	nA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

				Guaranteed Max Limit							
				−55 to 25°C			< 85°C		< 125°C		
Parameter	**Test Conditions**	**Symbol**	**V_{CC} (V)**	**Min**	**Typ***	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Turn−On Time (Figures 12 and 13) INH to Output	$R_L = 300\ \Omega$, $C_L = 35$ pF (Figures 4 and 5)	t_{ON}	2.5 3.0 4.5 5.5	2 2 1 1	7 5 4 3	12 10 9 8	2 2 1 1	15 15 12 12	2 2 1 1	15 15 12 12	ns
Turn−Off Time (Figures 12 and 13) INH to Output	$R_L = 300\ \Omega$, $C_L = 35$ pF (Figures 4 and 5)	t_{OFF}	2.5 3.0 4.5 5.5	2 2 1 1	7 5 4 3	12 10 9 8	2 2 1 1	15 15 12 12	2 2 1 1	15 15 12 12	ns
Transition Time (Channel Selection Time) (Figure) Select to Output	$R_L = 300\ \Omega$, $C_L = 35$ pF (Figures and)	t_{trans}	2.5 3.0 4.5 5.5	5 5 2 2	18 13 12 9	28 21 16 14	5 5 2 2	30 25 20 20	5 5 2 2	30 25 20 20	ns
Minimum Break−Before−Make Time	$V_{IS} = 3.0$ V (Figure 3) $R_L = 300\ \Omega$, $C_L = 35$ pF	t_{BBM}	2.5 3.0 4.5 5.5	1 1 1 1	12 11 6 5		1 1 1 1		1 1 1 1		ns
			Typical @ 25, VCC = 5.0 V								
Maximum Input Capacitance, Select/INH Input Analog I/O (switch off) Common I/O (switch off) Feedthrough (switch on)		C_{IN} C_{NO} or C_{NC} C_{COM} $C_{(ON)}$	8 10 10 20								pF

*Typical Characteristics are at 25°C.

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

				Typical	
Parameter	**Condition**	**Symbol**	**V_{CC} V**	**25°C**	**Unit**
Maximum On−Channel −3dB Bandwidth or Minimum Frequency Response (Figure 10)	$V_{IN} = 0$ dBm V_{IN} centered between V_{CC} and GND (Figure 7)	BW	3.0 4.5 5.5	170 200 200	MHz
Maximum Feedthrough On Loss	$V_{IN} = 0$ dBm @ 100 kHz to 50 MHz V_{IN} centered between V_{CC} and GND (Figure 7)	V_{ONL}	3.0 4.5 5.5	−3 −3 −3	dB
Off−Channel Isolation (Figure 10)	f = 100 kHz; $V_{IS} = 1$ V RMS V_{IN} centered between V_{CC} and GND (Figure 7)	V_{ISO}	3.0 4.5 5.5	−93 −93 −93	dB
Charge Injection Select Input to Common I/O (Figure 15)	$V_{IN} = V_{CC}$ to GND, $F_{IS} = 20$ kHz $t_r = t_f = 3$ ns $R_{IS} = 0\ \Omega$, $C_L = 1000$ pF $Q = C_L * \Delta V_{OUT}$ (Figure 8)	Q	3.0 5.5	1.5 3.0	pC
Total Harmonic Distortion THD + Noise (Figure 14)	$F_{IS} = 20$ Hz to 100 kHz, RL = Rgen = 600 Ω $C_L = 50$ pF $V_{IS} = 5.0\ V_{PP}$ sine wave	THD	5.5	0.1	%

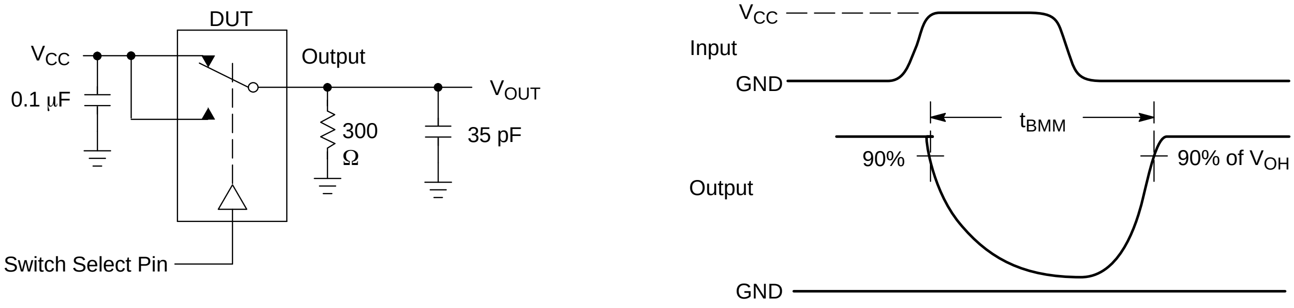


Figure 3. t_{BBM} (Time Break−Before−Make)

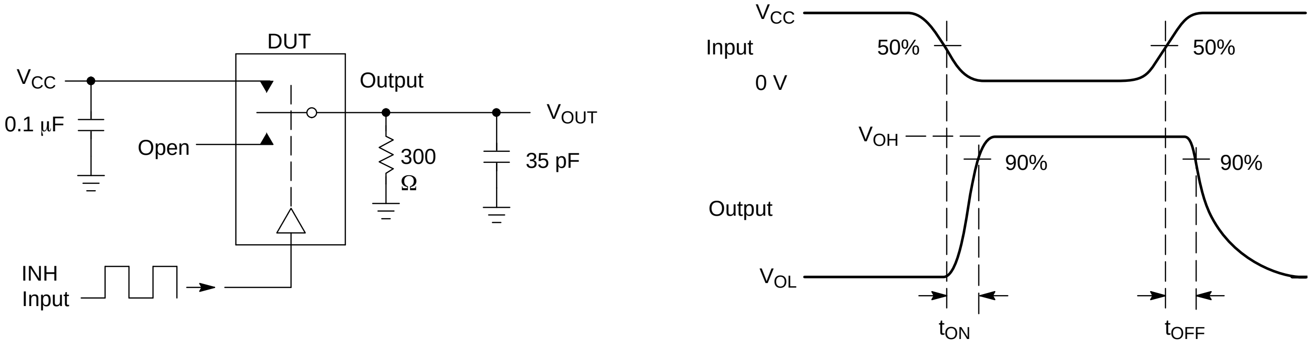


Figure 4. t_{ON}/t_{OFF}

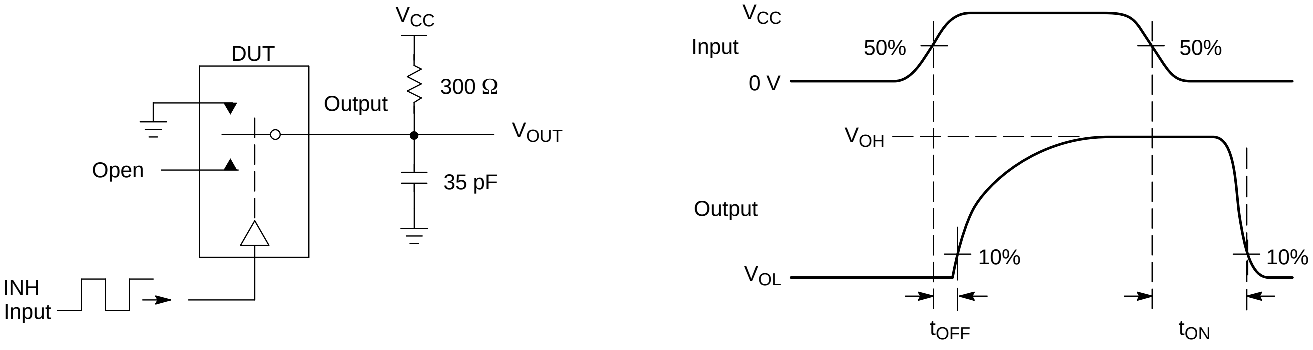


Figure 5. t_{ON}/t_{OFF}

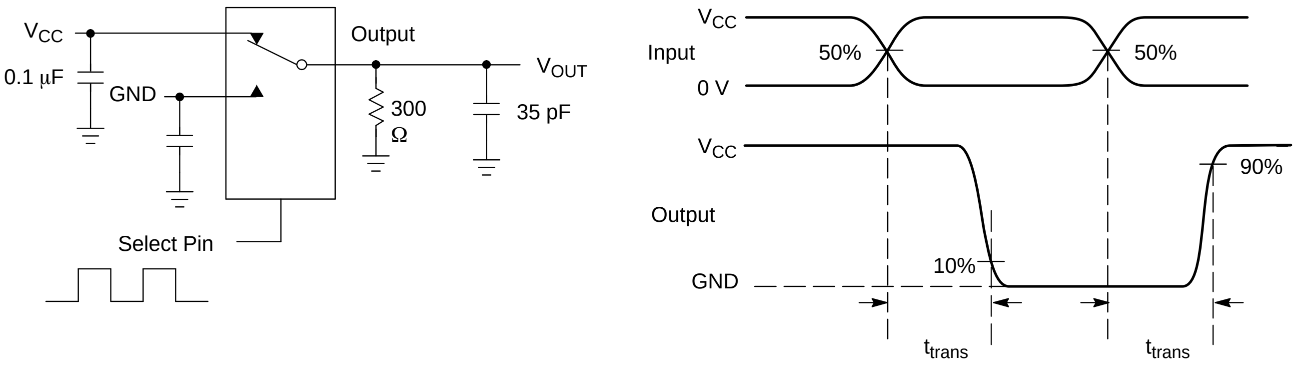
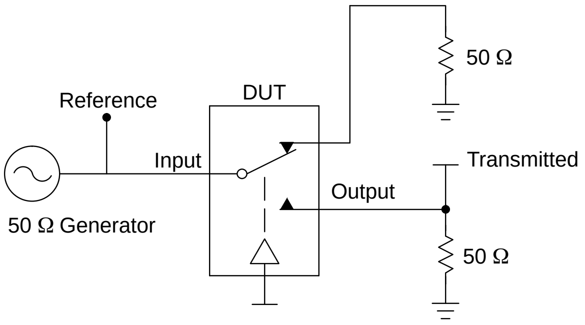


Figure 6. t_{trans} **(Channel Selection Time)**



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO}, Bandwidth and V_{ONL} are independent of the input signal direction.

V_{ISO} = Off Channel Isolation = 20 Log $\left(\frac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz

V_{ONL} = On Channel Loss = 20 Log $\left(\frac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz to 50 MHz

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

Figure 7. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/V_{ONL}

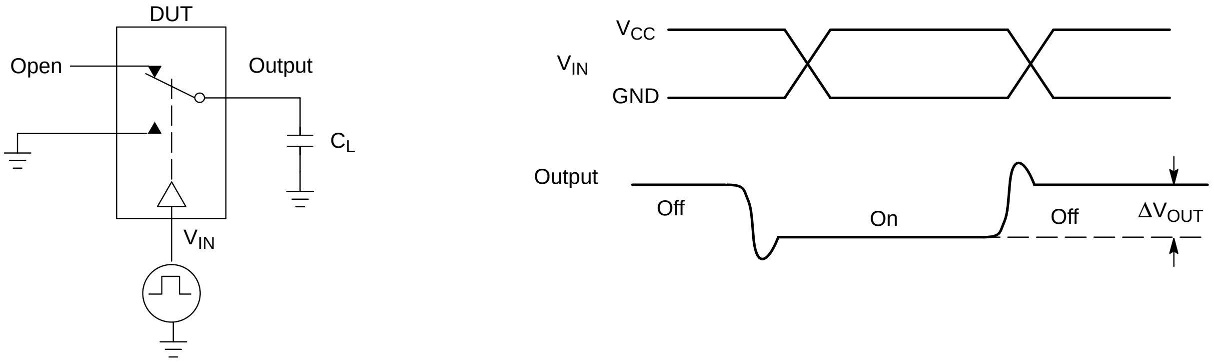


Figure 8. Charge Injection: (Q)

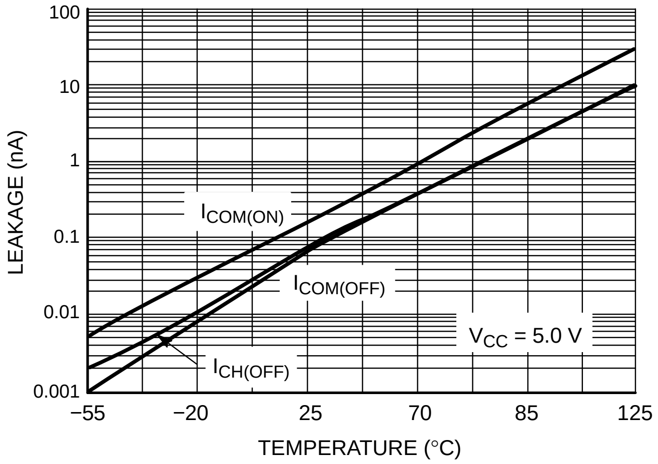


Figure 9. Switch Leakage versus Temperature

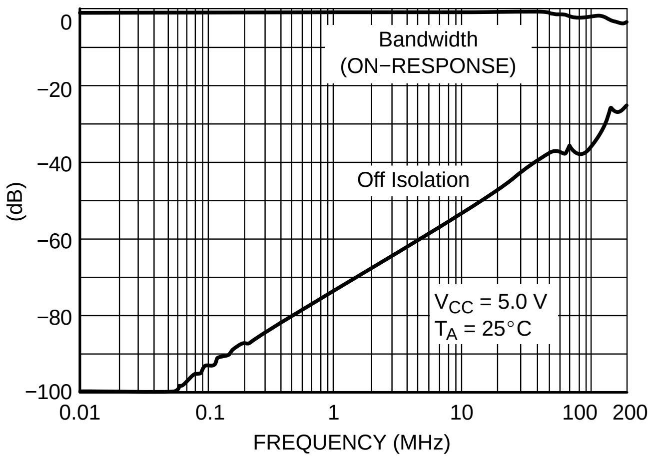


Figure 10. Bandwidth and Off−Channel Isolation

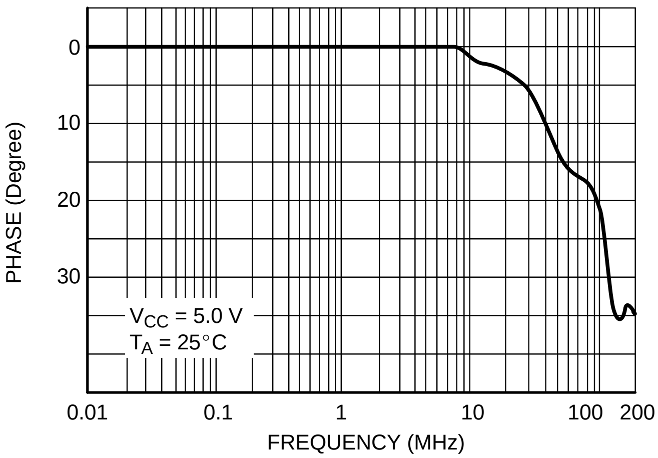


Figure 11. Phase versus Frequency

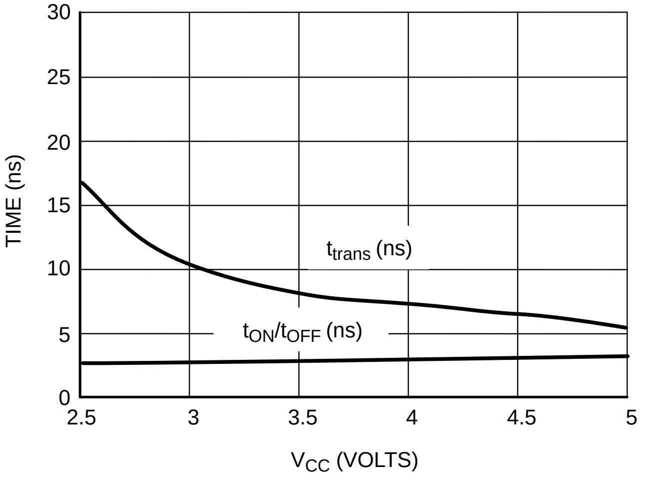


Figure 12. t_{ON} and t_{OFF} versus V_{CC} at 25°C

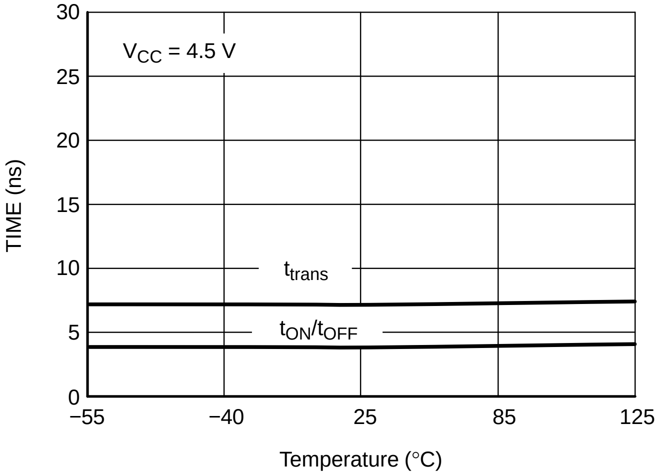


Figure 13. t_{ON} and t_{OFF} versus Temp

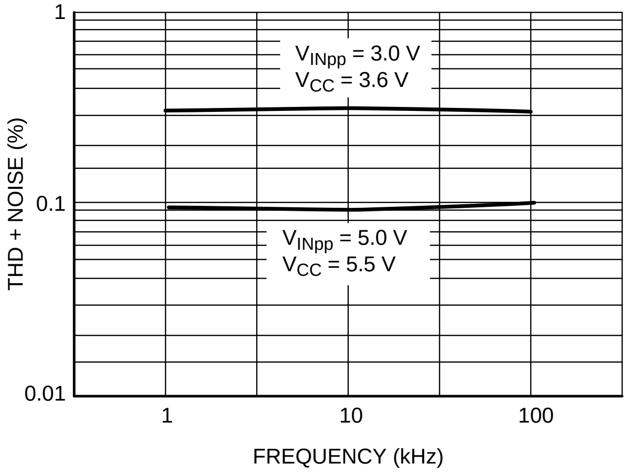


Figure 14. Total Harmonic Distortion Plus Noise versus Frequency

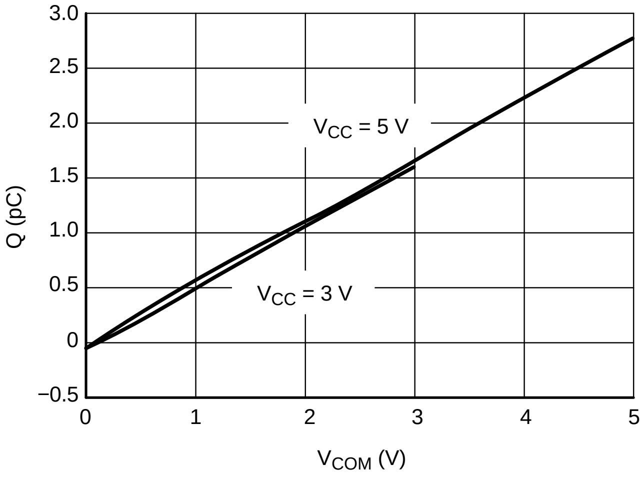


Figure 15. Charge Injection versus COM Voltage

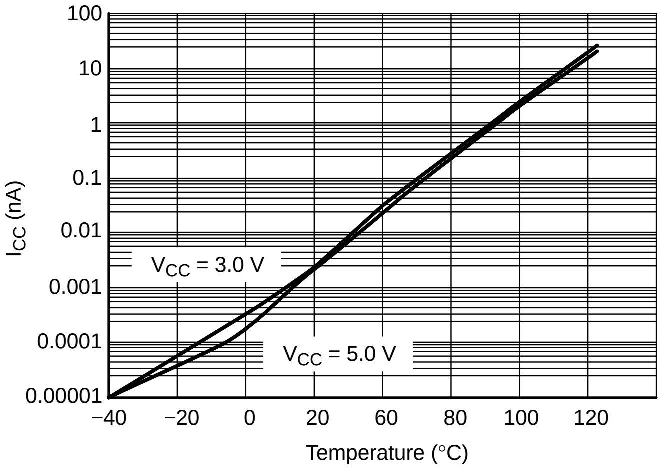


Figure 16. I_{CC} versus Temp, V_{CC} = 3 V & 5 V

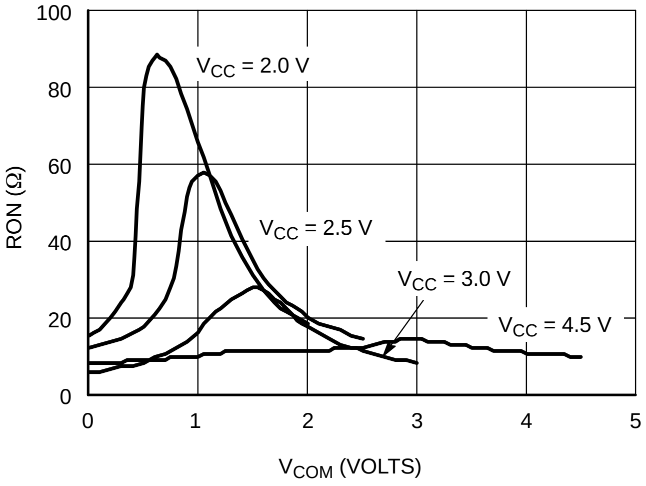


Figure 17. R_{ON} versus V_{COM} and V_{CC} (@ 25°C

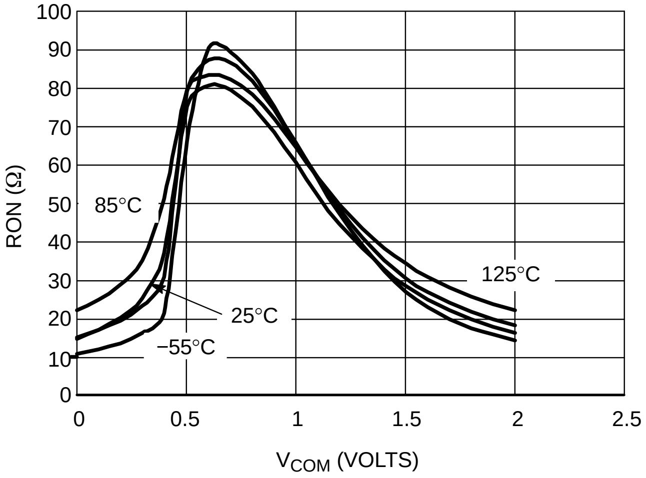


Figure 18. R_{ON} versus V_{COM} and Temperature, V_{CC} 2.0 V

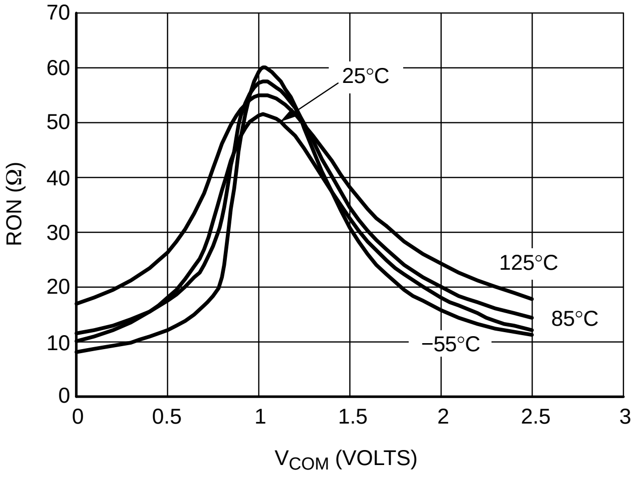


Figure 19. R_{ON} versus V_{COM} and Temperature, V_{CC} = 2.5 V

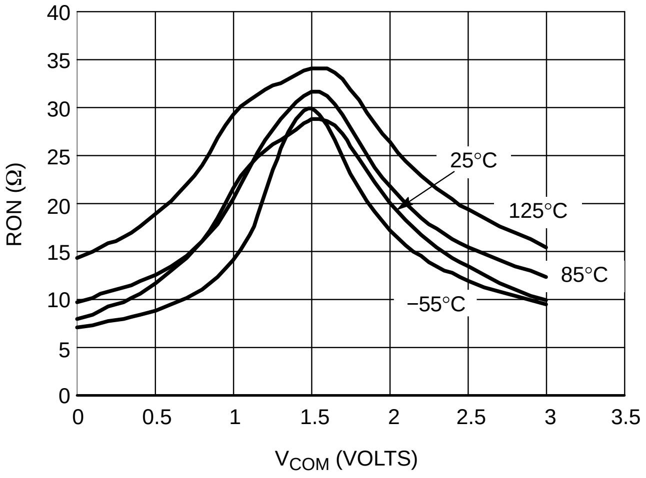


Figure 20. R_{ON} versus V_{COM} and Temperature, V_{CC} = 3.0 V

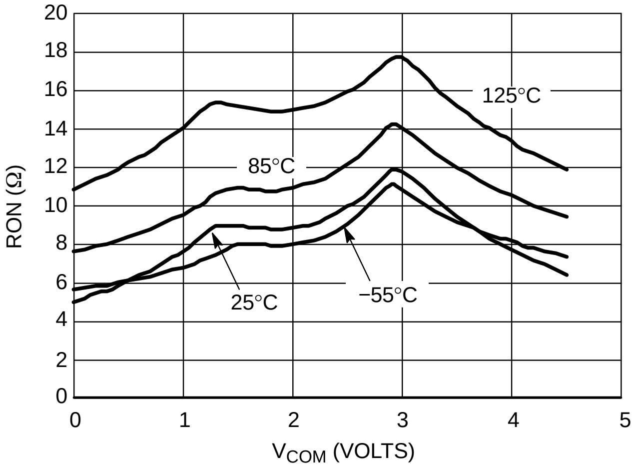


Figure 21. R_{ON} versus V_{COM} and Temperature, V_{CC} = 4.5 V

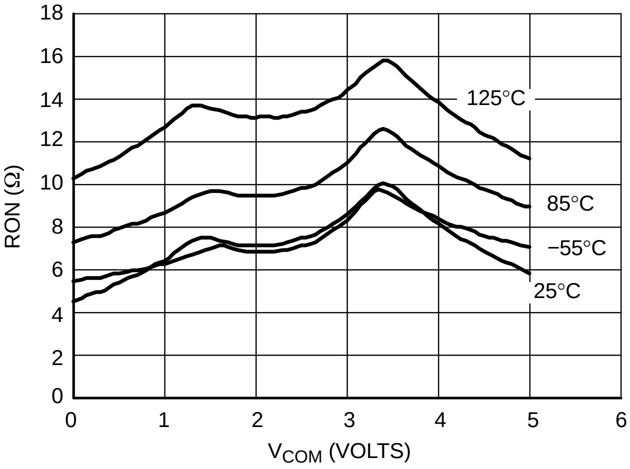


Figure 22. R_{ON} versus V_{COM} and Temperature, V_{CC} = 5.0 V

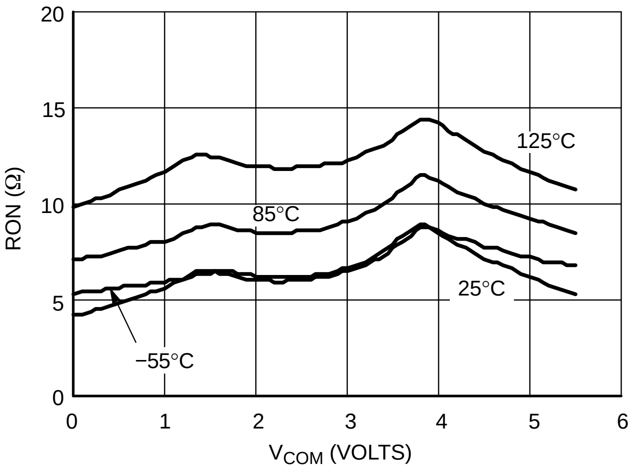
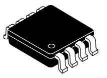


Figure 23. R_{ON} versus V_{COM} and Temperature, V_{CC} = 5.5 V

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



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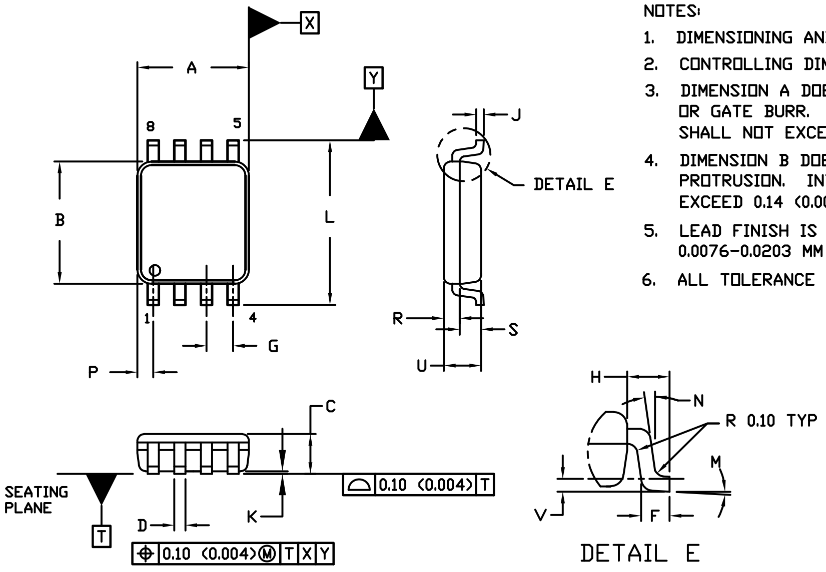
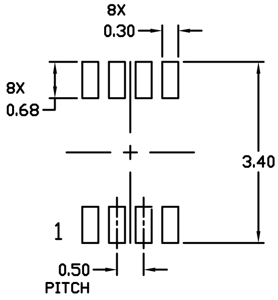


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR. MOLD FLASH, PROTRUSION, OR GATE BURR SHALL NOT EXCEED 0.14 (0.0055") PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.14 (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076-0.0203 MM (0.003-0.008").
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.0508 MM (0.002").

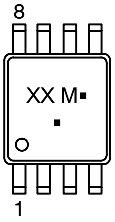
	MILLIMETERS		INCHES	
DIM	MIN.	MAX.	MIN.	MAX.
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.25	0.118	0.128
M	0°	6°	0°	6°
N	0°	10°	0°	10°
P	0.23	0.34	0.010	0.013
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12 BSC		0.005 BSC	



RECOMMENDED *
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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