

TinyLogic UHS Dual Buffer (Open-Drain Outputs)

NC7WZ07

Description

The NC7WZ07 is a dual buffer with open-drain outputs from onsemi's Ultra-High Speed (UHS) series of TinyLogic. The device is fabricated with advanced CMOS technology to achieve ultra-high speed with high output drive, while maintaining low static power dissipation over a broad V_{CC} operating range. The device is specified to operate over a very broad V_{CC} operating range. The device is specified to operate over the 1.65 V to 5.5 V V_{CC} range. The inputs and outputs are high impedance when V_{CC} is 0 V. Inputs tolerate voltages up to 5.5 V independent of V_{CC} operating voltage.

Features

- Ultra-High Speed: $t_{PZL} = 2.3$ ns (Typical)
- High I_{OL} Output Drive: ± 24 mA at 3 V V_{CC}
- Broad V_{CC} Operating Range: 1.65 V to 5.50 V
- Power Down High-Impedance Inputs / Outputs
- Over-Voltage Tolerance Inputs Facilitate 5 V to 3 V Translation
- Proprietary Noise / EMI Reduction Circuitry
- Ultra-Small MicroPak™ Packages
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

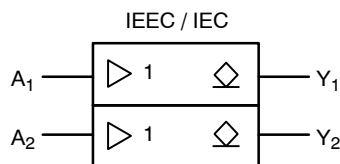
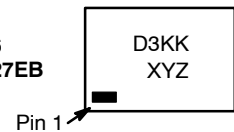


Figure 1. Logic Symbol

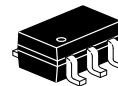
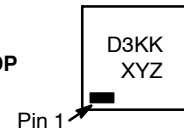
MARKING DIAGRAMS



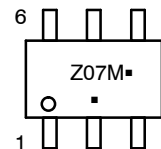
SIP6
CASE 127EB



UDFN6
CASE 517DP



SC-88
CASE 419B-02



| | |
|---------|-------------------------------------|
| D3, Z07 | = Specific Device Code |
| KK | = 2-Digit Lot Run Traceability Code |
| XY | = 2-Digit Date Code Format |
| Z | = Assembly Plant Code |
| M | = Date Code* |
| ▪ | = Pb-Free Package |

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

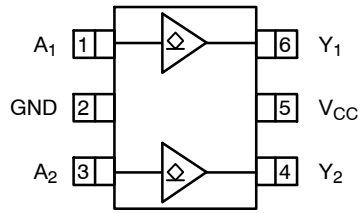


Figure 2. SC-88 (Top View)

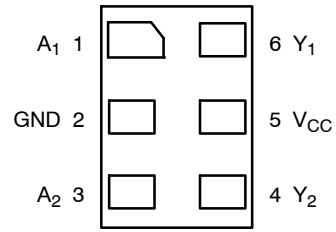
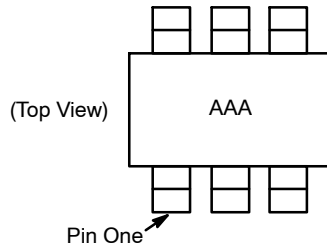


Figure 3. MicroPak (Top Through View)



- NOTES:
1. AAA represents product code top mark (*see Ordering Information*).
 2. Orientation of top mark determines pin one location.
 3. Read the top mark left to right, pin one is the lower left pin.

Figure 4. Pin 1 Orientation

PIN DEFINITIONS

| Pin # SC-88 | Pin # MicroPak | Name | Description |
|-------------|----------------|-----------------|----------------|
| 1 | 1 | A ₁ | Input |
| 2 | 2 | GND | Ground |
| 3 | 3 | A ₂ | Input |
| 4 | 4 | Y ₂ | Output |
| 5 | 5 | V _{CC} | Supply Voltage |
| 6 | 6 | Y ₁ | Output |

FUNCTION TABLE (Y = A)

| Inputs | Output |
|------------------|---|
| A | Y |
| LOW Logic Level | LOW Logic Level |
| HIGH Logic Level | HIGH Impedance Output State, Open Drain |

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | | Min | Max | Unit |
|-------------------------------------|---|------------------------|------|------|------|
| V _{CC} | Supply Voltage | | -0.5 | 6.5 | V |
| V _{IN} | DC Input Voltage | | -0.5 | 6.5 | V |
| V _{OUT} | DC Output Voltage | | -0.5 | 6.5 | V |
| I _{IK} | DC Input Diode Current | V _{IN} < 0 V | - | -50 | mA |
| I _{OK} | DC Output Diode Current | V _{OUT} < 0 V | - | -50 | mA |
| I _{OUT} | DC Output Current | | - | ±50 | mA |
| I _{CC} or I _{GND} | DC V _{CC} or Ground Current | | - | ±100 | mA |
| T _{STG} | Storage Temperature Range | | -65 | +150 | °C |
| T _J | Junction Temperature Under Bias | | - | +150 | °C |
| T _L | Junction Lead Temperature (Soldering, 10 Seconds) | | - | +260 | °C |
| P _D | Power Dissipation in Still Air | SC-88 | - | 332 | mW |
| | | MicroPak-6 | - | 812 | |
| | | MicroPak2™-6 | - | 812 | |
| ESD | Human Body Model, JEDEC: JESD22-A114 | | - | 4000 | V |
| | Charge Device Model, JEDEC: JESD22-C101 | | - | 2000 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------------------|-------------------------------|--|------|-----|------|
| V _{CC} | Supply Voltage Operating | | 1.65 | 5.5 | V |
| | Supply Voltage Data Retention | | 1.5 | 5.5 | |
| V _{IN} | Input Voltage | | 0 | 5.5 | V |
| V _{OUT} | Output Voltage | | 0 | 5.5 | V |
| t _r , t _f | Input Rise and Fall Times | V _{CC} at 1.8 V ±0.15 V, 2.5 V ±0.2 V | 0 | 20 | ns/V |
| | | V _{CC} at 3.3 V ±0.3 V | 0 | 10 | |
| | | V _{CC} at 5.0 V ±0.5 V | 0 | 5 | |
| T _A | Operating Temperature | | -40 | +85 | °C |
| θ _{JA} | Thermal Resistance | SC-88-6 | - | 377 | °C/W |
| | | MicroPak-6 | - | 154 | |
| | | MicroPak2-6 | - | 154 | |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTRICAL CHARACTERISTICS

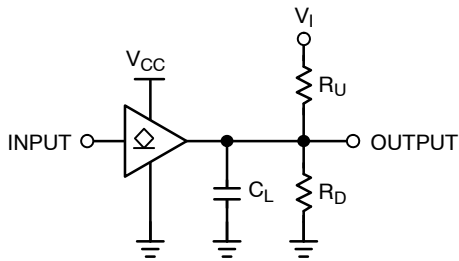
| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = +25°C | | | T _A = -40 to +85°C | | Unit |
|------------------|-----------------------------------|---------------------|---|------------------------|------|----------------------|-------------------------------|----------------------|------|
| | | | | Min | Typ | Max | Min | Max | |
| V _{IH} | HIGH Level Input Voltage | 1.65 to 1.95 | | 0.65 V _{CC} | – | – | 0.65 V _{CC} | – | V |
| | | 2.30 to 5.50 | | 0.70 V _{CC} | – | – | 0.70 V _{CC} | – | |
| V _{IL} | LOW Level Input Voltage | 1.65 to 1.95 | | – | – | 0.35 V _{CC} | – | 0.35 V _{CC} | V |
| | | 2.30 to 5.50 | | – | – | 0.30 V _{CC} | – | 0.30 V _{CC} | |
| I _{LKG} | HIGH Level Output Leakage Current | 1.65 to 1.95 | V _{IN} = V _{IH} or V _{IL} , V _{OUT} = V _{CC} or GND | – | – | ±5 | – | ±10 | µA |
| V _{OL} | LOW Level Output Voltage | 1.65 | V _{IN} = V _{IH} or V _{IL} , I _{OL} = 100 µA | – | 0.00 | 0.10 | – | 0.00 | V |
| | | 1.80 | | – | 0.00 | 0.10 | – | 0.10 | |
| | | 2.30 | | – | 0.00 | 0.10 | – | 0.10 | |
| | | 3.00 | | – | 0.00 | 0.10 | – | 0.10 | |
| | | 4.50 | | – | 0.00 | 0.10 | – | 0.10 | |
| | | 1.65 | I _{OL} = 4 mA | – | 0.80 | 0.24 | – | 0.24 | |
| | | 2.30 | I _{OL} = 8 mA | – | 0.10 | 0.30 | – | 0.30 | |
| | | 3.00 | I _{OL} = 16 mA | – | 0.16 | 0.40 | – | 0.40 | |
| | | 3.00 | I _{OL} = 24 mA | – | 0.24 | 0.55 | – | 0.55 | |
| | | 4.50 | I _{OL} = 32 mA | – | 0.25 | 0.55 | – | 0.55 | |
| I _{IN} | Input Leakage Current | 1.65 to 5.5 | 0 ≤ V _{IN} ≤ 5.5 V | – | – | ±0.1 | – | ±1.0 | µA |
| I _{OFF} | Power Off Leakage Current | 0 | V _{IN} or V _{OUT} = 5.5 V | – | – | 1 | – | 10 | µA |
| I _{CC} | Quiescent Supply Current | 1.65 to 5.50 | V _{IN} = 5.5 V, GND | – | – | 1 | – | 10 | µA |

AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = +25°C | | | T _A = -40 to +85°C | | Unit |
|-------------------------------------|--|---------------------|---|------------------------|-----|------|-------------------------------|------|------|
| | | | | Min | Typ | Max | Min | Max | |
| t _{PZL} , t _{PLZ} | Propagation Delay (Figure 5, 6) | 1.65 | C _L = 50 pF, R _U = 500 Ω, R _D = 500 Ω, V _I = 2 × V _{CC} | – | 6.6 | 11.5 | – | 12.6 | ns |
| | | 1.80 | | – | 5.5 | 9.5 | – | 10.5 | |
| | | 2.50 ±0.20 | | – | 3.7 | 5.8 | – | 6.4 | |
| | | 3.30 ±0.30 | | – | 2.9 | 4.4 | – | 4.8 | |
| | | 5.00 ±0.50 | | – | 2.3 | 3.5 | – | 3.9 | |
| | | 1.65 | C _L = 50 pF, R _U = 500 Ω, R _D = 500 Ω, V _I = 2 × V _{CC} | – | 5.5 | 11.5 | – | 12.6 | |
| | | 1.80 | | – | 4.3 | 9.5 | – | 10.5 | |
| | | 2.50 ±0.20 | | – | 2.8 | 5.8 | – | 6.4 | |
| | | 3.30 ±0.30 | | – | 2.1 | 4.4 | – | 4.8 | |
| | | 5.00 ±0.50 | | – | 1.4 | 3.5 | – | 3.9 | |
| C _{IN} | Input Capacitance | 0 | | – | 2.5 | – | – | – | pF |
| C _{OUT} | Output Capacitance | 0 | | – | 4.0 | – | – | – | pF |
| C _{PD} | Power Dissipation Capacitance (Note 5) (Figure 7) | 3.30 | | – | 3 | – | – | – | pF |
| | | 5.00 | | – | 4 | – | – | – | |

5. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression:
I_{CCD} = (C_{PD}) (V_{CC}) (f_{IN}) + (I_{CC}static).

NC7WZ07



NOTE:

6. C_L includes load and stray capacitance.
7. Input PRR = 1.0 MHz, $t_W = 500$ ns.

Figure 5. AC Test Circuit

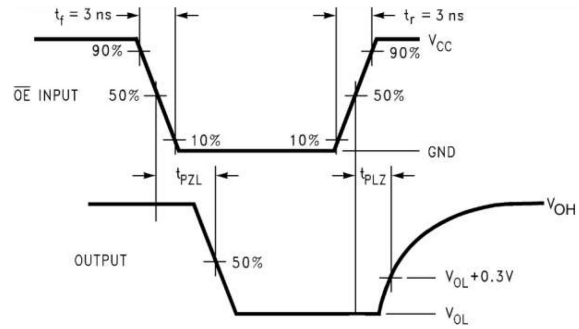
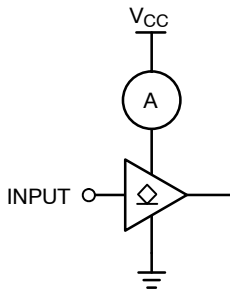


Figure 6. AC Waveforms



NOTE:

8. Input = AC Waveform; $t_r = t_f = 1.8$ ns;
PRR = Variable; Duty Cycle = 50%.

Figure 7. I_{CCD} Test Circuit

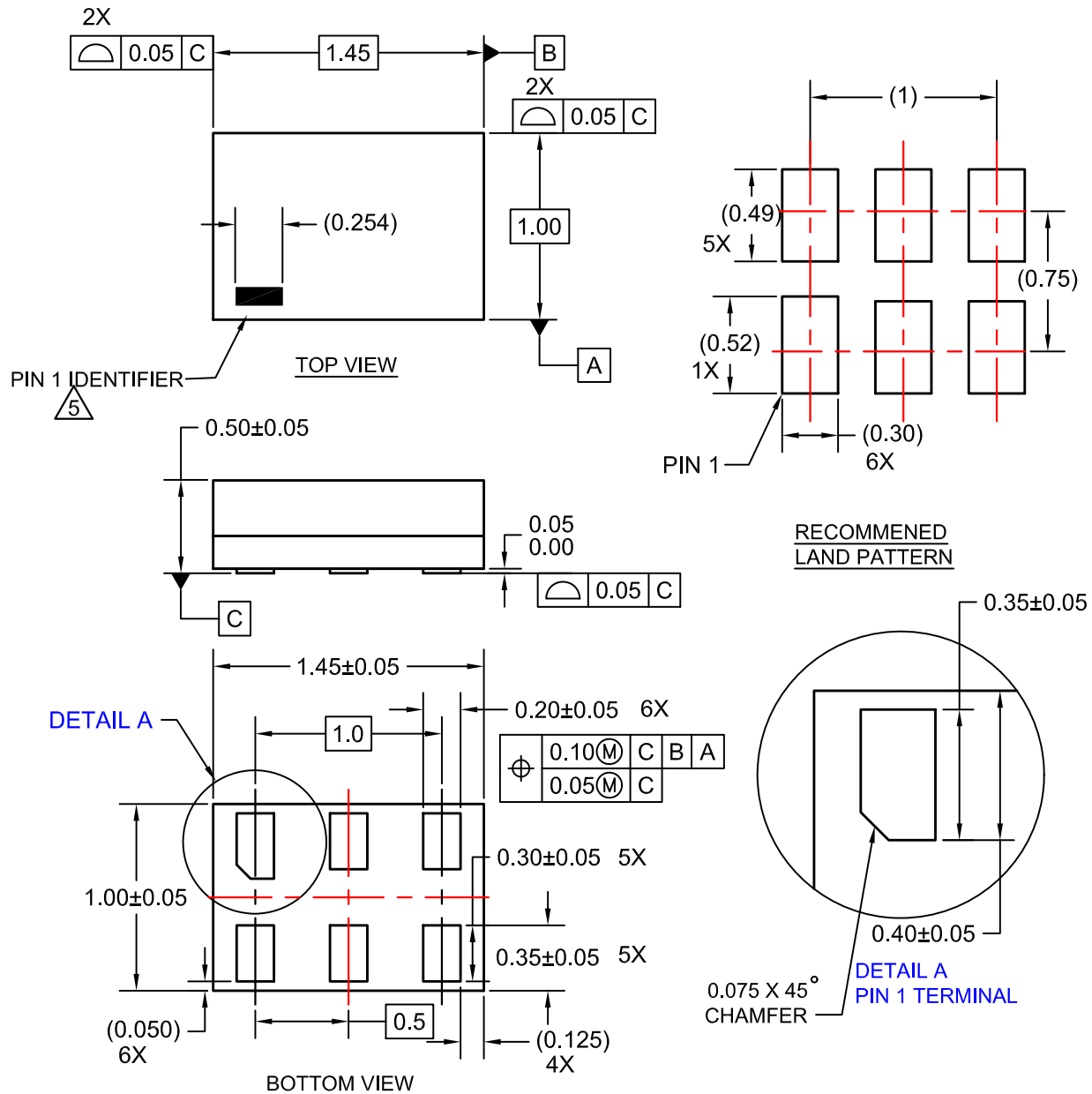
ORDERING INFORMATION

| Part Number | Top Mark | Package | Shipping [†] |
|-------------------|----------|-----------|-----------------------|
| NC7WZ07P6X | Z07 | SC-88 | 3000 / Tape & Reel |
| NC7WZ07P6X-L22347 | Z07 | SC-88 | 3000 / Tape & Reel |
| NC7WZ07L6X | D3 | MicroPak | 5000 / Tape & Reel |
| NC7WZ07FHX | D3 | MicroPak2 | 5000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ON


DATE 31 AUG 2016



NOTES:

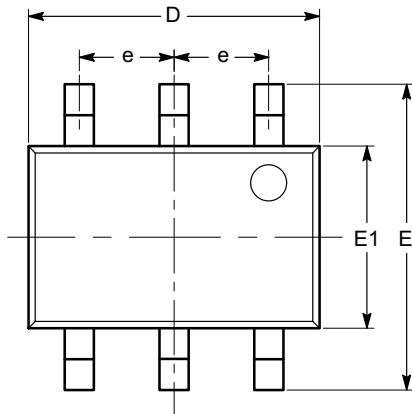
1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

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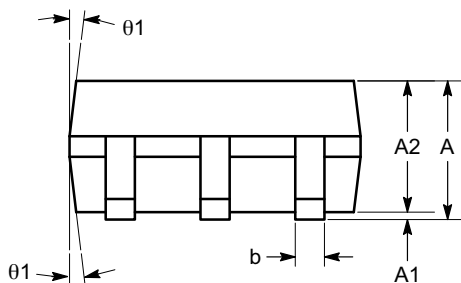
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SC-88 (SC-70 6 Lead), 1.25x2
CASE 419AD-01
ISSUE A

DATE 07 JUL 2010

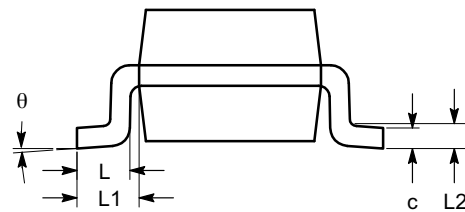


TOP VIEW



SIDE VIEW

| SYMBOL | MIN | NOM | MAX |
|--------|----------|------|------|
| A | 0.80 | | 1.10 |
| A1 | 0.00 | | 0.10 |
| A2 | 0.80 | | 1.00 |
| b | 0.15 | | 0.30 |
| c | 0.10 | | 0.18 |
| D | 1.80 | 2.00 | 2.20 |
| E | 1.80 | 2.10 | 2.40 |
| E1 | 1.15 | 1.25 | 1.35 |
| e | 0.65 BSC | | |
| L | 0.26 | 0.36 | 0.46 |
| L1 | 0.42 REF | | |
| L2 | 0.15 BSC | | |
| θ | 0° | | 8° |
| θ1 | 4° | | 10° |




END VIEW

Notes:

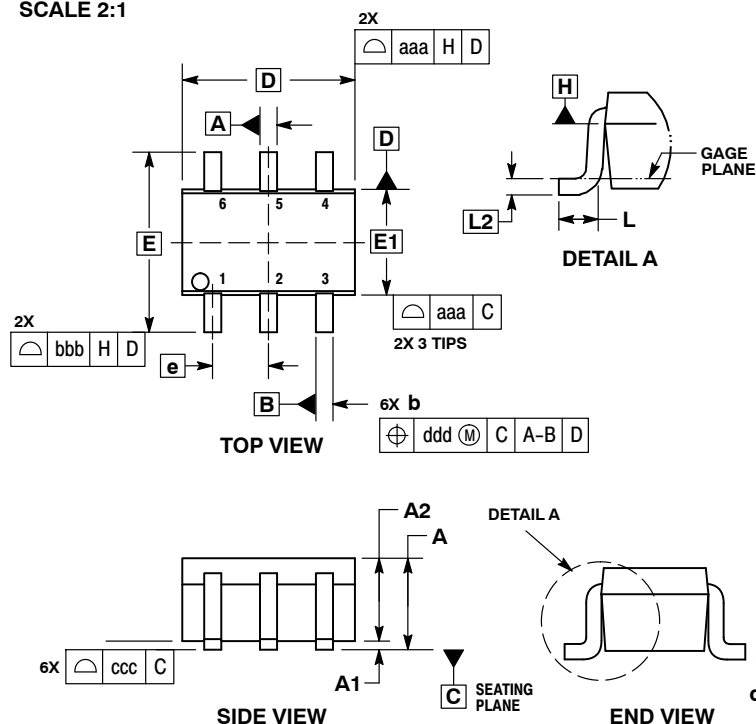
- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-203.

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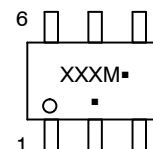
DATE 11 DEC 2012



- NOTES:**
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
 4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
 5. DATUMS A AND B ARE DETERMINED AT DATUM H.
 6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
 7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

| DIM | MILLIMETERS | | | INCHES | | |
|------------|-------------|------|------|-----------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | --- | --- | 1.10 | --- | --- | 0.043 |
| A1 | 0.00 | --- | 0.10 | 0.000 | --- | 0.004 |
| A2 | 0.70 | 0.90 | 1.00 | 0.027 | 0.035 | 0.039 |
| b | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| C | 0.08 | 0.15 | 0.22 | 0.003 | 0.006 | 0.009 |
| D | 1.80 | 2.00 | 2.20 | 0.070 | 0.078 | 0.086 |
| E | 2.00 | 2.10 | 2.20 | 0.078 | 0.082 | 0.086 |
| E1 | 1.15 | 1.25 | 1.35 | 0.045 | 0.049 | 0.053 |
| e | 0.65 BSC | | | 0.026 BSC | | |
| L | 0.26 | 0.36 | 0.46 | 0.010 | 0.014 | 0.018 |
| L2 | 0.15 BSC | | | 0.006 BSC | | |
| aaa | 0.15 | | | 0.006 | | |
| bbb | 0.30 | | | 0.012 | | |
| ccc | 0.10 | | | 0.004 | | |
| ddd | 0.10 | | | 0.004 | | |

GENERIC MARKING DIAGRAM*



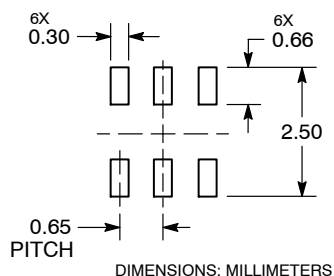
XXX = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.


RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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SC-88/SC70-6/SOT-363
CASE 419B-02
ISSUE Y

DATE 11 DEC 2012

| | | | | | |
|---|---|--|--|--|--|
| STYLE 1: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2 | STYLE 2: CANCELLED | STYLE 3: CANCELLED | STYLE 4: PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE | STYLE 5: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE | STYLE 6: PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2 |
| STYLE 7: PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2 | STYLE 8: CANCELLED | STYLE 9: PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2 | STYLE 10: PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2 | STYLE 11: PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2 | STYLE 12: PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2 |
| STYLE 13: PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE | STYLE 14: PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC | STYLE 15: PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1 | STYLE 16: PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1 | STYLE 17: PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1 | STYLE 18: PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1 |
| STYLE 19: PIN 1. IOUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF | STYLE 20: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR | STYLE 21: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1 | STYLE 22: PIN 1. D1 (i) 2. GND 3. D2 (i) 4. D2 (c) 5. VBUS 6. D1 (c) | STYLE 23: PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C | STYLE 24: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE |
| STYLE 25: PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1 | STYLE 26: PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1 | STYLE 27: PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2 | STYLE 28: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN | STYLE 29: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE | STYLE 30: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1 |

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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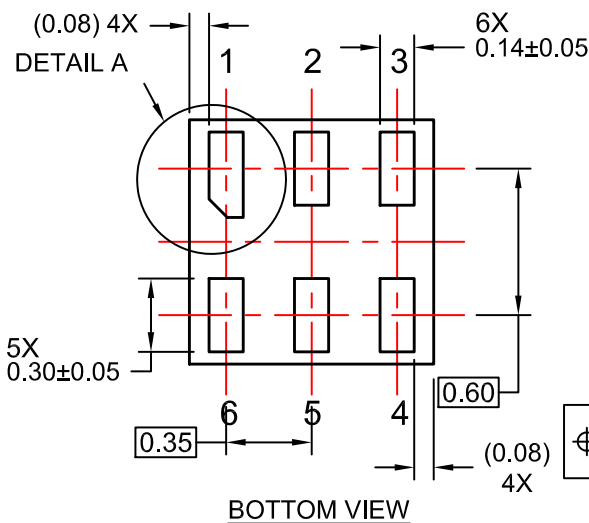
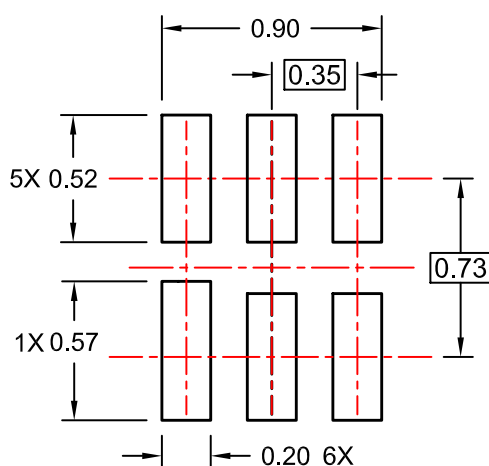
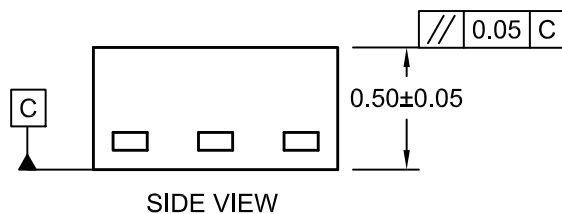
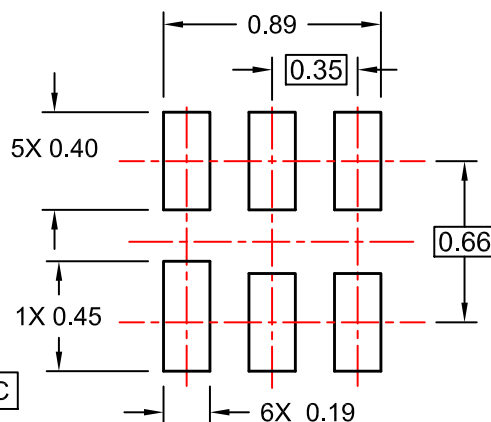
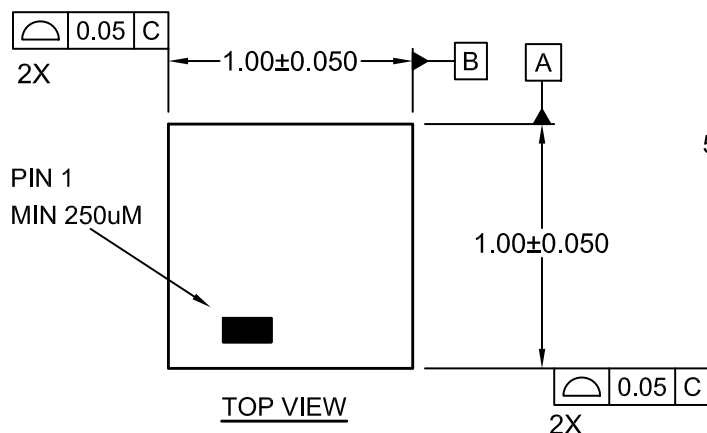
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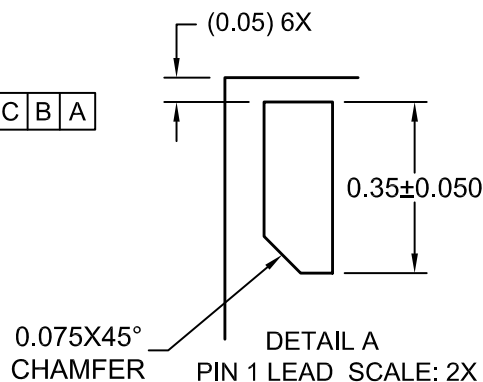
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DATE 31 AUG 2016



NOTES:

- A. COMPLIES TO JEDEC MO-252 STANDARD
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009



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