

TinyLogic UHS D-Type Flip-Flop with Asynchronous Clear

NC7SZ175

Description

The NC7SZ175 is a single positive edge-triggered D-type CMOS Flip-Flop with Asynchronous Clear from onsemi's Ultra High Speed Series of TinyLogic in the space saving SC70 6-lead package. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.65 V to 5.5 V V_{CC} range. The inputs and output are high impedance when V_{CC} is 0 V. Inputs tolerate voltages up to 5.5 V independent of V_{CC} operating voltage. This single flip-flop will store the state of the D input that meets the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. A LOW input to Clear sets the Q output to LOW level. The Clear input is independent of clock.

Features

- Space Saving SC-88 6-Lead Package
- Ultra Small MicroPak™ Leadless Package
- Ultra High Speed: $t_{PD} = 2.6$ ns Typ into 50 pF at 5 V V_{CC}
- High Output Drive: ± 24 mA at 3 V V_{CC}
- Broad V_{CC} Operating Range: 1.65 V to 5.5 V
- Matches the Performance of LCX when Operated at 3.3 V V_{CC}
- Power Down High Impedance Inputs / Output
- Overvoltage Tolerant Inputs Facilitate 5 V to 3 V Translation
- Proprietary Noise / EMI Reduction Circuitry Implemented
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

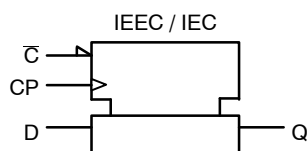
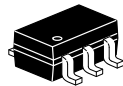
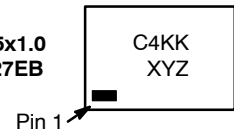


Figure 1. Logic Symbol

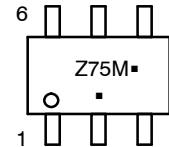
MARKING DIAGRAMS



SIP6 1.45x1.0
CASE 127EB



SC-88
CASE 419B-02



| | |
|---------|-------------------------------------|
| C4, Z75 | = Specific Device Code |
| KK | = 2-Digit Lot Run Traceability Code |
| XY | = 2-Digit Date Code Format |
| Z | = Assembly Plant Code |
| M | = Date Code* |
| ▪ | = Pb-Free Package |

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

Connection Diagrams

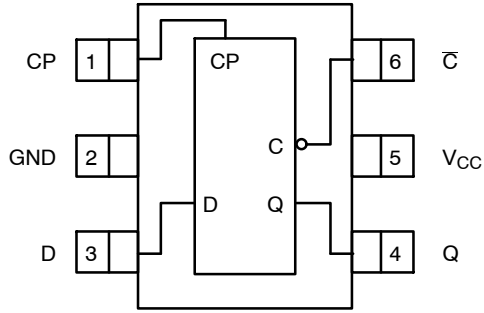


Figure 2. SC70 (Top View)

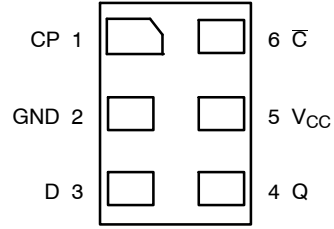
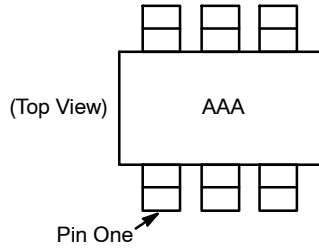


Figure 4. MicroPak (Top Through View)



AAA represents Product Code Top Mark – see ordering code.

NOTE: Orientation of Top Mark determines Pin One location.
Read the Top Product Code Mark left to right, Pin One is the lower left pin (see diagram).

Figure 3. Pin 1 Orientation

PIN DESCRIPTIONS

| Pin Name | Description |
|-----------|-------------------|
| D | Data Input |
| CP | Clock Pulse Input |
| \bar{C} | Clear Input |
| Q | Flip-Flop Output |

FUNCTION TABLE

| Inputs | | | Output |
|--------|---|-----------|--------|
| CP | D | \bar{C} | Q |
| | L | H | L |
| | H | H | H |
| | X | H | Qn |
| X | X | L | L |

H = HIGH Logic Level
L = LOW Logic Level

Qn = No Change in Data
X = Immaterial

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | | Min | Max | Unit |
|------------------------------------|---|------------------------|------|------|------|
| V _{CC} | Supply Voltage | | –0.5 | +6.5 | V |
| V _{IN} | DC Input Voltage | | –0.5 | +6.5 | V |
| V _{OUT} | DC Output Voltage | | –0.5 | +6.5 | V |
| I _{IK} | DC Input Diode Current | V _{IN} < 0 V | – | –50 | mA |
| I _{OK} | DC Output Diode Current | V _{OUT} < 0 V | – | –50 | mA |
| I _{OUT} | DC Output Source / Sink Current | | – | ±50 | mA |
| I _{CC} / I _{GND} | DC V _{CC} / GND Current | | – | ±50 | mA |
| T _{STG} | Storage Temperature Range | | –65 | +150 | °C |
| T _J | Junction Temperature under Bias | | – | 150 | °C |
| T _L | Junction Lead Temperature (Soldering, 10 Seconds) | | – | 260 | °C |
| P _D | Power Dissipation in Still Air | SC–88 | – | 332 | mW |
| | | MicroPak–6 | – | 812 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------------------|-------------------------------|---------------------------------------|------|-----------------|------|
| V _{CC} | Supply Voltage Operating | | 1.65 | 5.5 | V |
| | Supply Voltage Data Retention | | 1.5 | 5.5 | |
| V _{IN} | Input Voltage | | 0 | 5.5 | V |
| V _{OUT} | Output Voltage | | 0 | V _{CC} | V |
| t _r , t _f | Input Rise and Fall Time | V _{CC} = 1.8 V, 2.5 V ±0.2 V | 0 | 20 | ns/V |
| | | V _{CC} = 3.3 V ±0.3 V | 0 | 10 | |
| | | V _{CC} = 5.5 V ±0.5 V | 0 | 5 | |
| T _A | Operating Temperature | | –40 | +85 | °C |
| θ _{JA} | Thermal Resistance | SC–88 | – | 377 | °C/W |
| | | MicroPak–6 | – | 154 | |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = +25°C | | | T _A = -40 to +85°C | | Unit |
|------------------|-----------------------------------|---------------------|--|---------------------------|------|----------------------|-------------------------------|----------------------|------|
| | | | | Min | Typ | Max | Min | Max | |
| V _{IH} | HIGH Level Input Control Voltage | 1.65 to 1.95 | | 0.65 V _{CC} | – | – | 0.65 V _{CC} | – | V |
| | | 2.3 to 5.5 | | 0.7 V _{CC} | – | – | 0.7 V _{CC} | – | |
| V _{IL} | LOW Level Input Control Voltage | 1.65 to 1.95 | | – | – | 0.35 V _{CC} | – | 0.35 V _{CC} | V |
| | | 2.3 to 5.5 | | – | – | 0.3 V _{CC} | – | 0.3 V _{CC} | |
| V _{OH} | HIGH Level Control Output Voltage | 1.65 | V _{IN} = V _{IH} or V _{IL} | I _{OH} = -100 µA | 1.55 | 1.65 | – | 1.55 | V |
| | | 1.8 | | | 1.7 | 1.8 | – | 1.7 | |
| | | 2.3 | | | 2.2 | 2.3 | – | 2.2 | |
| | | 3.0 | | | 2.9 | 3.0 | – | 2.9 | |
| | | 4.5 | | | 4.4 | 4.5 | – | 4.4 | |
| | | 1.65 | | I _{OH} = -4 mA | 1.24 | 1.52 | – | 1.29 | |
| | | 2.3 | | I _{OH} = -8 mA | 1.9 | 2.15 | – | 1.9 | |
| | | 3.0 | | I _{OH} = -16 mA | 2.4 | 2.8 | – | 2.4 | |
| | | 3.0 | | I _{OH} = -24 mA | 2.3 | 2.68 | – | 2.3 | |
| | | 4.5 | | I _{OH} = -32 mA | 3.8 | 4.2 | – | 3.8 | |
| V _{OL} | LOW Level Control Output Voltage | 1.65 | V _{IN} = V _{IH} or V _{IL} | I _{OL} = 100 µA | – | 0.0 | 0.1 | – | V |
| | | 1.8 | | | – | 0.0 | 0.1 | – | |
| | | 2.3 | | | – | 0.0 | 0.1 | – | |
| | | 3.0 | | | – | 0.0 | 0.1 | – | |
| | | 4.5 | | | – | 0.0 | 0.1 | – | |
| | | 1.65 | | I _{OL} = 4 mA | – | 0.08 | 0.24 | – | |
| | | 2.3 | | I _{OL} = 8 mA | – | 0.10 | 0.3 | – | |
| | | 3.0 | | I _{OL} = 16 mA | – | 0.15 | 0.4 | – | |
| | | 3.0 | | I _{OL} = 24 mA | – | 0.22 | 0.55 | – | |
| | | 4.5 | | I _{OL} = 32 mA | – | 0.22 | 0.55 | – | |
| I _{IN} | Input Leakage Current | 1.65 to 5.5 | 0 ≤ V _{IN} ≤ 5.5 V | – | – | ±0.1 | – | ±1.0 | µA |
| I _{OFF} | Power Off Leakage Current | 0.0 | V _{IN} or V _{OUT} = 5.5 V | – | – | 1.0 | – | 10 | µA |
| I _{CC} | Quiescent Supply Current | 1.65 to 5.5 | V _{IN} = 5.5 V, GND | – | – | 1.0 | – | 10.0 | µA |

AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = +25°C | | | T _A = -40 to +85°C | | Unit |
|-------------------------------------|---|---------------------|---|------------------------|-----|------|-------------------------------|------|------|
| | | | | Min | Typ | Max | Min | Max | |
| f _{MAX} | Maximum Clock Frequency (Figures 5, 8) | 1.65 | C _L = 50 pF, R _L = 500 Ω | – | – | – | 100 | – | MHz |
| | | 1.8 | | – | – | – | 100 | – | |
| | | 2.5 ±0.2 | | – | – | – | 125 | – | |
| | | 3.3 ±0.3 | | – | – | – | 150 | – | |
| | | 5.0 ±0.5 | | – | – | – | 175 | – | |
| t _{PLH} , t _{PHL} | Propagation Delay CP to Q (Figures 5, 7) | 1.65 | C _L = 15 pF, R _L = 1 MΩ | – | 9.8 | 15.0 | – | 16.5 | ns |
| | | 1.8 | | – | 6.5 | 10.0 | – | 11.0 | |
| | | 2.5 ±0.2 | | – | 3.8 | 6.5 | – | 7.0 | |
| | | 3.3 ±0.3 | | – | 2.8 | 4.5 | – | 5.0 | |
| | | 5.0 ±0.5 | | – | 2.2 | 3.5 | – | 3.8 | |
| | | 3.3 ±0.3 | C _L = 50 pF, R _L = 500 Ω | – | 3.4 | 5.5 | – | 6.2 | |
| | | 5.0 ±0.5 | | – | 2.6 | 4.0 | – | 4.7 | |
| t _{PHL} | Propagation Delay \overline{C} to Q (Figures 5, 7) | 1.65 | C _L = 15 pF, R _L = 1 MΩ | – | 9.8 | 13.5 | – | 15.0 | ns |
| | | 1.8 | | – | 6.5 | 9.0 | – | 10.0 | |
| | | 2.5 ±0.2 | | – | 3.8 | 6.0 | – | 6.4 | |
| | | 3.3 ±0.3 | | – | 2.8 | 4.3 | – | 4.6 | |
| | | 5.0 ±0.5 | | – | 2.2 | 3.2 | – | 3.5 | |
| | | 3.3 ±0.3 | C _L = 50 pF, R _L = 500 Ω | – | 3.4 | 5.3 | – | 5.8 | |
| | | 5.0 ±0.5 | | – | 2.7 | 4.0 | – | 4.5 | |
| t _S | Setup Time, CP to D (Figures 5, 8) | 2.5 ±0.2 | C _L = 50 pF, R _L = 500 Ω | – | – | – | 2.5 | – | ns |
| | | 3.3 ±0.3 | | – | – | – | 2.0 | – | |
| | | 5.0 ±0.5 | | – | – | – | 1.5 | – | |
| t _H | Hold Time, CP to D (Figures 5, 8) | 2.5 ±0.2 | C _L = 50 pF, R _L = 500 Ω | – | – | – | 1.5 | – | ns |
| | | 3.3 ±0.3 | | – | – | – | 1.5 | – | |
| | | 5.0 ±0.5 | | – | – | – | 1.5 | – | |
| t _W | Pulse Width, CP (Figures 5, 8) | 2.5 ±0.2 | C _L = 50 pF, R _L = 500 Ω | – | – | – | 3.0 | – | ns |
| | | 3.3 ±0.3 | | – | – | – | 2.8 | – | |
| | | 5.0 ±0.5 | | – | – | – | 2.5 | – | |
| | Pulse Width, \overline{C} (Figures 5, 8) | 2.5 ±0.2 | Clock HIGH or LOW C _L = 50 pF, R _L = 500 Ω | – | – | – | 3.0 | – | ns |
| | | 3.3 ±0.3 | | – | – | – | 2.8 | – | |
| | | 5.0 ±0.5 | | – | – | – | 2.5 | – | |
| t _{rec} | Recovery Time, \overline{C} to CP (Figures 5, 8) | 2.5 ±0.2 | C _L = 50 pF, R _L = 500 Ω | – | – | – | 1.0 | – | ns |
| | | 3.3 ±0.3 | | – | – | – | 1.0 | – | |
| | | 5.0 ±0.5 | | – | – | – | 1.0 | – | |

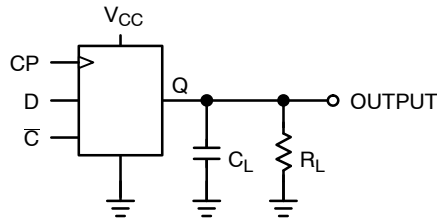
CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1\text{ MHz}$)

| Symbol | Parameter | Condition | Typ | Max | Units |
|-----------|---|--|----------|--------|-------|
| C_{IN} | Input Capacitance | $V_{CC} = \text{Open}$, $V_{IN} = 0\text{ V or } V_{CC}$ | 3 | – | pF |
| C_{OUT} | Output Capacitance | $V_{CC} = 3.3\text{ V}$, $V_{IN} = 0\text{ V or } V_{CC}$ | 4 | – | pF |
| C_{PD} | Power Dissipation Capacitance (Note 2) | $V_{CC} = 3.3\text{ V}$ $V_{CC} = 5.0\text{ V}$ | 10 12 | – – | pF |

2. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 6)

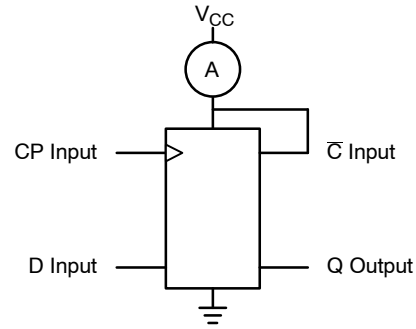
C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD}) (V_{CC}) (f_{IN}) + (I_{CCstatic})$.

AC Loading and Waveforms



C_L includes load and stray capacitance
Input PRR = 1.0 MHz, $t_W = 500\text{ ns}$.

Figure 5. AC Test Circuit



CP Input = AC Waveform; $t_r = t_f = 1.8\text{ ns}$;
CP Input PRR = 10 MHz; Duty Cycle = 50%
D Input PRR = 5 MHz; Duty Cycle = 50%.

Figure 6. I_{CCD} Test Circuit

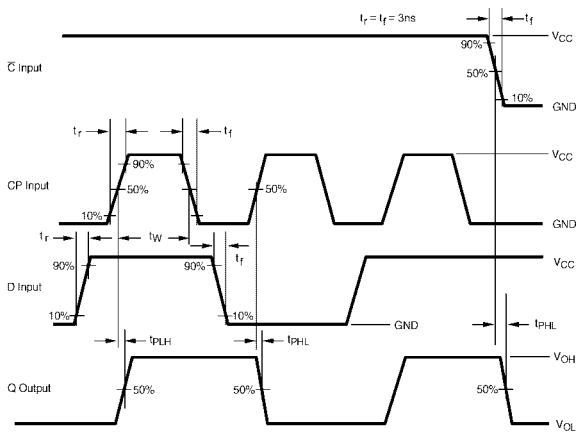


Figure 7. AC Waveforms

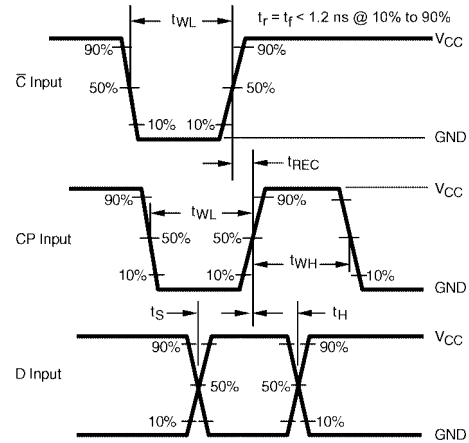


Figure 8. AC Waveforms

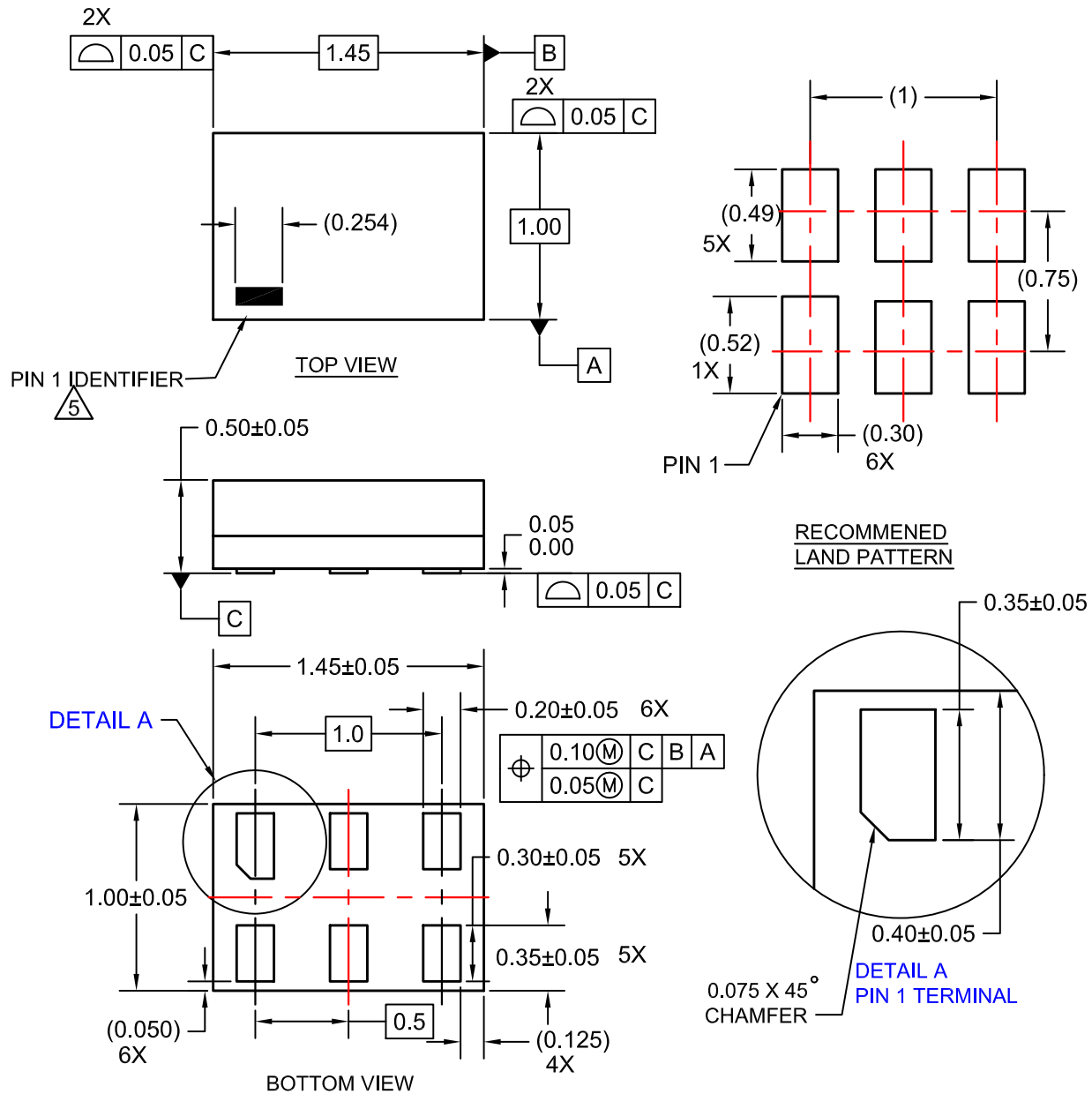
DEVICE ORDERING INFORMATION

| Device | Top Mark | Packages | Shipping† |
|--------------------|----------|--------------------------------------|--------------------|
| NC7SZ175P6X | Z75 | 6-Lead SC70, EIAJ SC88, 1.25 mm Wide | 3000 / Tape & Reel |
| NC7SZ175P6X–L22347 | Z75 | 6-Lead SC70, EIAJ SC88, 1.25 mm Wide | 3000 / Tape & Reel |
| NC7SZ175L6X | C4 | 6-Lead MicroPak, 1.00 mm Wide | 5000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ON


DATE 31 AUG 2016



NOTES:

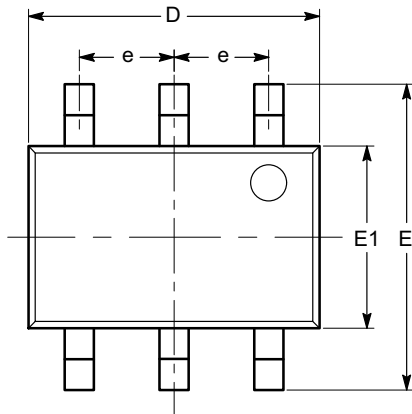
1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

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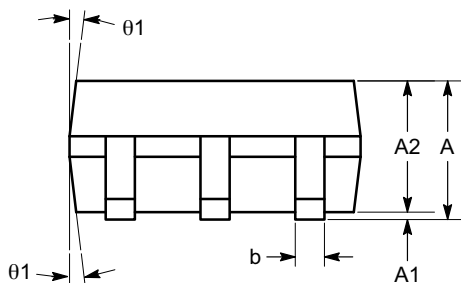
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SC-88 (SC-70 6 Lead), 1.25x2
CASE 419AD-01
ISSUE A

DATE 07 JUL 2010

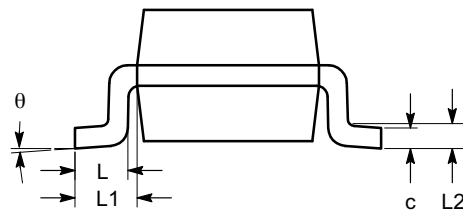


TOP VIEW



SIDE VIEW

| SYMBOL | MIN | NOM | MAX |
|--------|----------|------|------|
| A | 0.80 | | 1.10 |
| A1 | 0.00 | | 0.10 |
| A2 | 0.80 | | 1.00 |
| b | 0.15 | | 0.30 |
| c | 0.10 | | 0.18 |
| D | 1.80 | 2.00 | 2.20 |
| E | 1.80 | 2.10 | 2.40 |
| E1 | 1.15 | 1.25 | 1.35 |
| e | 0.65 BSC | | |
| L | 0.26 | 0.36 | 0.46 |
| L1 | 0.42 REF | | |
| L2 | 0.15 BSC | | |
| θ | 0° | | 8° |
| θ1 | 4° | | 10° |




END VIEW

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-203.

| | | |
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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

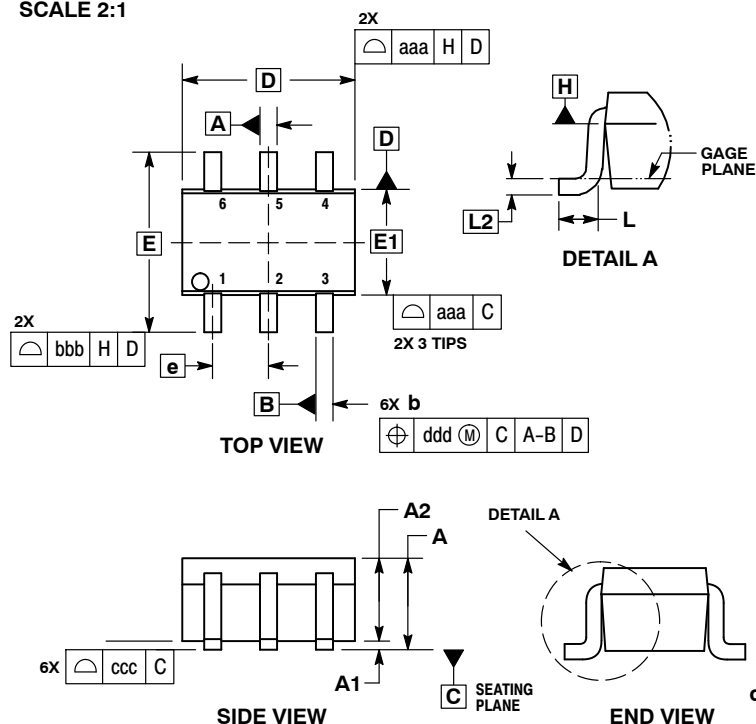
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SCALE 2:1

SC-88/SC70-6/SOT-363
CASE 419B-02
ISSUE Y

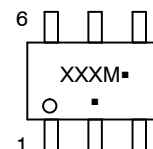
DATE 11 DEC 2012



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
 4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
 5. DATUMS A AND B ARE DETERMINED AT DATUM H.
 6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
 7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

| DIM | MILLIMETERS | | | INCHES | | |
|-----|-------------|------|------|-----------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | --- | --- | 1.10 | --- | --- | 0.043 |
| A1 | 0.00 | --- | 0.10 | 0.000 | --- | 0.004 |
| A2 | 0.70 | 0.90 | 1.00 | 0.027 | 0.035 | 0.039 |
| b | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| C | 0.08 | 0.15 | 0.22 | 0.003 | 0.006 | 0.009 |
| D | 1.80 | 2.00 | 2.20 | 0.070 | 0.078 | 0.086 |
| E | 2.00 | 2.10 | 2.20 | 0.078 | 0.082 | 0.086 |
| E1 | 1.15 | 1.25 | 1.35 | 0.045 | 0.049 | 0.053 |
| e | 0.65 BSC | | | 0.026 BSC | | |
| L | 0.26 | 0.36 | 0.46 | 0.010 | 0.014 | 0.018 |
| L2 | 0.15 BSC | | | 0.006 BSC | | |
| aaa | 0.15 | | | 0.006 | | |
| bbb | 0.30 | | | 0.012 | | |
| ccc | 0.10 | | | 0.004 | | |
| ddd | 0.10 | | | 0.004 | | |

GENERIC MARKING DIAGRAM*



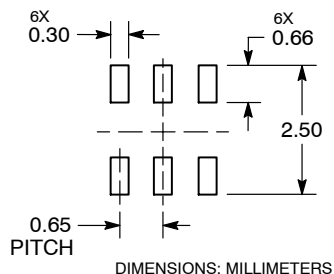
XXX = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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| DESCRIPTION: | SC-88/SC70-6/SOT-363 | PAGE 1 OF 2 |

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SC-88/SC70-6/SOT-363
CASE 419B-02
ISSUE Y

DATE 11 DEC 2012

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|---|---|--|--|--|--|
| STYLE 1: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2 | STYLE 2: CANCELLED | STYLE 3: CANCELLED | STYLE 4: PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE | STYLE 5: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE | STYLE 6: PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2 |
| STYLE 7: PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2 | STYLE 8: CANCELLED | STYLE 9: PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2 | STYLE 10: PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2 | STYLE 11: PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2 | STYLE 12: PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2 |
| STYLE 13: PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE | STYLE 14: PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC | STYLE 15: PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1 | STYLE 16: PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1 | STYLE 17: PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1 | STYLE 18: PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1 |
| STYLE 19: PIN 1. I OUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF | STYLE 20: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR | STYLE 21: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1 | STYLE 22: PIN 1. D1 (i) 2. GND 3. D2 (i) 4. D2 (c) 5. VBUS 6. D1 (c) | STYLE 23: PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C | STYLE 24: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE |
| STYLE 25: PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1 | STYLE 26: PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1 | STYLE 27: PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2 | STYLE 28: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN | STYLE 29: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE | STYLE 30: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1 |

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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