# IP4283CZ10 series

# ESD protection for ultra high-speed interfaces

Rev. 4 — 8 April 2013

Product data sheet

### 1. Product profile

#### 1.1 General description

The devices are designed to protect high-speed interfaces such as High-Definition Multimedia Interface (HDMI), DisplayPort, external Serial Advanced Technology Attachment (eSATA) and Low-Voltage Differential Signaling (LVDS) interfaces against ElectroStatic Discharge (ESD).

The devices include four high-level ESD protection diode structures for ultra high-speed signal lines. They are available in three package variants: DFN2510-10 (SOT1165-1), DFN2510A-10 (SOT1176-1) and TSSOP10 (SOT552-1).

All signal lines are protected by a special diode configuration offering ultra low line capacitance of only 0.6 pF. These diodes provide protection to downstream components from ESD voltages up to  $\pm 8$  kV contact according to IEC 61000-4-2, level 4.

#### 1.2 Features and benefits

- System ESD protection for HDMI, DisplayPort, eSATA and LVDS
- All signal lines with integrated rail-to-rail clamping diodes for downstream ESD protection of ±8 kV according to IEC 61000-4-2, level 4
- Matched 0.5 mm trace spacing
- Signal lines with ≤ 0.05 pF matching capacitance between signal pairs
- Line capacitance of only 0.6 pF for each channel
- Design-friendly 'pass-thru' signal routing

#### 1.3 Applications

The devices are designed for high-speed receiver and transmitter port protection:

- TVs, monitors
- DVD recorders and players
- Notebooks, main board graphics cards and ports
- Set-top boxes and game consoles



## 2. Pinning information

Table 1. Pinning

	<u> </u>							
Pin	Symbol	Description	Simplified outline	Graphic symbol				
IP42	IP4283CZ10-TBA (SOT1165-1)							
1	TMDS_CH1-	negative channel 1 ESD protection	10 9 8 7 6	1 2 4 5				
2	TMDS_CH1+	positive channel 1 ESD protection	1 2 3 4 5					
3	GND	ground	Transparent top view	31.8 201.202				
4	TMDS_CH2-	negative channel 2 ESD protection	DFN2510-10					
5	TMDS_CH2+	positive channel 2 ESD protection		o, 001aai619				
6	n.c.	not connected						
7	n.c.	not connected						
8	GND	ground						
9	n.c.	not connected						
10	n.c.	not connected						
IP42	83CZ10-TBR (SOT	1176-1)						
1	TMDS_CH1-	negative channel 1 ESD protection	10 9 8 7 6	1 2 4 5				
2	TMDS_CH1+	positive channel 1 ESD protection		<del>                                    </del>				
3	GND	ground	1 2 3 4 5 Transparent top view	7777				
4	TMDS_CH2-	negative channel 2 ESD protection	DFN2510A-10	3,8 24, 124				
5	TMDS_CH2+	positive channel 2 ESD protection		3, 0 001aai619				
6	n.c.	not connected						
7	n.c.	not connected						
8	GND	ground						
9	n.c.	not connected						
10	n.c.	not connected						

 Table 1.
 Pinning ...continued

Pin	Symbol	Description	Simplified outline	Graphic symbol			
IP42	83CZ10-TT (SOT	552-1)					
1	TMDS_CH1-	negative channel 1 ESD protection	10	1 2 4 5			
2	TMDS_CH1+	positive channel 1 ESD protection					
3	GND	ground					
4	TMDS_CH2-	negative channel 2 ESD protection		3, 8 <sub>001aai619</sub>			
5	TMDS_CH2+	positive channel 2 ESD protection					
6	n.c.	not connected	1 📗 📗 📗 5				
7	n.c.	not connected	TSSOP10				
8	GND	ground					
9	n.c.	not connected					
10	n.c.	not connected					

## 3. Ordering information

Table 2. Ordering information

Type number	Package					
	Name	Description	Version			
IP4283CZ10-TBA	DFN2510-10	plastic extremely thin small outline package; no leads; 10 terminals; body 1 $\times$ 2.5 $\times$ 0.5 mm	SOT1165-1			
IP4283CZ10-TBR	DFN2510A-10	plastic extremely thin small outline package; no leads; 10 terminals; body 1 $\times$ 2.5 $\times$ 0.5 mm	SOT1176-1			
IP4283CZ10-TT	TSSOP10	plastic thin shrink small outline package; 10 leads; body width 3 mm	SOT552-1			

# 4. Marking

Table 3. Marking codes

Type number	Marking code
IP4283CZ10-TBA	83
IP4283CZ10-TBR	83
IP4283CZ10-TT	4283

## 5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{I}$	input voltage		-0.5	+5.5	V
V <sub>ESD</sub>	electrostatic discharge voltage	IEC 61000-4-2, level 4	<u>[1]</u>		
		contact discharge	-8	+8	kV
		air discharge	-15	+15	kV
T <sub>stg</sub>	storage temperature		-55	+125	°C
T <sub>amb</sub>	ambient temperature		-40	+85	°C

<sup>[1]</sup> All pins to ground.

## 6. Characteristics

Table 5. Characteristics

 $T_{amb} = 25$  °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$V_{BR}$	breakdown voltage	$I_{test} = 1 \text{ mA}$		6	-	9	V
$I_{LR}$	reverse leakage current	per TMDS channel; V = 3 V		-	-	1	μΑ
V <sub>F</sub>	forward voltage	I <sub>test</sub> = 1 mA		-	0.7	-	V
C <sub>line</sub>	line capacitance	f = 1 MHz; $V_{bias} = 2.5 V$	<u>[1]</u>	-	0.6	-	pF
$\Delta C_{line}$	line capacitance difference	f = 1 MHz; $V_{bias} = 2.5 V$	[1]	-	0.05	-	pF
C <sub>line(mutual)</sub>	mutual line capacitance	f = 1 MHz; $V_{bias} = 2.5 V$	[1][2]	-	0.07	-	pF
r <sub>dyn</sub>	dynamic resistance	surge	[3]				
		positive transient		-	8.0	-	Ω
		negative transient		-	0.85	-	Ω
V <sub>CL</sub>	clamping voltage	positive transient; I <sub>PP</sub> = 3.8 A	[3]	-	9.5	-	V
		negative transient; $I_{PP} = -2.8 \text{ A}$	[3]	-	-3.2	-	V

<sup>[1]</sup> This parameter is guaranteed by design.

<sup>[2]</sup> Between signal pin and pin n.c.

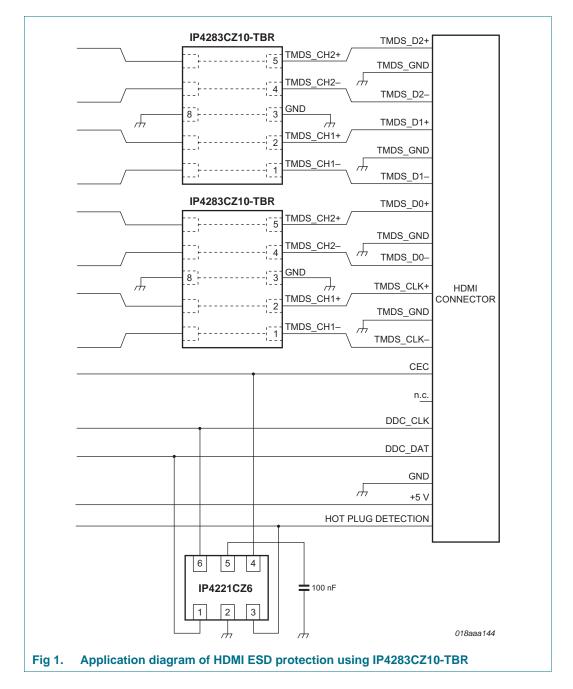
<sup>[3]</sup> According to IEC 61000-4-5 (8/20  $\mu$ s).

## 7. Application information

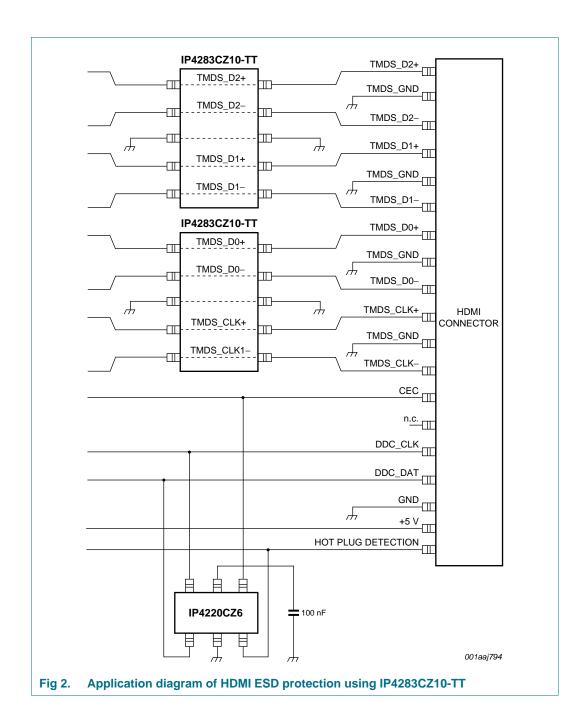
The devices are designed to provide high-level ESD protection for high-speed serial data buses such as HDMI, DisplayPort, eSATA and LVDS data lines.

When designing the Printed-Circuit Board (PCB), give careful consideration to impedance matching, and signal coupling.

Basic application diagrams for the ESD protection of an HDMI interface are shown in Figure 1 and  $\underline{2}$ .



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## 8. Package outline

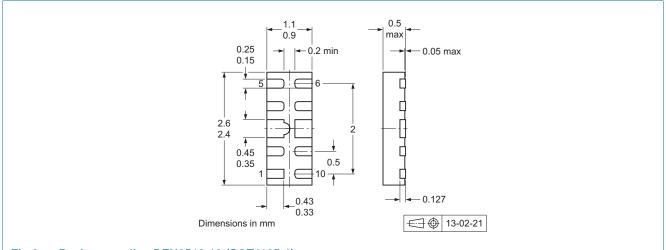


Fig 3. Package outline DFN2510-10 (SOT1165-1)

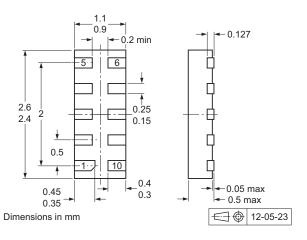


Fig 4. Package outline DFN2510A-10 (SOT1176-1)

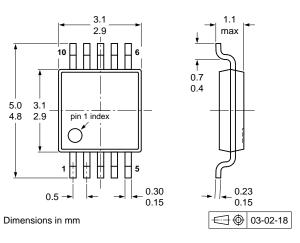


Fig 5. Package outline TSSOP10 (SOT552-1)

## 9. Soldering

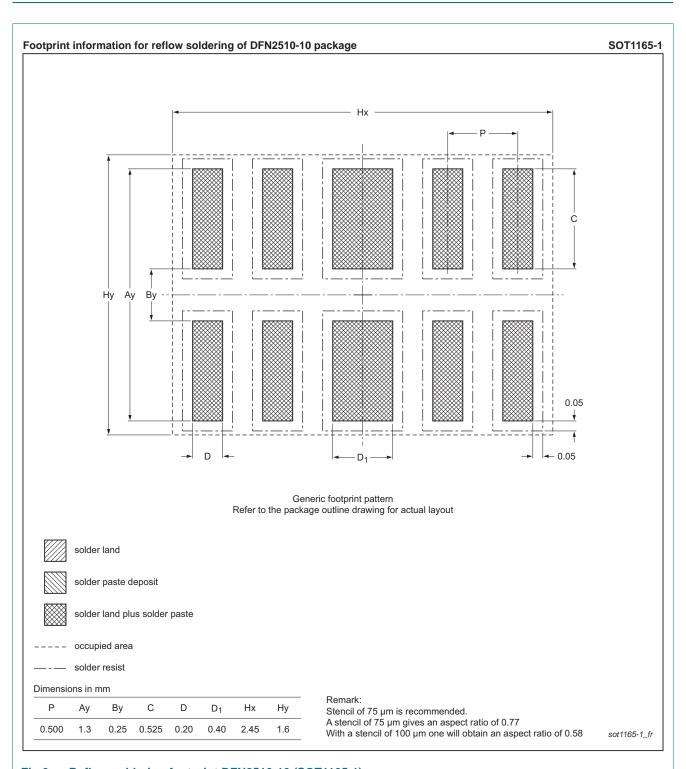
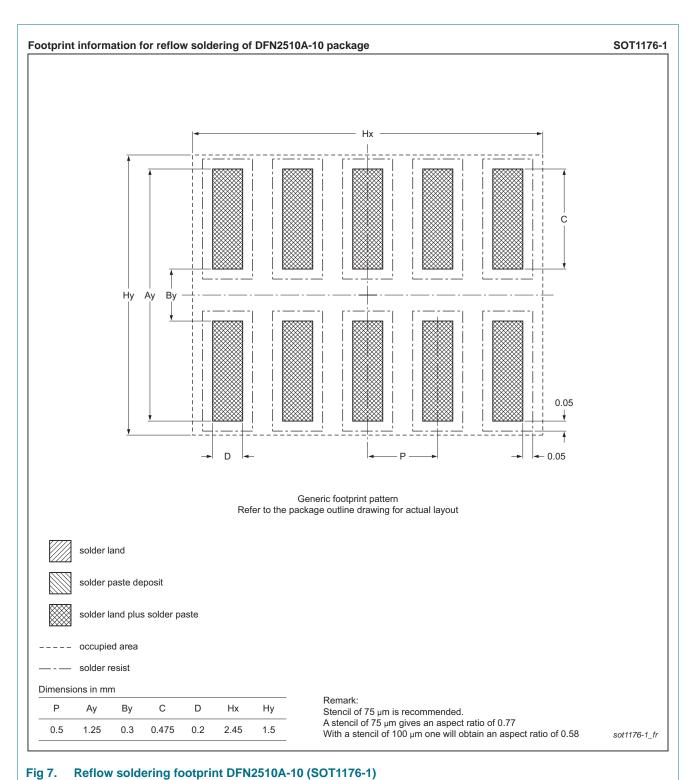
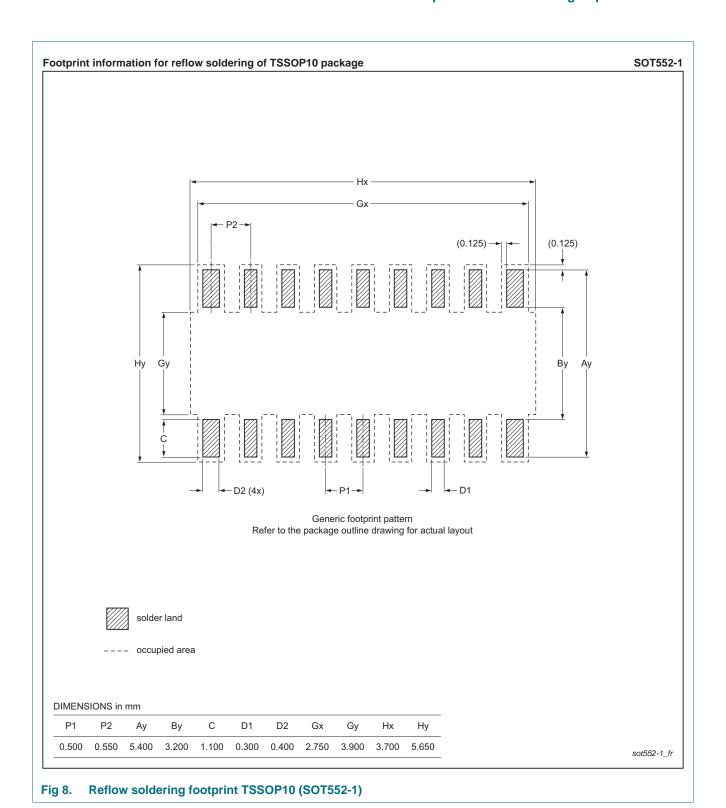


Fig 6. Reflow soldering footprint DFN2510-10 (SOT1165-1)





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## 10. Revision history

### Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4283CZ10_SER v.4	20130408	Product data sheet	-	IP4283CZ10_SER v.3
Modifications:	Section 1.1	"General description": upd	ated	
	• Section 1.2	"Features and benefits": u	pdated	
	<ul> <li>Section 2 "F</li> </ul>	Pinning information": updat	ed	
	<ul> <li>Section 3 "C</li> </ul>	Ordering information": upda	ated	
	• Table 5 "Ch	aracteristics": updated; r <sub>dyr</sub>	n value corrected	
	<ul> <li>Section 8 "F</li> </ul>	Package outline": drawings	replaced with minimized	I package outline drawings
	Section 9 "S	Soldering": updated		
	<ul><li>Section 11 '</li></ul>	"Legal information": update	d	
IP4283CZ10_SER v.3	20110624	Product data sheet	-	IP4283CZ10_SER v.2
IP4283CZ10_SER v.2	20100827	Product data sheet	-	IP4283CZ10 v.1
IP4283CZ10 v.1	20090507	Product data sheet		

### 11. Legal information

#### 11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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# IP4283CZ10 series

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ESD protection for ultra high-speed interfaces

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