MIC4423/4/5

Dual 3A Peak Low-Side MOSFET Drivers

Features

- Reliable, Low-Power Bipolar/CMOS/DMOS Construction
- Latch-Up Protected to >500 mA Reverse Current
- Logic Input Withstands Swing to –5V
- High 3A Peak Output Current
- Wide 4.5V to 18V Operating Range
- Drives 1800 pF Capacitance in 25 ns
- Short <40 ns Typical Delay Time
- Delay Times Consistent Within Supply Voltage Range
- Matched Rise and Fall Times
- TTL Logic Input Independent of Supply Voltage
- Low Equivalent 6 pF Input Capacitance
- Low Supply Current
  - 3.5 mA with Logic 1 Input
  - 350 µA with Logic 0 Input
- Low 3.5Ω Typical Output Impedance
- Output Voltage Swings within 25 mV of Ground or V_S.
- '426/7/8-, '1426/7/8-, '4426/7/8-Compatible Pinout
- Inverting, Non-Inverting, and Differential Configurations

General Description

The MIC4423/4424/4425 family are highly reliable BiCMOS/DMOS buffer/driver/MOSFET drivers. They are higher output current versions of the MIC4426/4427/4428, which are improved versions of the MIC426/427/428. All three families are pin-compatible. MIC4423 has dual inverting outputs, MIC4424 has dual non-inverting outputs, and MIC4425 has inverting and non-inverting outputs. The MIC4423/4424/4425 drivers are capable of giving reliable service in more demanding electrical environments than their predecessors. They will not latch under any conditions within their power and voltage ratings. They can survive up to 5V of noise spiking, of either polarity, on the ground pin. They can accept, without either damage or logic upset, up to half an amp of reverse current (either polarity) forced back into their outputs.

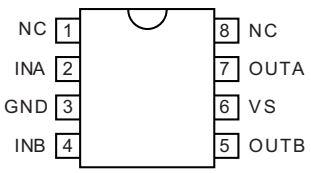
The MIC4423/4424/4425 series drivers are easier to use, more flexible in operation, and more forgiving than other CMOS or bipolar drivers currently available. Their BiCMOS/DMOS construction dissipates minimum power and provides rail-to-rail voltage swings.

Primarily intended for driving power MOSFETs, the MIC4423/4424/4425 drivers are suitable for driving other loads (capacitive, resistive, or inductive) that require low-impedance, high peak currents, and fast switching times. Heavily loaded clock lines, coaxial cables, or piezoelectric transducers are some examples. The only known limitation on loading is that total power dissipated in the driver must be kept within the maximum power dissipation limits of the package.

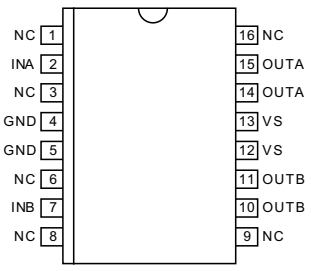
See MIC4123/4124/4125 for high power and narrow pulse applications.

Package Types

8-Pin DIP (N)
8-Pin SOIC (M)

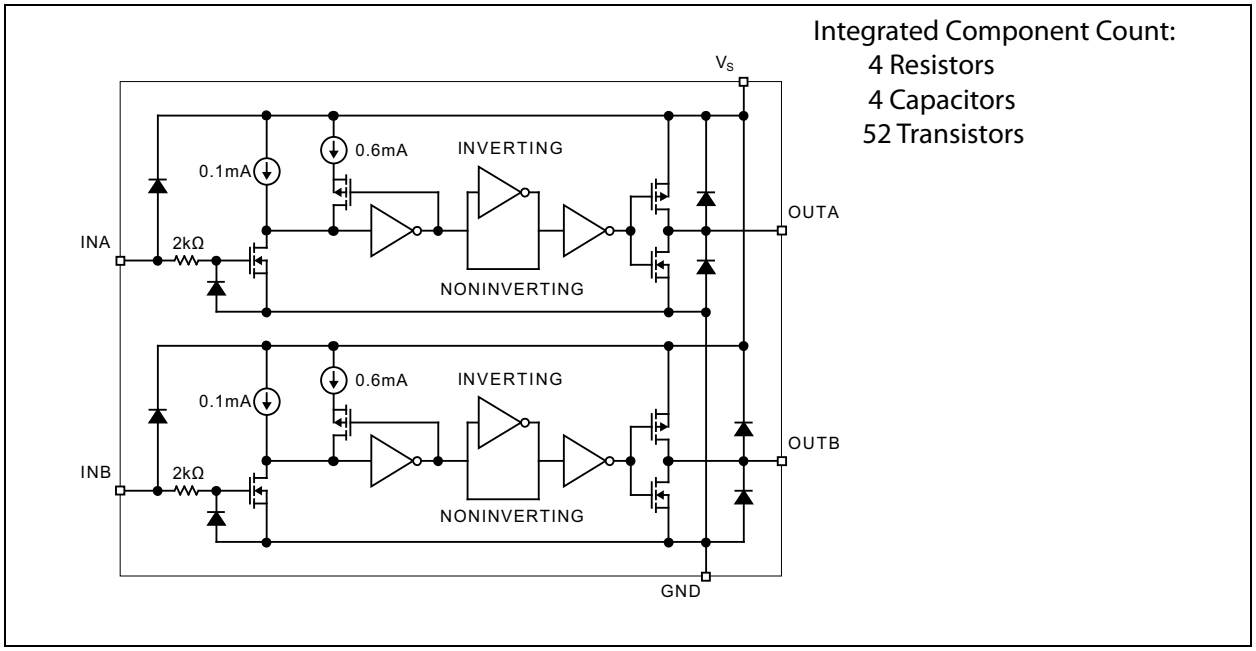


16-Pin Wide SOIC (WM)



Note: **WM Package:** Duplicate GND, VS, OUTA, and OUTB pins must be externally connected together.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage ..... +22V
Input Voltage ..... V_S + 0.3V to GND – 5V
ESD Susceptability, (Note 1) 1000V

Operating Ratings ‡

Supply Voltage (V_S) ..... +4.5V to +18V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability. Specifications are for packaged product only.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Characteristics: 4.5V ≤ V_S ≤ 18V; T_A = +25°C, **Bold** values indicate –40°C ≤ T_A ≤ +85°C; unless otherwise specified. Specifications for packaged product only.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input						
Logic 1 Input Voltage	V_{IH}	**2.4**	—	—	V	—
Logic 0 Input Voltage	V_{IL}	—	—	**0.8**	V	—
Input Current	I_{IN}	–1	—	1	µA	0V ≤ V_{IN} ≤ V_S
		–10	—	**10**		—
Output						
High Output Voltage	V_{OH}	**V_S–0.025**	—	—	V	—
Low Output Voltage	V_{OL}	—	—	**0.025**	V	—
Output Resistance HI State	R_O	—	2.8	5	Ω	I_{OUT} = 10 mA, V_S = 18V
		—	**3.7**	**8**	Ω	V_{IN} = 0.8V, I_{OUT} = 10 mA, V_S = 18V
Output Resistance LO State		—	3.5	5	Ω	I_{OUT} = 10 mA, V_S = 18V
		—	**4.3**	**8**	Ω	V_{IN} = 2.4V, I_{OUT} = 10 mA, V_S = 18V
Peak Output Resistance	I_{PK}	—	3	—	A	—
Latch-Up Protection Withstand Reverse Current	I	>500	—	—	mA	—

Electrical Characteristics: 4.5V ≤ V_S ≤ 18V; T_A = +25°C, **Bold** values indicate –40°C ≤ T_A ≤ +85°C; unless otherwise specified. Specifications for packaged product only.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Switching Time (Switching times ensured by design)						
Rise Time	t_R	—	23	35	ns	Figure 1-1, C_L = 1800 pF
		—	**28**	**60**		
Fall Time	t_F	—	25	35	ns	Figure 1-1, C_L = 1800 pF
		—	**32**	**60**		
Delay Time	t_{D1}	—	33	75	ns	Figure 1-1, C_L = 1800 pF
		—	**32**	**100**		
	t_{D2}	—	38	75	ns	Figure 1-1, C_L = 1800 pF
		—	**38**	**100**		
Pulse Width	t_{PW}	**400**	—	—	ns	Figure 1-1
Power Supply						
Power Supply Current	I_S	—	—	2.5	mA	V_{IN} = 3.0V (both inputs)
		—	—	**3.5**		
		—	—	0.25	mA	V_{IN} = 0.0V (both inputs)
		—	—	**0.3**		

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Maximum Junction Temperature	$T_{J(MAX)}$	—	—	+150	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	T_{LEAD}	—	—	+300	°C	—
Ambient Temperature Range	T_A	0	—	+70	°C	Z ordering option
		–40	—	+85	°C	Y ordering option
Package Thermal Resistances						
Thermal Resistance DIP	θ_{JA}	—	130	—	°C/W	—
Thermal Resistance DIP	θ_{JC}	—	42	—		—
Thermal Resistance Wide-SOIC	θ_{JA}	—	120	—		—
Thermal Resistance Wide-SOIC	θ_{JC}	—	75	—		—
Thermal Resistance SOIC	θ_{JA}	—	120	—		—
Thermal Resistance SOIC	θ_{JC}	—	75	—		—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}).

Test Circuit

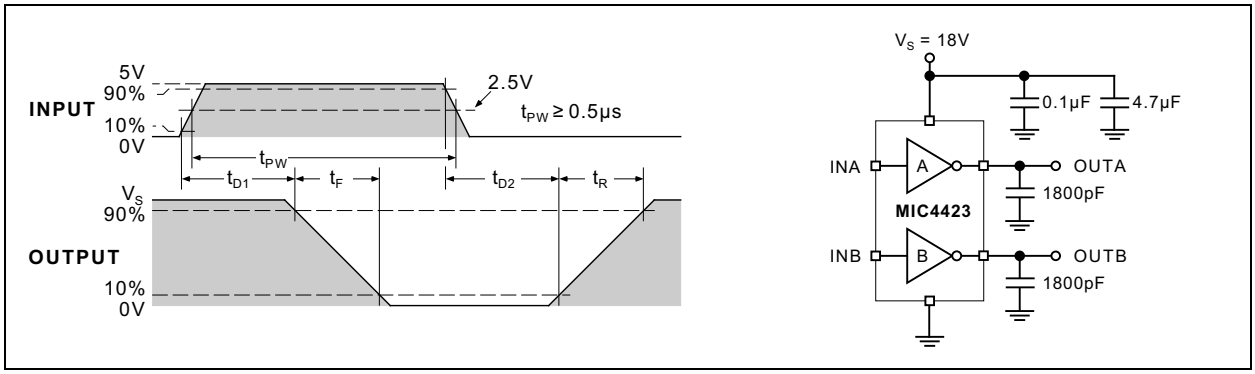


FIGURE 1-1: *Inverting Driver Switching Time.*

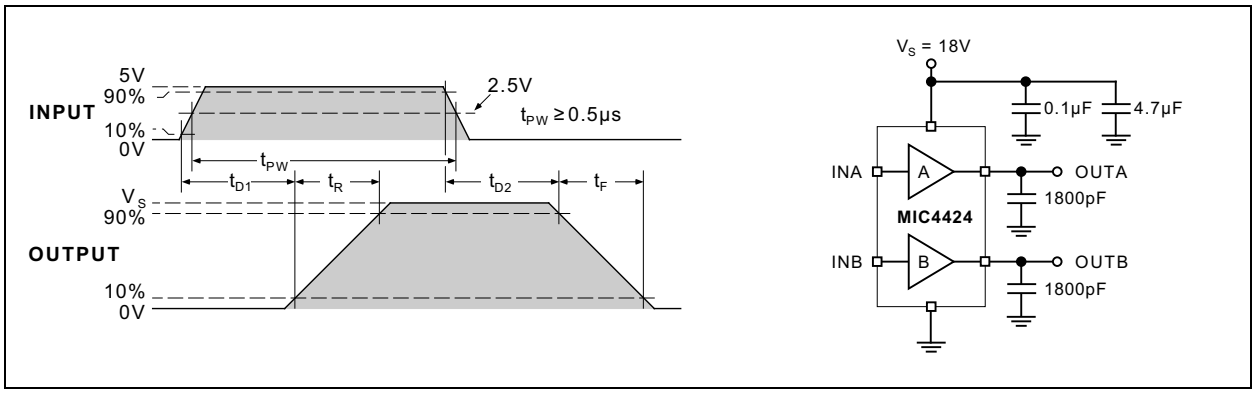


FIGURE 1-2: *Non-Inverting Driver Switching Time.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

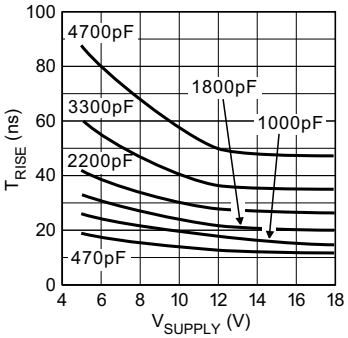


FIGURE 2-1: *Rise Time vs. Supply Voltage.*

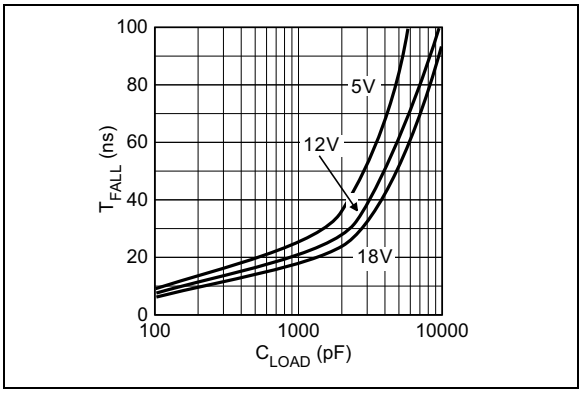


FIGURE 2-4: *Fall Time vs. Capacitive Load.*

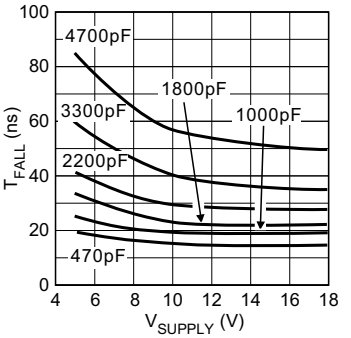


FIGURE 2-2: *Fall Time vs. Supply Voltage.*

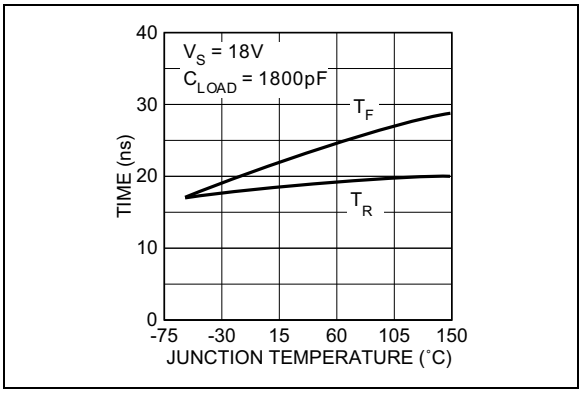


FIGURE 2-5: *Rise and Fall Time vs. Temperature.*

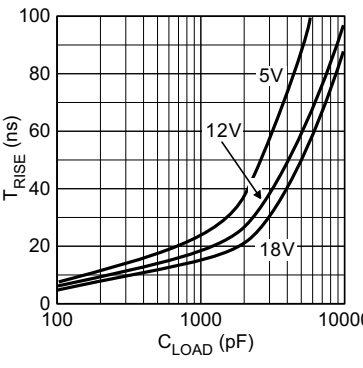


FIGURE 2-3: *Rise Time vs. Capacitive Load.*

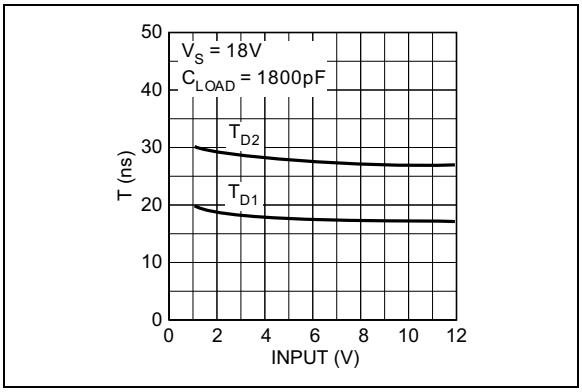


FIGURE 2-6: *Propagation Delay vs. Input Amplitude.*

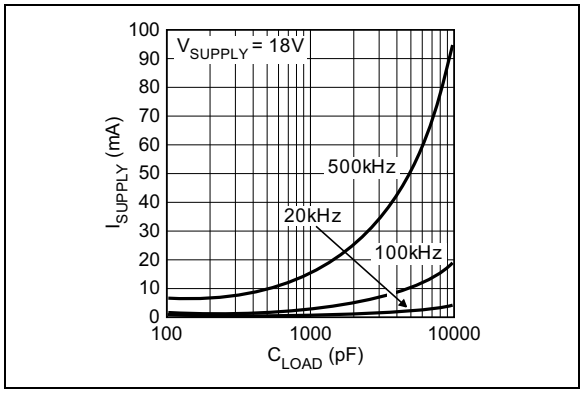


FIGURE 2-7: *Supply Current vs. Capacitive Load.*

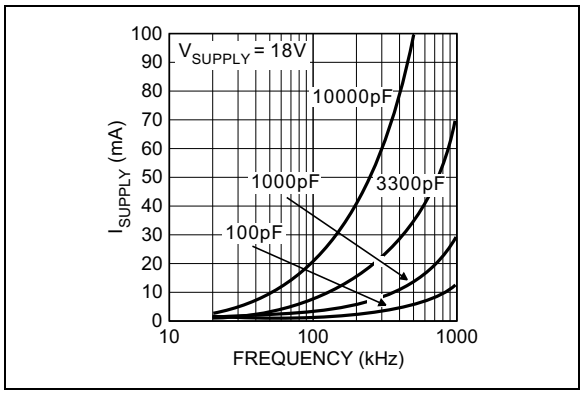


FIGURE 2-8: *Supply Current vs. Frequency.*

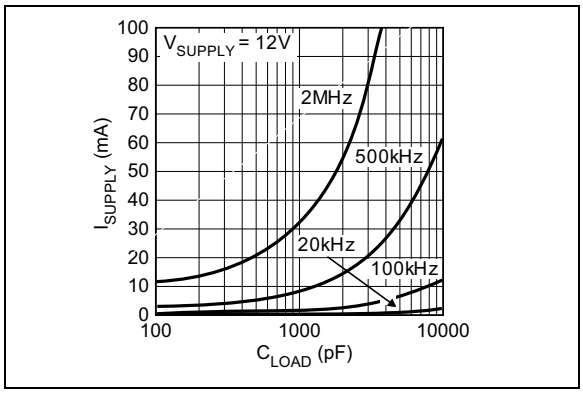


FIGURE 2-9: *Supply Current vs. Capacitive Load.*

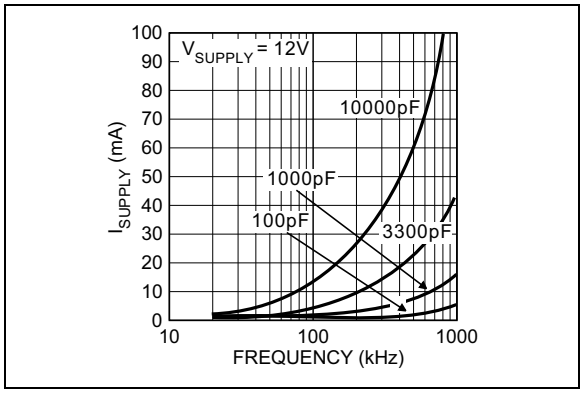


FIGURE 2-10: *Supply Current vs. Frequency.*

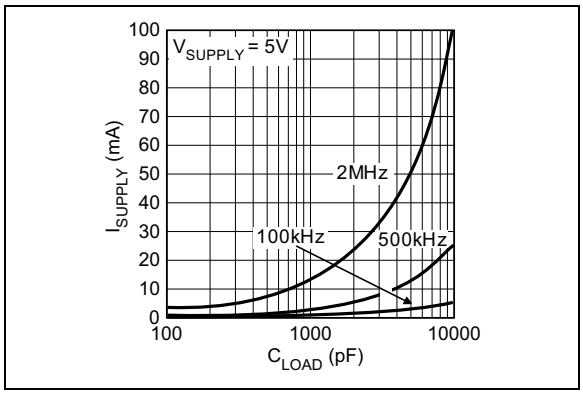


FIGURE 2-11: *Supply Current vs. Capacitive Load.*

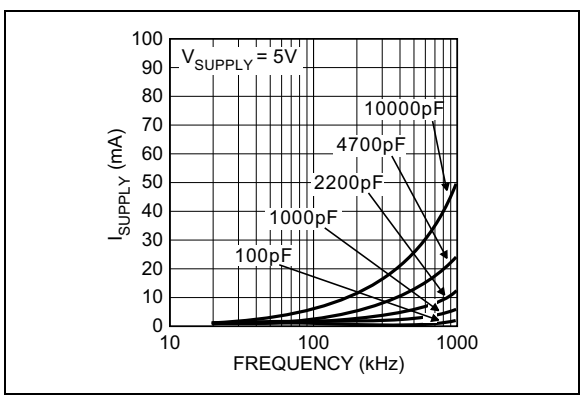


FIGURE 2-12: *Supply Current vs. Frequency.*

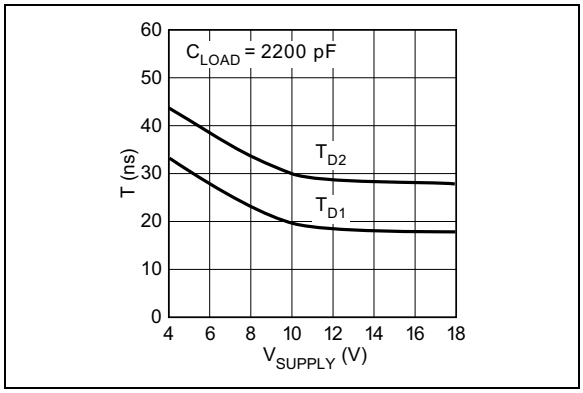


FIGURE 2-13: *Delay Time vs. Supply Voltage.*

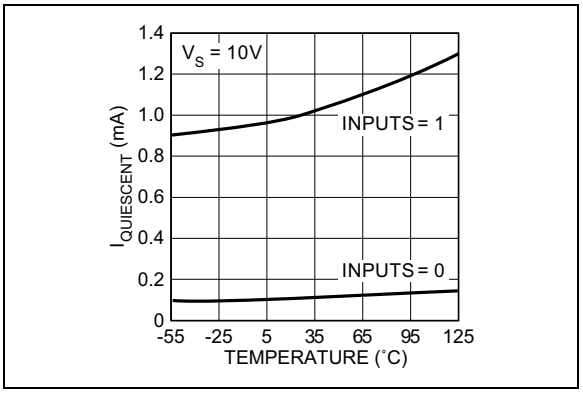


FIGURE 2-16: *Quiescent Current vs. Temperature.*

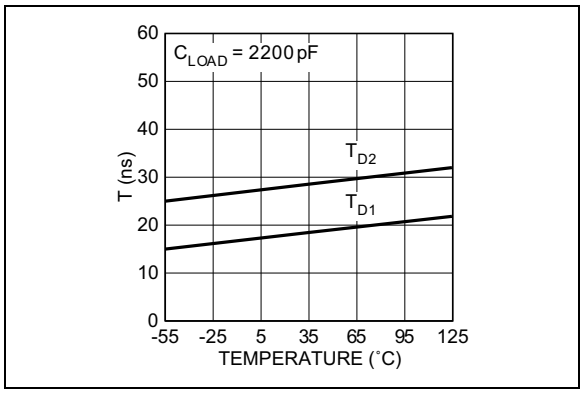


FIGURE 2-14: *Delay Time vs. Temperature.*

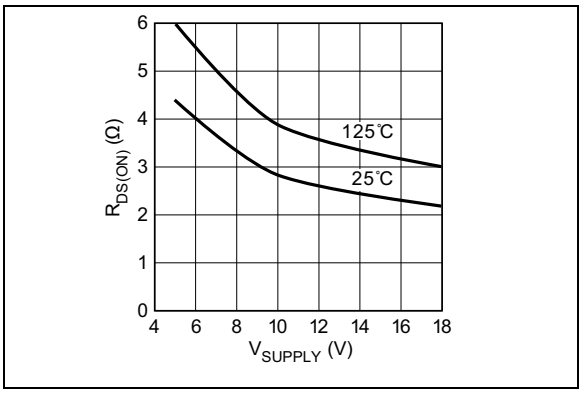


FIGURE 2-17: *Output Resistance (Output High) vs. Supply Voltage.*

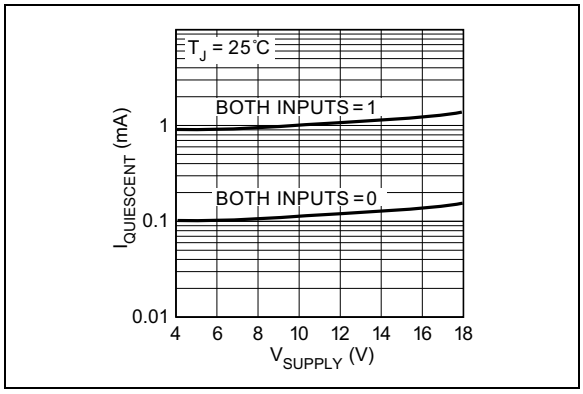


FIGURE 2-15: *Quiescent Supply Current vs. Voltage.*

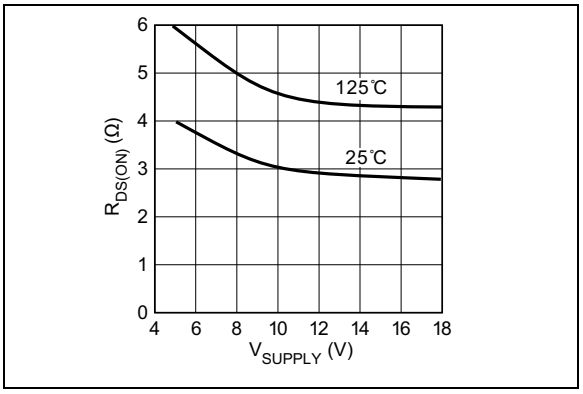


FIGURE 2-18: *Output Resistance (Output Low) vs. Supply Voltage.*

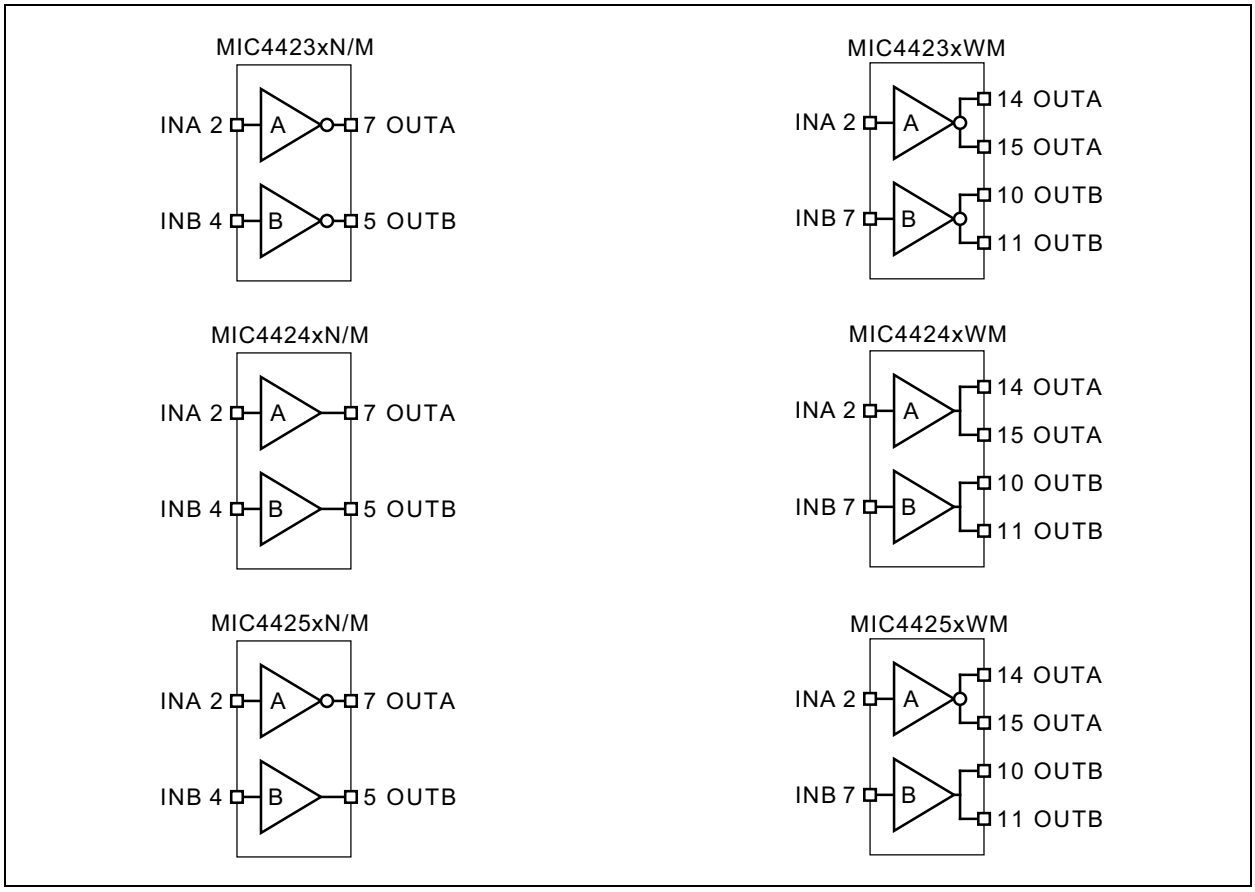
3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number DIP, SOIC	Pin Number Wide SOIC	Pin Name	Description
2/4	2/7	INA/B	Control Input.
3	4, 5	GND	Ground: Duplicate pins must be externally connected together.
6	12, 13	VS	Supply Input: Duplicate pins must be externally connected together.
7/5	14, 15/10, 11	OUTA/B	Output: Duplicate pins must be externally connected together.
1, 8	1, 3, 6, 8, 9, 16	NC	Not connected.

Device Configuration



4.0 APPLICATION INFORMATION

Although the MIC4423/4/5 drivers have been specifically constructed to operate reliably under any practical circumstances. There are, nonetheless, details of usage that will provide better operation of the device.

4.1 Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, charging 2000 pF from 0 to 15 volts in 20 ns requires a constant current of 1.5A. In practice, the charging current is not constant, and will usually peak at around 3A. In order to charge the capacitor, the driver must be capable of drawing this much current, this quickly, from the system power supply. In turn, this means that as far as the driver is concerned, the system power supply, as seen by the driver, must have a very low impedance.

As a practical matter, this means that the power supply bus must be capacitively bypassed at the driver with at least 100 times the load capacitance in order to achieve optimum driving speed. It also implies that the bypassing capacitor must have very low internal inductance and resistance at all frequencies of interest. Generally, this means using two capacitors, one a high-performance low ESR film, the other a low internal resistance ceramic, as together the valleys in their two impedance curves allow adequate performance over a broad enough band to get the job done. Please note that many film capacitors can be sufficiently inductive as to be useless for this service. Likewise, many multilayer ceramic capacitors have unacceptably high internal resistance. Use capacitors intended for high pulse current service. The high pulse current demands of capacitive drivers also mean that the bypass capacitors must be mounted very close to the driver in order to prevent the effects of lead inductance or PCB land inductance from nullifying what you are trying to accomplish. For optimum results the sum of the lengths of the leads and the lands from the capacitor body to the driver body should total 2.5 cm or less.

Bypass capacitance, and its close mounting to the driver serves two purposes. Not only does it allow optimum performance from the driver, it minimizes the amount of lead length radiating at high frequency during switching, (due to the large ΔI) thus minimizing the amount of EMI later available for system disruption and subsequent cleanup. It should also be noted that the actual frequency of the EMI produced by a driver is not the clock frequency at which it is driven, but is related to the highest rate of change of current produced during switching, a frequency generally one or two orders of magnitude higher, and thus more difficult to filter if you let it permeate your system. **Good bypassing practice is essential for proper operation of high speed driver ICs.**

4.2 Grounding

Both proper bypassing and proper grounding are necessary for optimum driver operation. Bypassing capacitance only allows a driver to turn the load ON. Eventually (except in rare circumstances) it is also necessary to turn the load OFF. This requires attention to the ground path. Two things other than the driver affect the rate at which it is possible to turn a load off: The adequacy of the grounding available for the driver, and the inductance of the leads from the driver to the load. The latter will be discussed in a separate section.

Best practice for a ground path is obviously a well laid out ground plane. However, this is not always practical, and a poorly-laid out ground plane can be worse than none.Attention to the paths taken by return currents even in a ground plane is essential. In general, the leads from the driver to its load, the driver to the power supply, and the driver to whatever is driving it should all be as low in resistance and inductance as possible. Of the three paths, the ground lead from the driver to the logic driving it is most sensitive to resistance or inductance, and ground current from the load are what is most likely to cause disruption. Thus, these ground paths should be arranged so that they never share a land, or do so for as short a distance as is practical.

To illustrate what can happen, consider the following: The inductance of a 2 cm long land, 1.59 mm (0.062") wide on a PCB with no ground plane is approximately 45 nH. Assuming a dl/dt of 0.3 A/ns (which will allow a current of 3A to flow after 10 ns, and is thus slightly slow for our purposes) a voltage of 13.5 volts will develop along this land in response to our postulated ΔI. For a 1 cm land, (approximately 15 nH) 4.5 volts is developed. Either way, anyone using TTL level input signals to the driver will find that the response of their driver has been seriously degraded by a common ground path for input to and output from the driver of the given dimensions. Note that this is before accounting for any resistive drops in the circuit. The resistive drop in a 1.59 mm (0.062") land of 2 oz. Copper carrying 3A will be about 4 mV/cm (10 mV/in) at DC, and the resistance will increase with frequency as skin effect comes into play.

The problem is most obvious in inverting drivers where the input and output currents are in phase so that any attempt to raise the driver's input voltage (in order to turn the driver's load off) is countered by the voltage developed on the common ground path as the driver attempts to do what it was supposed to. It takes very little common ground path, under these circumstances, to alter circuit operation drastically.

4.3 Output Lead Inductance

The same descriptions just given for PCB land inductance apply equally well for the output leads from a driver to its load, except that commonly the load is located much further away from the driver than the driver's ground bus.

Generally, the best way to treat the output lead inductance problem, when distances greater than 4 cm (2") are involved, requires treating the output leads as a transmission line. Unfortunately, as both the output impedance of the driver and the input impedance of the MOSFET gate are at least an order of magnitude lower than the impedance of common coax, using coax is seldom a cost-effective solution. A twisted pair works about as well, is generally lower in cost, and allows use of a wider variety of connectors. The second wire of the twisted pair should carry common from as close as possible to the ground pin of the driver directly to the ground terminal of the load. Do not use a twisted pair where the second wire in the pair is the output of the other driver, as this will not provide a complete current path for either driver. Likewise, do not use a twisted triad with two outputs and a common return unless both of the loads to be driver are mounted extremely close to each other, and you can guarantee that they will never be switching at the same time.

For output leads on a printed circuit, the general rule is to make them as short and as wide as possible. The lands should also be treated as transmission lines: i.e. minimize sharp bends, or narrowings in the land, as these will cause ringing. For a rough estimate, on a 1.59 mm (0.062") thick G-10 PCB a pair of opposing lands each 2.36 mm (0.093") wide translates to a characteristic impedance of about 50Ω. Half that width suffices on a 0.787 mm (0.031") thick board. For accurate impedance matching with a MIC4423/24/25 driver, on a 1.59 mm (0.062") board a land width of 42.75 mm (1.683") would be required, due to the low impedance of the driver and (usually) its load. This is obviously impractical under most circumstances. Generally the trade-off point between lands and wires comes when lands narrower than 3.18 mm (0.125") would be required on a 1.59 mm (0.062") board.

To obtain minimum delay between the driver and the load, it is considered best to locate the driver as close as possible to the load (using adequate bypassing). Using matching transformers at both ends of a piece of coax, or several matched lengths of coax between the driver and the load, works in theory, but is not optimum.

4.4 Driving at Controlled Rates

Occasionally there are situations where a controlled rise or fall time (which may be considerably longer than the normal rise or fall time of the driver's output) is desired for a load. In such cases it is still prudent to employ best possible practice in terms of bypassing, grounding and PCB layout, and then reduce the switching speed of the load (not the driver) by adding a non-inductive series resistor of appropriate value between the output of the driver and the load. For situations where only rise or only fall should be slowed, the resistor can be paralleled with a fast diode so that switching in the other direction remains fast. Due to the Schmitt trigger action of the driver's input it is not possible to slow the rate of rise (or fall) of the driver's input signal to achieve slowing of the output.

4.5 Input Stage

The input stage of the MIC4423/24/25 consists of a single-MOSFET class A stage with an input capacitance of ≤38 pF.

This capacitance represents the maximum load from the driver that will be seen by its controlling logic. The drain load on the input MOSFET is a –2 mA current source. Thus, the quiescent current drawn by the driver varies, depending on the logic state of the input.

Following the input stage is a buffer stage which provides ~400 mV of hysteresis for the input, to prevent oscillations when slowly-changing input signals are used or when noise is present on the input. Input voltage switching threshold is approximately 1.5V which makes the driver directly compatible with TTL signals, or with CMOS powered from any supply voltage between 3V and 15V.

The MIC4423/24/25 drivers can also be driven directly by the SG1524/25/26/27, TL494/95, TL594/95, NE5560/61/62/68, TSC170, MIC38C42, and similar switch mode power supply ICs. By relocating the main switch drive function into the driver rather than using the somewhat limited drive capabilities of a PWM IC. The PWM IC runs cooler, which generally improves its performance and longevity, and the main switches switch faster, which reduces switching losses and increase system efficiency.

The input protection circuitry of the MIC4423/24/25, in addition to providing 2 kV or more of ESD protection, also works to prevent latch-up or logic upset due to ringing or voltage spiking on the logic input terminal. In most CMOS devices when the logic input rises above the power supply terminal, or descends below the ground terminal, the device can be destroyed or rendered inoperable until the power supply is cycled OFF and ON. The MIC4423/24/25 drivers have been designed to prevent this. Input voltages excursions as great as 5V below ground will not alter the operation of the device. Input excursions above the power supply voltage will result in the excess voltage being conducted to the power supply terminal of the IC. Because the excess voltage is simply conducted to the power terminal, if the input to the driver is left in a high state when the power supply to the driver is turned off, currents as high as 30 mA can be conducted through the driver from the input terminal to its power supply terminal. This may overload the output of whatever is

driving the driver, and may cause other devices that share the driver's power supply, as well as the driver, to operate when they are assumed to be off, but it will not harm the driver itself. Excessive input voltage will also slow the driver down, and result in much longer internal propagation delays within the drivers. T_{D2}, for example, may increase to several hundred nanoseconds. In general, while the driver will accept this sort of misuse without damage, proper termination of the line feeding the driver so that line spiking and ringing are minimized, will always result in faster and more reliable operation of the device, leave less EMI to be filtered elsewhere, be less stressful to other components in the circuit, and leave less chance of unintended modes of operation.

4.6 Power Dissipation

CMOS circuits usually permit the user to ignore power dissipation. Logic families such as 4000 series and 74Cxxx have outputs which can only source or sink a few milliamps of current, and even shorting the output of the device to ground or V_{CC} may not damage the device. CMOS drivers, on the other driver hand, are intended to source or sink several Amps of current. This is necessary in order to drive large capacitive loads at frequencies into the megahertz range. Package power dissipation of driver ICs can easily be exceeded when driving large loads at high frequencies. Care must therefore be paid to device dissipation when operating in this domain.

The Supply Current vs Frequency and Supply Current vs Load in the **Section 2.0 "Typical Performance Curves"** furnished with this data sheet aid in estimating power dissipation in the driver. Operating frequency, power supply voltage, and load all affect power dissipation.

Given the power dissipation in the device, and the thermal resistance of the package, junction operating temperature for any ambient is easy to calculate. For example, the thermal resistance of the 8-pin plastic DIP package, from the data sheet, is 150°C/W. In a 25°C ambient, then, using a maximum junction temperature of 150°C, this package will dissipate 960 mW.

Accurate power dissipation numbers can be obtained by summing the three sources of power dissipation in the device:

- Load power dissipation (P_L)
- Quiescent power dissipation (P_Q)
- Transition power dissipation (P_T)

Calculation of load power dissipation differs depending on whether the load is capacitive, resistive or inductive.

4.7 Resistive Load Power Dissipation

Dissipation caused by a resistive load can be calculated in the following Equation 4-1:

EQUATION 4-1:

$$P_L = I^2 \times R_O \times D$$

Where:

I = The current drawn by the load

R_O = The output resistance of the driver when the output is high, at the power supply voltage used (See **Section 2.0 "Typical Performance Curves"**)

D = Fraction of time the load is conducting (duty cycle)

4.8 Capacitive Load Power Dissipation

Dissipation caused by a capacitive load is simply the energy placed in, or removed from, the load capacitance by the driver. The energy stored in a capacitor is described in the following Equation 4-2:

EQUATION 4-2:

$$E = 1/2 \times C \times V^2$$

As this energy is lost in the driver each time the load is charged or discharged, for power dissipation calculations the 1/2 is removed. This equation also shows that it is good practice not to place more voltage in the capacitor than is necessary, as dissipation increases as the square of the voltage applied to the capacitor. For a driver with a capacitive load.

EQUATION 4-3:

$$P_L = f \times C(V_S)^2$$

Where:

f = Operating frequency

C = Load capacitance

V_S = Driver supply voltage

4.9 Inductive Load Power Dissipation

For inductive loads the situation is more complicated. For the part of the cycle in which the driver is actively forcing current into the inductor, the situation is the same as it is in the resistive case:

EQUATION 4-4:

$$P_{L1} = I^2 \times R_O \times D$$

However, in this instance the R_O required may be either the on resistance of the driver when its output is in the high state, or its on resistance when the driver is in the low state, depending on how the inductor is connected, and this is still only half the story. For the part of the cycle when the inductor is forcing current through the driver, dissipation is best described as:

EQUATION 4-5:

$$P_{L2} = I \times V_D(1 - D)$$

Where:

V_D = The forward drop of the clamp diode in the driver (generally around 0.7V).

The two parts of the load dissipation must be summed in to produce P_L.

EQUATION 4-6:

$$P_L = P_{L1} + P_{L2}$$

4.10 Quiescent Power Dissipation

Quiescent power dissipation (P_Q, as described in the input section) depends on whether the input is high or low. A low input will result in a maximum current drain (per driver) of ≤0.2 mA; a logic high will result in a current drain of ≤2.0 mA. Quiescent power can therefore be found from:

EQUATION 4-7:

$$P_Q = V_S[D \times I_H + (1 - D) \times I_L]$$

Where:

I_H = Quiescent current with input high

I_L = Quiescent current with input low

D = Fraction of time input is high (duty cycle)

V_S = Power supply voltage

4.11 Transition Power Dissipation

Transition power is dissipated in the driver each time its output changes state, because during the transition, for a very brief interval, both the N-Channel and P-Channel MOSFETs in the output totem-pole are ON simultaneously, and a current is conducted through them from V_S to ground. The transition power dissipation is approximately:

EQUATION 4-8:

$$P_T = f \times V_S(A \times s)$$

Where:

(A x s) = A time current factor derived from Figure 4-1

Total power (P_D) then, is described as:

EQUATION 4-9:

$$P_D = P_L + P_Q + P_T$$

Examples show the relative magnitude for each term.

EXAMPLE 1: The MIC4423 operating on a 12V supply driving two capacitive loads of 3000 pF each, operating at 250 kHz, with a duty cycle of 50%, in a maximum ambient of 60°C.

First, calculate load power loss:

$$P_L = f \times C \times (V_S)^2$$

$$P_L = 250,000 \times (3 \times 10^{-9} + 3 \times 10^{-9}) \times 12^2 = 0.2160 W$$

Then, transition power loss:

$$P_T = f \times V_S \times (A \times s)$$
$$= 250,000 \times 12 \times 2.2 \times 10^{-9} = 6.6 mW$$

Then quiescent power loss:

$$P_Q = V_S[D \times I_H + (1 - D) \times I_L]$$
$$= 12 \times [(0.5 \times 0.0035) + (0.5 \times 0.0003)]$$
$$= 0.0228 W$$

Total power dissipation, then, is:

$$P_D = 0.2160 + 0.0066 + 0.0228 = 0.2454 W$$

Assuming an SOIC package, with θ_{JA} of 120°C/W, this will result in the junction running at 29.4°C above ambient.

$$0.2454 \times 120 = 29.4°C$$

Given a maximum ambient temperature of 60°C, this will result in a maximum junction temperature of 89.4°C.

EXAMPLE 2: A MIC4424 operating on a 15V input, with one driver driving a 50Ω resistive load at 1 MHz, with a duty cycle of 67%, and the other driver quiescent, in a maximum ambient temperature of 40°C:

$$P_L = I^2 \times R_O \times D$$

First, I_O must be determined.

$$I_O = V_S / (R_O + R_{LOAD})$$

Given R_O from the characteristic curves then:

$$I_O = 15 / (3.3 + 50)$$

$$I_O = 0.281 A$$

and:

$$P_L = (0.281)^2 \times 3.3 \times 0.67 = 0.174 W$$
$$P_T = F \times V_S \times (A \times s) / 2$$

because only one side is operating,

$$= (1,000,000 \times 15 \times 3.3 \times 10^{-9}) / 2 = 0.025 W$$

and

$$P_Q = 15 \times [(0.67 \times 0.00125) + (0.33 \times 0.000125) + (1 \times 0.000125)]$$

this assumes that the unused side of the driver has its input grounded, which is more efficient = 0.015W.

Then,

$$P_D = 0.174 + 0.025 + 0.0150 = 0.213 W$$

In a ceramic package with an θ_{JA} of 100°C/W, this amount of power results in a junction temperature given the maximum 40°C ambient of:

$$(0.213 \times 100) + 40 = 61.4°C$$

The actual junction temperature will be lower than calculated both because duty cycle is less than 100% and because the graph lists $R_{DS(ON)}$ at a T_J of 125°C and the $R_{DS(ON)}$ at 61°C T_J will be somewhat lower.

4.12 Definitions

C_L = Load Capacitance in Farads.

D = Duty Cycle expressed as the fraction of time the input to the driver is high.

f = Operating Frequency of the driver in Hertz.

I_H = Power supply current drawn by a driver when both inputs are high and neither output is loaded.

I_L = Power supply current drawn by a driver when both inputs are low and neither output is loaded.

I_D = Output current from a driver in Amps.

P_D = Total power dissipated in a driver in Watts.

P_L = Power dissipated in the driver due to the driver's load in Watts.

P_Q = Power dissipated in a quiescent driver in Watts.

P_T = Power dissipated in a driver when the output changes states ("shoot-through current") in Watts. NOTE: The "shoot-through" current from a dual transition (once up, once down) for both drivers is stated in the graph on the following page in ampere-nanoseconds. This figure must be multiplied by the number of repetitions per second (frequency to find Watts).

R_O = Output resistance of a driver in Ohms.

V_S = Power supply voltage to the IC in Volts.

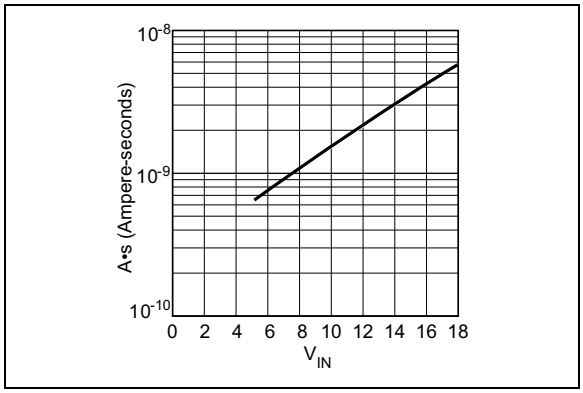


FIGURE 4-1: *Crossover Energy Loss.*

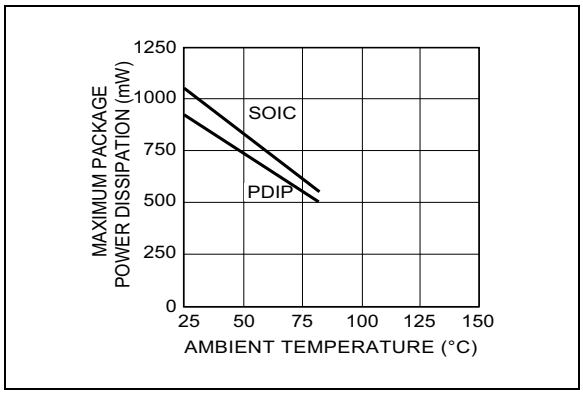


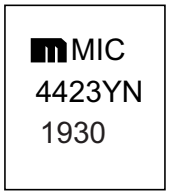
FIGURE 4-2: *Power Dissipation vs. Ambient Temperature.*

5.0 PACKAGING INFORMATION

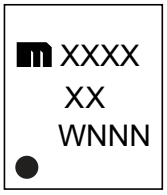
5.1 Package Marking Information

8-Lead PDIP*

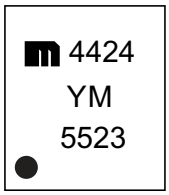
Example



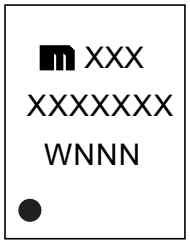
8-Lead SOIC*



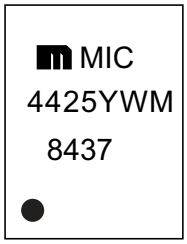
Example



16-Lead Wide SOIC*



Example

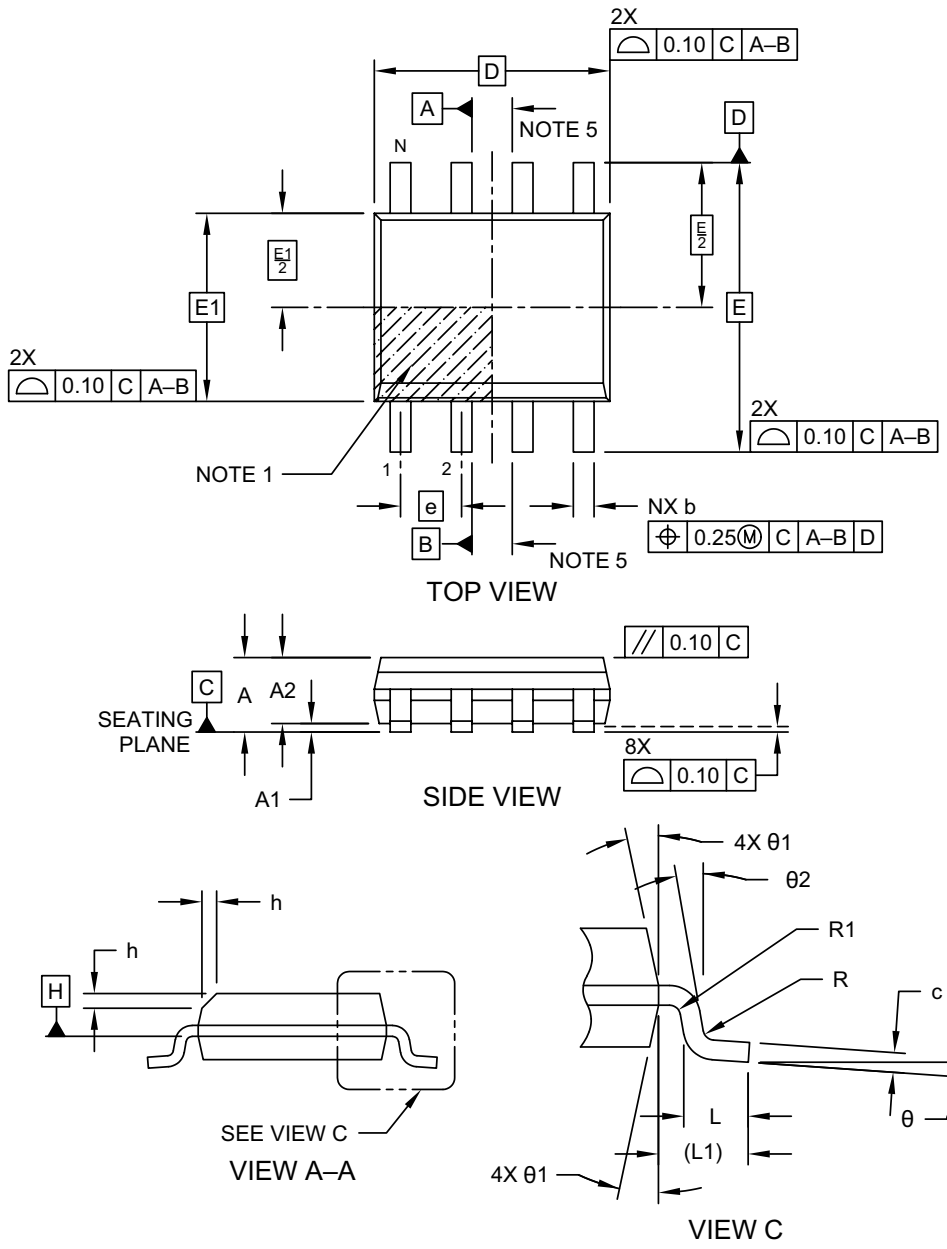


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

8-Lead SOIC Package Outline and Recommended Land Pattern

8-Lead Plastic Small Outline (3BX) - Narrow, 3.90 mm (.150 In.) Body [SOIC]
Atmel Legacy Global Package Code SWB

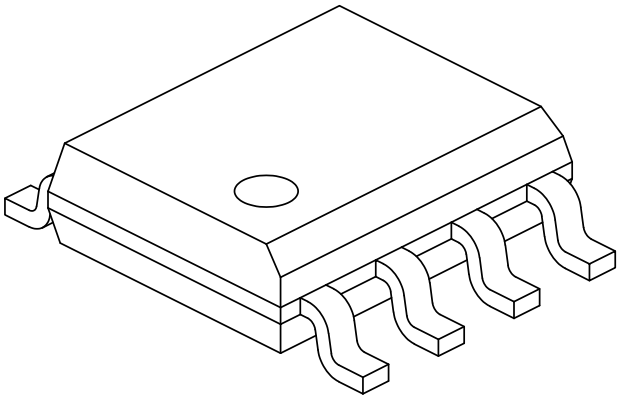
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-3BX Rev J Sheet 1 of 2

8-Lead Plastic Small Outline (3BX) - Narrow, 3.90 mm (.150 In.) Body [SOIC]
Atmel Legacy Global Package Code SWB

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	8°

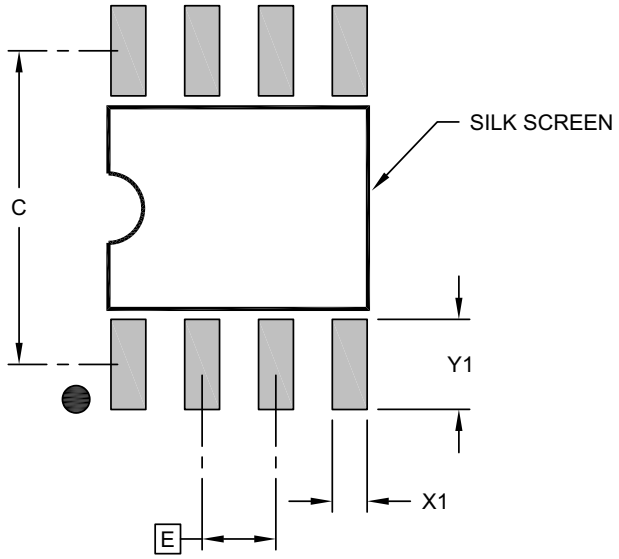
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-3BX Rev J Sheet 2 of 2

8-Lead Plastic Small Outline (3BX) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

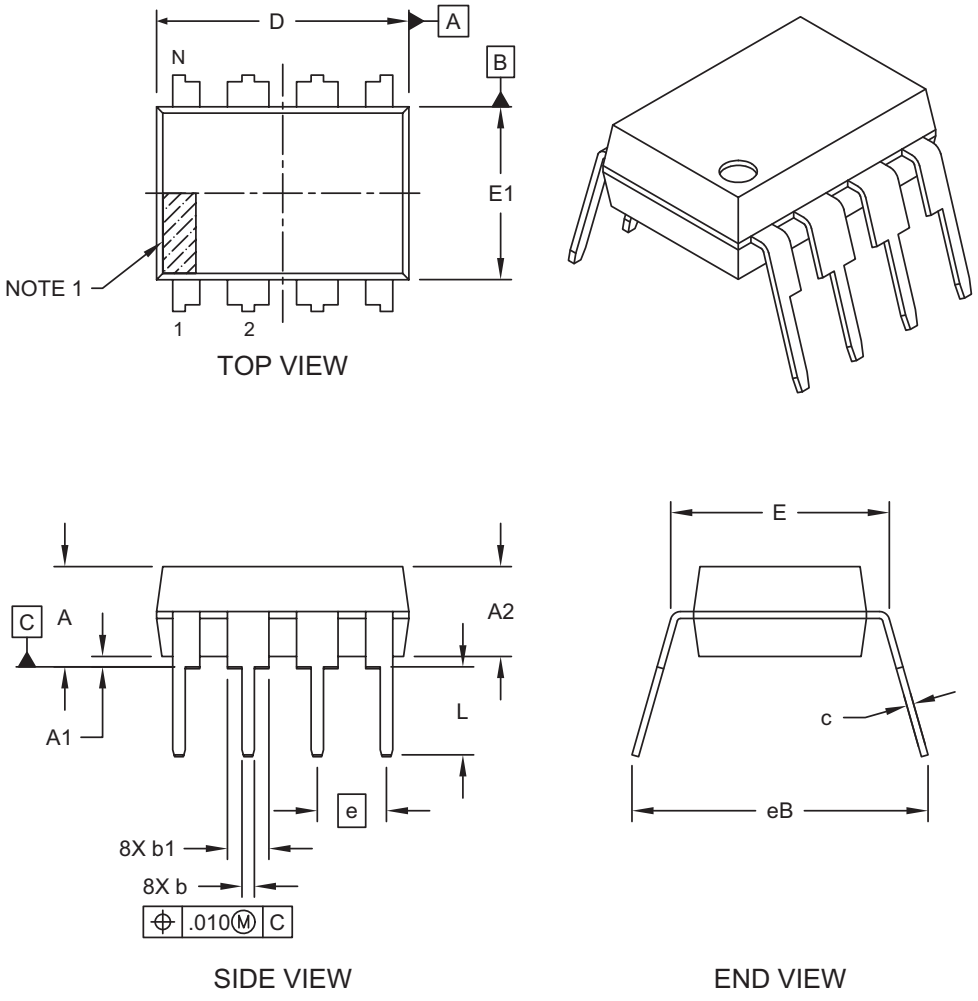
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-3BX Rev J

8-Lead PDIP Package Outline and Recommended Land Pattern

8-Lead Plastic Dual In-Line (PA) - 300 mil Body [PDIP]

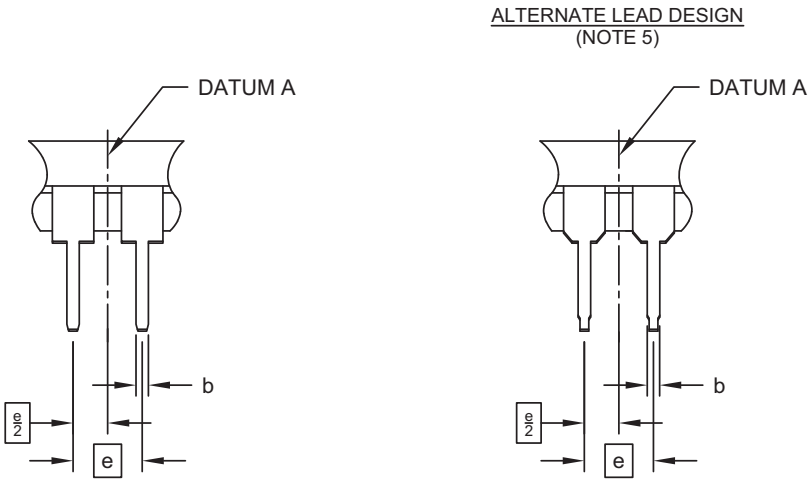
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-018-PA Rev F Sheet 1 of 2

8-Lead Plastic Dual In-Line (PA) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

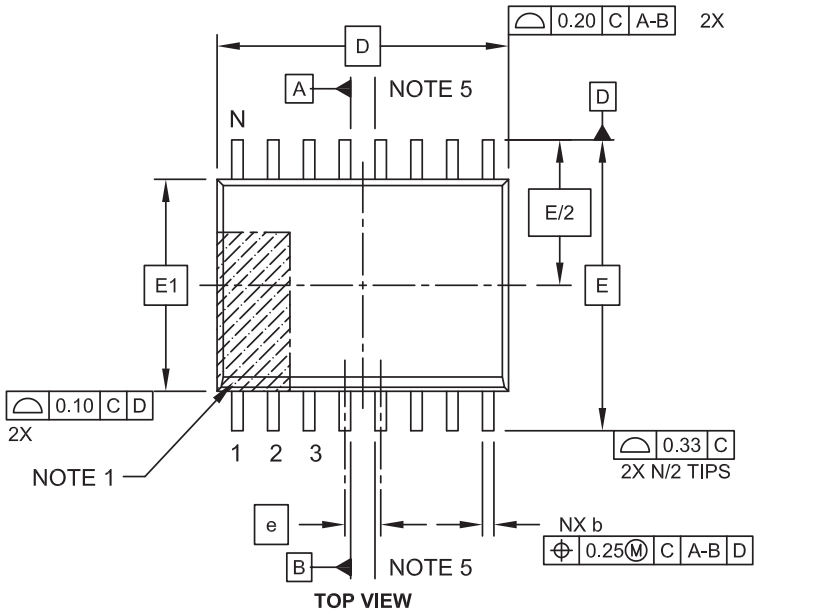
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-PA Rev F Sheet 2 of 2

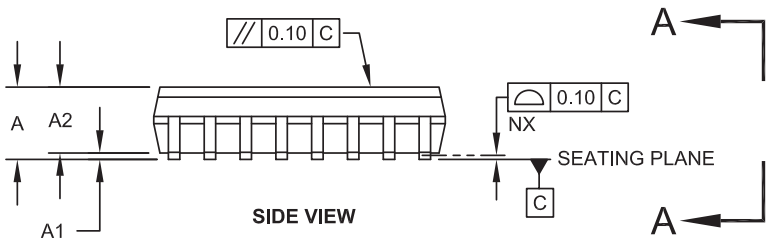
16-Lead Wide SOIC Package Outline and Recommended Land Pattern

16-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

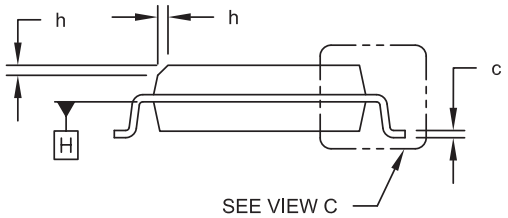
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

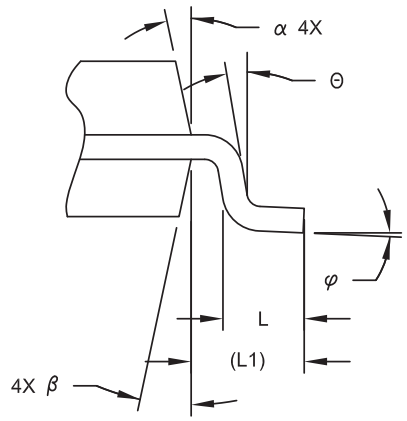


VIEW A-A

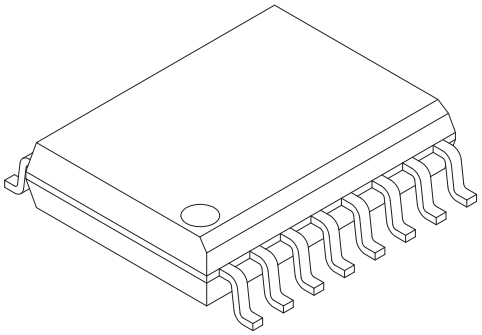
Microchip Technology Drawing C04-102C Sheet 1 of 2

16-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		10.30 BSC	
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1		1.40 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.20	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

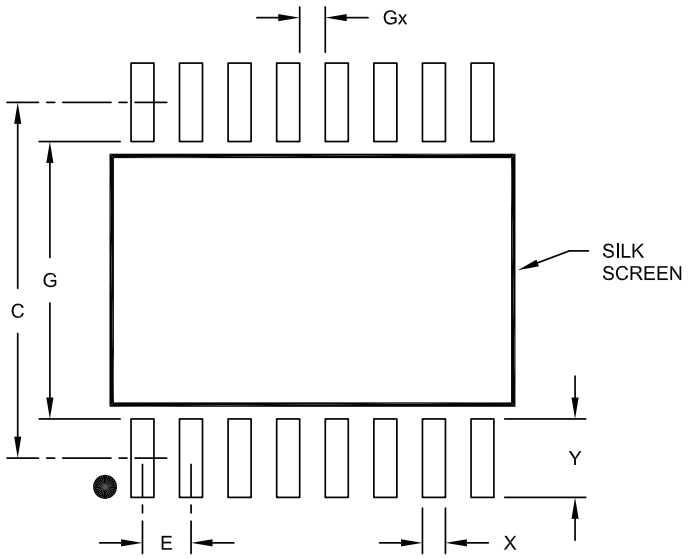
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-102C Sheet 2 of 2

16-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC] Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		9.30	
Contact Pad Width	X			0.60
Contact Pad Length	Y			2.05
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2102A

APPENDIX A: REVISION HISTORY

Revision A (May 2022)

- Converted Micrel document MIC4423/4/5 to Microchip data sheet DS20006638A.
- Minor text changes throughout.

Revision B (June 2022)

- Corrected examples in the Product Identification System to correctly reflect the orderable part numbers.
- Updated each of the package outline drawings in the Packaging Information section to their Microchip equivalents.

Revision C (July 2022)

- Updated Equation 4-1, Equation 4-4, and Example 1 in **Section 4.11 "Transition Power Dissipation"** to reflect the correct equations from the original Micrel data sheet.
- Removed temperature values from the Absolute Maximum Ratings † because they are already in the Temperature Specifications (Note 1) table.
- Ambient temperature ranges added to the Temperature Specifications (Note 1) table.
- Minor update to the Product Identification System for added clarity.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	XX	–XX
Device	Junction Temperature Range	Package	Media Type

Device:	MIC4423:	Dual 3A Peak Low-Side MOSFET Driver Bi-Polar/CMOS/DMOS Process, Dual Inverting
	MIC4424:	Dual 3A Peak Low-Side MOSFET Driver Bi-Polar/ CMOS/DMOS Process, Dual Non-Inverting
	MIC4425:	Dual 3A Peak Low-Side MOSFET Driver Bi-Polar/CMOS/DMOS Process, Inverting plus Non-Inverting
Junction Temperature Range:	Y =	–40°C to +85°C (RoHs Compliant)
	Z =	0°C to +70°C (RoHs Compliant)
Package:	N =	8-Lead PDIP
	M =	8-Lead SOIC
	WM =	16-Lead SOIC (Wide Body)
Media Type:	<blank> =	Tube
	TR =	Tape & Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Examples:

a) MIC4423Y:	**3A Peak, Dual Inverting High Speed, Low-Side MOSFET Driver, Industrial Grade, –40°C to +85°C Temperature Range, RoHS Compliant**
MIC4423YM	8-Lead SOIC Package, Tube
MIC4423YM-TR	8-Lead SOIC Package, Reel
MIC4423YN	8-Lead PDIP Package, Tube
MIC4423YWM	16-Lead SOIC Wide Package, Tube
MIC4423YWM-TR	16-Lead SOIC Wide Package, Reel
b) MIC4423Z:	**3A Peak, Dual Inverting High Speed, Low-Side MOSFET Driver, Commercial Grade, 0°C to +70°C Temperature Range, RoHS Compliant**
MIC4423ZN	8-Lead PDIP Package, Tube
MIC4423ZWM	16-Lead SOIC Wide Package, Tube
MIC4423ZWM-TR	16-Lead SOIC Wide Package, Reel
c) MIC4424Y:	**3A Peak, Dual Non-Inverting High Speed, Low-Side MOSFET Driver, Industrial Grade, –40°C to +85°C Temperature Range, RoHS Compliant**
MIC4424YM	8-Lead SOIC Package, Tube
MIC4424YM-TR	8-Lead SOIC Package, Reel
MIC4424YN	8-Lead PDIP Package, Tube
MIC4424YWM	16-Lead SOIC Wide Package, Tube
MIC4424YWM-TR	16-Lead SOIC Wide Package, Reel
d) MIC4424Z:	**3A Peak, Dual Non-Inverting High Speed, Low-Side MOSFET Driver, Commercial Grade, 0°C to +70°C Temperature Range, RoHS Compliant**
MIC4424ZN	8-Lead PDIP Package, Tube
MIC4424ZWM	16-Lead SOIC Wide Package, Tube
MIC4424ZWM-TR	16-Lead SOIC Wide Package, Reel
e) MIC4425Y:	**3A-Peak, Dual Inverting Plus Non-Inverting Hi-Speed, Low-Side MOSFET Driver, Industrial Grade, –40°C to +85°C Temperature Range, RoHS Compliant**
MIC4425YM	8-Lead SOIC Package, Tube
MIC4425YM-TR	8-Lead SOIC Package, Reel
MIC4425YN	8-Lead PDIP Package, Tube
MIC4425YWM	16-Lead SOIC Wide Package, Tube
MIC4425YWM-TR	16-Lead SOIC Wide Package, Reel
f) MIC4425Z:	**3A-Peak, Dual Inverting Plus Non-Inverting Hi-Speed, Low-Side MOSFET Driver, Commercial Grade, 0°C to +70°C Temperature Range, RoHS Compliant**
MIC4425ZWM	16-Lead SOIC Wide Package, Tube
MIC4425ZWM-TR	16-Lead SOIC Wide Package, Reel

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ISBN: 978-1-6683-0951-3

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