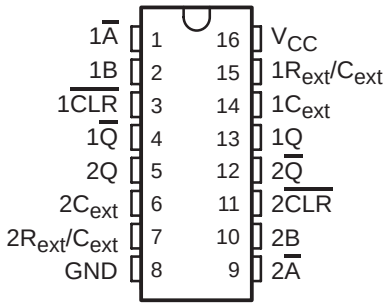
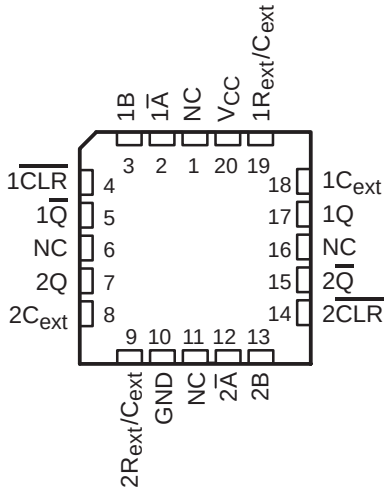
SCLS352H − JULY 1997 − REVISED OCTOBER 2005

- **Operating Range 2-V to 5.5-V V_{CC}**
- **Schmitt-Trigger Circuitry On $\overline{A}$, B, and $\overline{CLR}$ Inputs for Slow Input Transition Rates**
- **Edge Triggered From Active-High or Active-Low Gated Logic Inputs**
- **Retriggerable for Very Long Output Pulses**
- **Overriding Clear Terminates Output Pulse**
- **Glitch-Free Power-Up Reset On Outputs**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

SN54AHC123A . . . J OR W PACKAGE
SN74AHC123A . . . D, DB, DGV, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC123A . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

The ’AHC123A devices are dual retriggerable monostable multivibrators designed for 2-V to 5.5-V V_{CC} operation.

These edge-triggered multivibrators feature output pulse-duration control by three methods. In the first method, the $\overline{A}$ input is low, and the B input goes high. In the second method, the B input is high, and the $\overline{A}$ input goes low. In the third method, the $\overline{A}$ input is low, the B input is high, and the clear ($\overline{CLR}$) input goes high.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP − N	Tube	SN74AHC123AN	SN74AHC123AN
	SOIC − D	Tube	SN74AHC123AD	AHC123A
		Tape and reel	SN74AHC123ADR	
	SSOP − DB	Tape and reel	SN74AHC123ADBR	HA123A
	TSSOP − PW	Tape and reel	SN74AHC123APWR	HA123A
	TVSOP − DGV	Tape and reel	SN74AHC123ADGVR	HA123A
−55°C to 125°C	CDIP − J	Tube	SNJ54AHC123AJ	SNJ54AHC123AJ
	CFP − W	Tube	SNJ54AHC123AW	SNJ54AHC123AW
	LCCC − FK	Tube	SNJ54AHC123AFK	SNJ54AHC123AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

description/ordering information (continued)

The output pulse duration is programmed by selecting external resistance and capacitance values. The external timing capacitor must be connected between C_{ext} and R_{ext}/C_{ext} (positive) and an external resistor connected between R_{ext}/C_{ext} and V_{CC}. To obtain variable pulse durations, connect an external variable resistance between R_{ext}/C_{ext} and V_{CC}. The output pulse duration also can be reduced by taking $\overline{CLR}$ low.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. The $\overline{A}$, B, and $\overline{CLR}$ inputs have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the outputs.

Once triggered, the basic pulse duration can be extended by retriggering the gated low-level-active ($\overline{A}$) or high-level-active (B) input. Pulse duration can be reduced by taking $\overline{CLR}$ low. $\overline{CLR}$ input can be used to override $\overline{A}$ or B inputs. The input/output timing diagram illustrates pulse control by retriggering the inputs and early clearing.

The variance in output pulse duration from device to device typically is less than ±0.5% for given external timing components. An example of this distribution for the ’AHC123A is shown in Figure 10. Variations in output pulse duration versus supply voltage and temperature are shown in Figure 6.

During power up, Q outputs are in the low state, and $\overline{Q}$ outputs are in the high state. The outputs are glitch free, without applying a reset pulse.

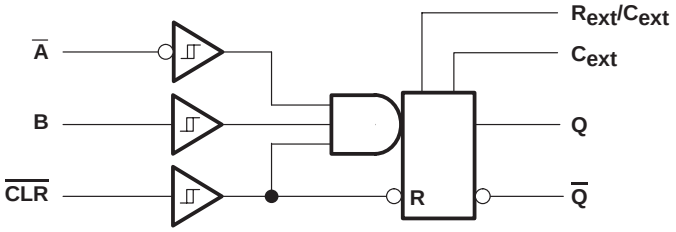
For additional application information on multivibrators, see the application report *Designing With the SN74AHC123A and SN74AHCT123A*, literature number SCLA014.

FUNCTION TABLE
(each multivibrator)

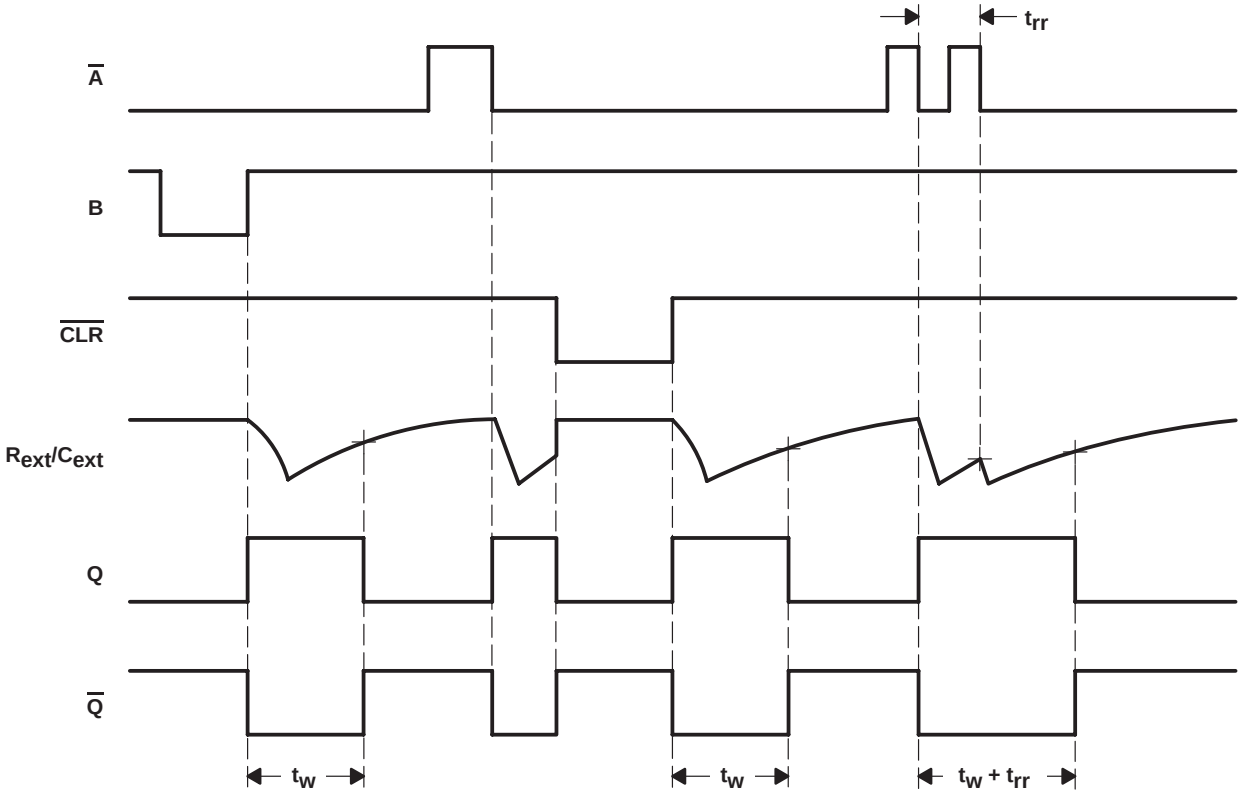
INPUTS			OUTPUTS	
$\overline{CLR}$	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L†	H†
X	X	L	L†	H†
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

† These outputs are based on the assumption that the indicated steady-state conditions at the $\overline{A}$ and B inputs have been set up long enough to complete any pulse started before the setup.

logic diagram, each multivibrator (positive logic)



input/output timing diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 2) . . . . . −0.5 V to 7 V
Output voltage range in high or low state, V_O (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage range in power-off state, V_O (see Note 1) . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} (V_I < 0) . . . . . −20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package . . . . . 73°C/W
DB package . . . . . 82°C/W
DGV package . . . . . 120°C/W
N package . . . . . 67°C/W
PW package . . . . . 108°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to the network ground terminal.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			SN54AHC123A		SN74AHC123A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		−50		−50	μA
		V_{CC} = 3.3 V ± 0.3 V		−4		−4	mA
		V_{CC} = 5 V ± 0.5 V		−8		−8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
R_{ext}	External timing resistance	V_{CC} = 2 V	5k		5k		Ω
		V_{CC} > 3 V	1k		1k		
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		1		1		ms/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused R_{ext}/C_{ext} terminals should be left unconnected. All remaining unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC123A		SN74AHC123A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
		I_{OH} = −4 mA	3 V	2.58			2.48		2.48		
		I_{OH} = −8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
			3 V			0.1		0.1		0.1	
			4.5 V			0.1		0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	R_{ext}/C_{ext}†	V_I = V_{CC} or GND	5.5 V			±0.25		±2.5		±2.5	μA
	$\overline{A}$, B, and $\overline{CLR}$	V_I = V_{CC} or GND	0 V to 5.5 V			±0.1		±1*		±1	
I_{CC}	Quiescent	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40	μA
I_{CC}	Active state (per circuit)	V_I = V_{CC} or GND, R_{ext}/C_{ext} = 0.5 V_{CC}	3 V		160	250		280		280	μA
			4.5 V		280	500		650		650	
			5.5 V		360	750		975		975	
C_i		V_I = V_{CC} or GND	5 V		1.9	10				10	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.
† This test is performed with the terminal in the off-state condition.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			TEST CONDITIONS	T_A = 25°C			SN54AHC123A		SN74AHC123A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$		5			5		5		ns
		$\overline{A}$ or B trigger		5			5		5		
t_{rr}	Pulse retrigger time		R_{ext} = 1 kΩ, C_{ext} = 100 pF	‡	76		‡		‡		ns
			R_{ext} = 1 kΩ, C_{ext} = 0.01 μF	‡	1.8		‡		‡		μs

‡ See retriggering data in the *application information* section.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			TEST CONDITIONS	T_A = 25°C			SN54AHC123A		SN74AHC123A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$		5			5		5		ns
		$\overline{A}$ or B trigger		5			5		5		
t_{rr}	Pulse retrigger time		R_{ext} = 1 kΩ, C_{ext} = 100 pF	‡	59		‡		‡		ns
			R_{ext} = 1 kΩ, C_{ext} = 0.01 μF	‡	1.5		‡		‡		μs

‡ See retriggering data in the *application information* section.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54AHC123A		SN74AHC123A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	$\overline{A}$ or B	Q or $\overline{Q}$	C_L = 15 pF		9.5*	20.6*	1*	24*	1	24	ns
t_{PHL}					10.2*	20.6*	1*	24*	1	24	
t_{PLH}	$\overline{CLR}$	Q or $\overline{Q}$	C_L = 15 pF		7.5*	15.8*	1*	18.5*	1	18.5	ns
t_{PHL}					9.3*	15.8*	1*	18.5*	1	18.5	
t_{PLH}	$\overline{CLR}$ trigger	Q or $\overline{Q}$	C_L = 15 pF		10*	22.4*	1*	26*	1	26	ns
t_{PHL}					10.6*	22.4*	1*	26*	1	26	
t_{PLH}	$\overline{A}$ or B	Q or $\overline{Q}$	C_L = 50 pF		10.5	24.1	1	27.5	1	27.5	ns
t_{PHL}					11.8	24.1	1	27.5	1	27.5	
t_{PLH}	$\overline{CLR}$	Q or $\overline{Q}$	C_L = 50 pF		8.9	19.3	1	22	1	22	ns
t_{PHL}					10.5	19.3	1	22	1	22	
t_{PLH}	$\overline{CLR}$ trigger	Q or $\overline{Q}$	C_L = 50 pF		11	25.9	1	29.5	1	29.5	ns
t_{PHL}					12.3	25.9	1	29.5	1	29.5	
t_w†		Q or $\overline{Q}$	C_L = 50 pF, C_{ext} = 28 pF, R_{ext} = 2 kΩ		182	240		300		300	ns
			C_L = 50 pF, C_{ext} = 0.01 μF, R_{ext} = 10 kΩ	90	100	110	90	110	90	110	μs
			C_L = 50 pF, C_{ext} = 0.1 μF, R_{ext} = 10 kΩ	0.9	1	1.1	0.9	1.1	0.9	1.1	ms
Δt_w‡					±1						%

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† t_w = Pulse duration at Q and $\overline{Q}$ outputs
‡ Δt_w = Output pulse-duration variation (Q and $\overline{Q}$) between circuits in same package

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

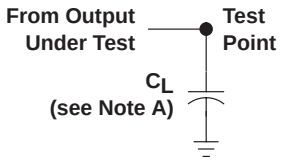
PARAMETER	FROM (NPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54AHC123A		SN74AHC123A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	$\overline{A}$ or B	Q or $\overline{Q}$	C_L = 15 pF		6.5*	12*	1*	14*	1	14	ns
t_{PHL}					7.1*	12*	1*	14*	1	14	
t_{PLH}	$\overline{CLR}$	Q or $\overline{Q}$	C_L = 15 pF		5.3*	9.4*	1*	11*	1	11	ns
t_{PHL}					6.5*	9.4*	1*	11*	1	11	
t_{PLH}	$\overline{CLR}$ trigger	Q or $\overline{Q}$	C_L = 15 pF		6.9*	12.9*	1*	15*	1	15	ns
t_{PHL}					7.4*	12.9*	1*	15*	1	15	
t_{PLH}	$\overline{A}$ or B	Q or $\overline{Q}$	C_L = 50 pF		7.3	14	1	16	1	16	ns
t_{PHL}					8.3	14	1	16	1	16	
t_{PLH}	$\overline{CLR}$	Q or $\overline{Q}$	C_L = 50 pF		6.3	11.4	1	13	1	13	ns
t_{PHL}					7.4	11.4	1	13	1	13	
t_{PLH}	$\overline{CLR}$ trigger	Q or $\overline{Q}$	C_L = 50 pF		7.6	14.9	1	17	1	17	ns
t_{PHL}					8.7	14.9	1	17	1	17	
t_w†		Q or $\overline{Q}$	C_L = 50 pF, C_{ext} = 28 pF, R_{ext} = 2 kΩ		167	200		240		240	ns
			C_L = 50 pF, C_{ext} = 0.01 μF, R_{ext} = 10 kΩ	90	100	110	90	110	90	110	μs
			C_L = 50 pF, C_{ext} = 0.1 μF, R_{ext} = 10 kΩ	0.9	1	1.1	0.9	1.1	0.9	1.1	ms
Δt_w‡					±1						%

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† t_w = Pulse duration at Q and $\overline{Q}$ outputs
‡ Δt_w = Output pulse-duration variation (Q and $\overline{Q}$) between circuits in same package

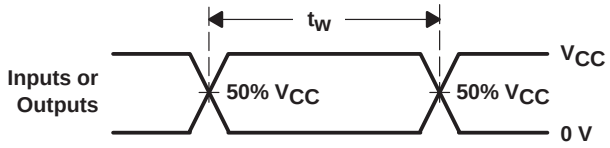
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	29	pF

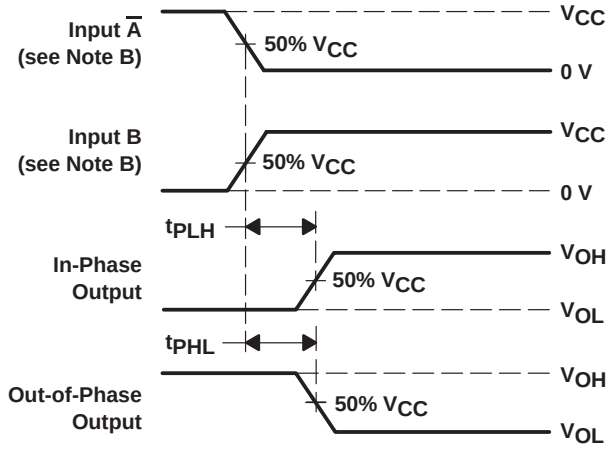
PARAMETER MEASUREMENT INFORMATION



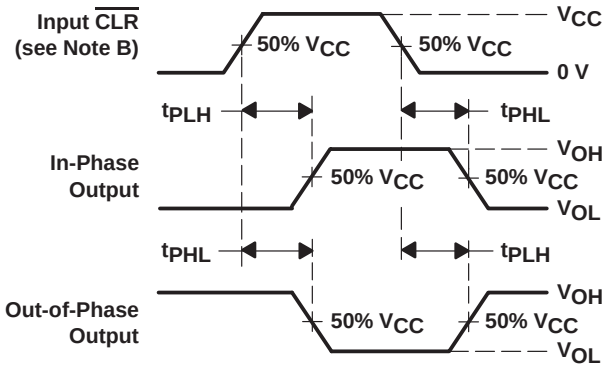
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
DELAY TIMES



VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

caution in use

To prevent malfunctions due to noise, connect a high-frequency capacitor between V_{CC} and GND, and keep the wiring between the external components and C_{ext} and R_{ext}/C_{ext} terminals as short as possible.

power-down considerations

Large values of C_{ext} can cause problems when powering down the ’AHC123A devices because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor can discharge from V_{CC} through the protection diodes at pin 2 or pin 14. Current through the input protection diodes must be limited to 30 mA; therefore, the turn-off time of the V_{CC} power supply must not be faster than $t = V_{CC} \times C_{ext}/30$ mA. For example, if V_{CC} = 5 V and C_{ext} = 15 pF, the V_{CC} supply must turn off no faster than $t = (5\ V) \times (15\ pF)/30\ mA = 2.5$ ns. Usually, this is not a problem because power supplies are heavily filtered and cannot discharge at this rate. When a more rapid decrease of V_{CC} to zero occurs, the ’AHC123A devices can sustain damage. To avoid this possibility, use external clamping diodes.

output pulse duration

The output pulse duration, t_w, is determined primarily by the values of the external capacitance (C_T) and timing resistance (R_T). The timing components are connected as shown in Figure 2.

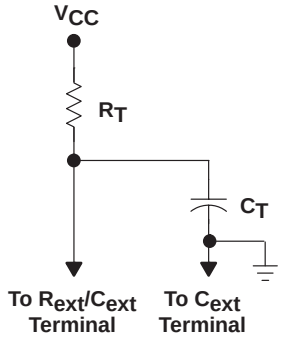


Figure 2. Timing-Component Connections

The pulse duration is given by:

$$t_w = K \times R_T \times C_T \qquad (1)$$

if C_T is ≥1000 pF, K = 1.0 or
if C_T is <1000 pF, K can be determined from Figure 9

where:

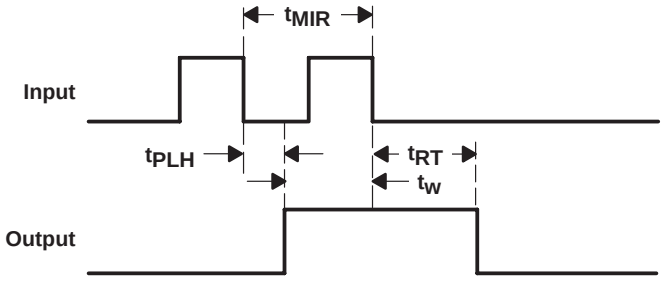
t_w = pulse duration in ns
R_T = external timing resistance in kΩ
C_T = external capacitance in pF
K = multiplier factor

Equation 1 and Figure 3 can be used to determine values for pulse duration, external resistance, and external capacitance.

APPLICATION INFORMATION

retriggering data

The minimum input retriggering time (t_{MIR}) is the minimum time required after the initial signal before retriggering the input. After t_{MIR}, the device retriggers the output. Experimentally, it also can be shown that to retrigger the output pulse, the two adjacent input signals should be t_{MIR} apart, where $t_{MIR} = 0.30 \times t_W$. The retrigger pulse duration is calculated as shown in Figure 3.



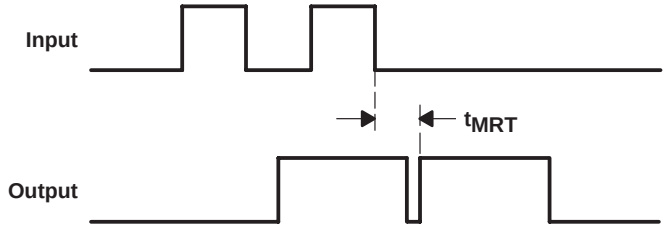
$t_{RT} = t_W + t_{PLH} = (K \times R_T \times C_T) + t_{PLH}$

Where:

t_{MIR} = Minimum Input Retriggering Time
t_{PLH} = Propagation Delay
t_{RT} = Retrigger Time
t_W = Output Pulse Duration Before Retriggering

Figure 3. Retrigger Pulse Duration

The minimum value from the end of the input pulse to the beginning of the retriggered output should be approximately 15 ns to ensure a retriggered output (see Figure 4).



t_{MRT} = Minimum Time Between the End of the Second Input Pulse and the Beginning of the Retriggered Output
t_{MRT} = 15 ns

Figure 4. Input/Output Requirements

APPLICATION INFORMATION†

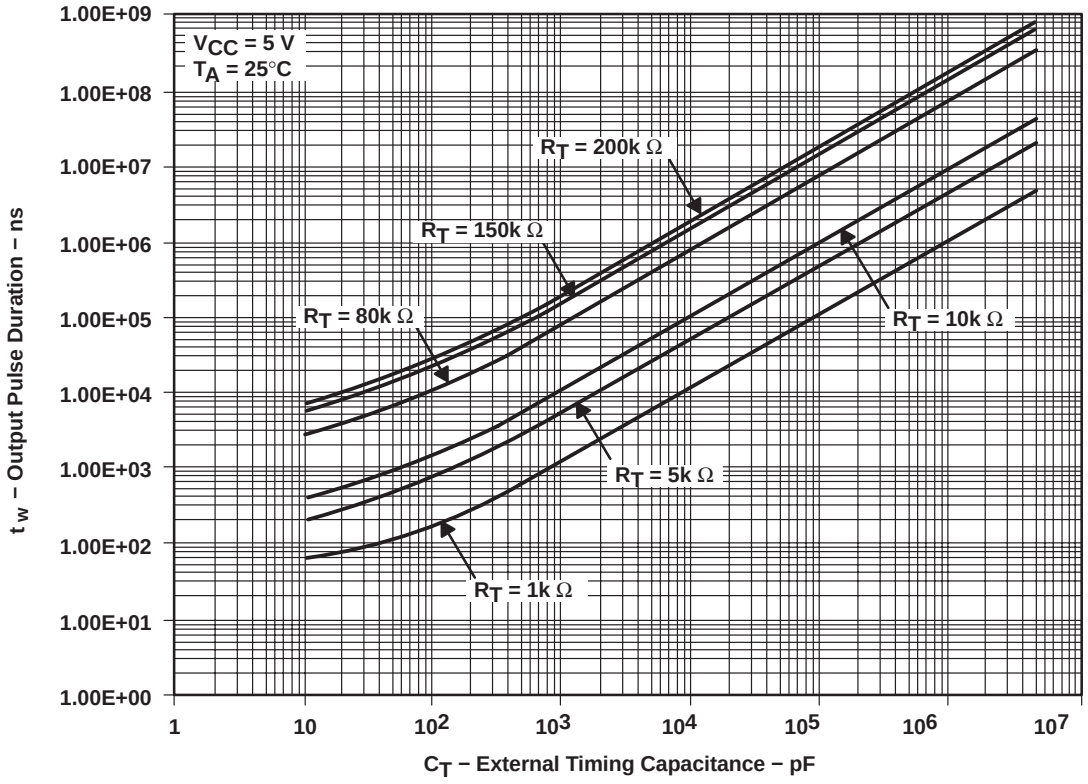


Figure 5. Output Pulse Duration vs External Timing Capacitance

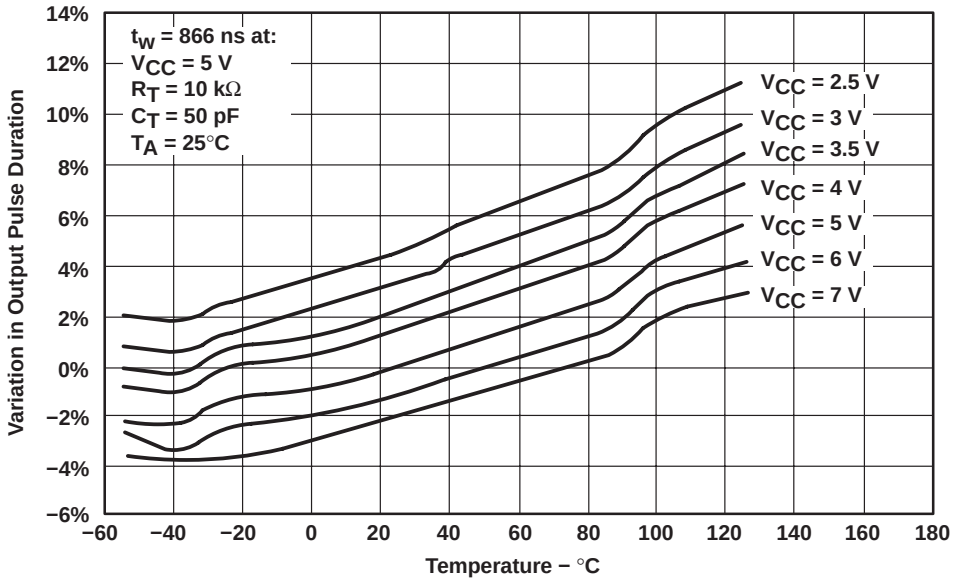


Figure 6. Variations in Output Pulse Duration vs Temperature

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

APPLICATION INFORMATION†

MINIMUM TRIGGER TIME vs V_{CC} CHARACTERISTICS

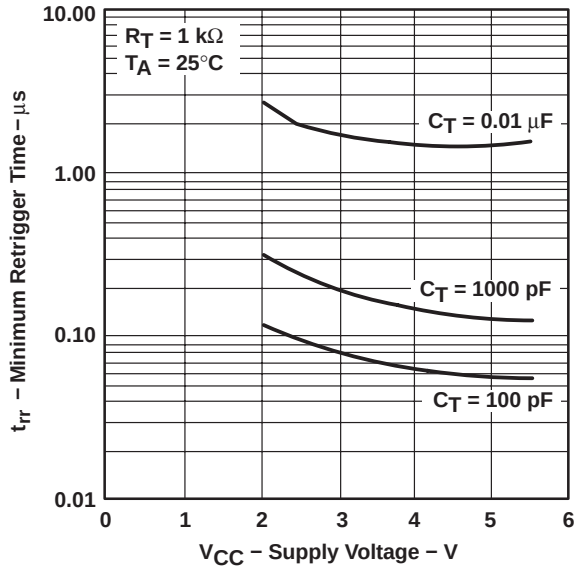


Figure 7

OUTPUT PULSE-DURATION CONSTANT vs SUPPLY VOLTAGE

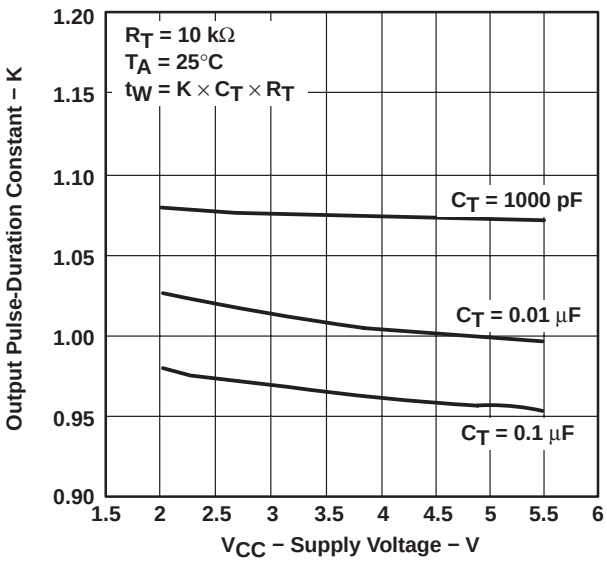


Figure 8

EXTERNAL CAPACITANCE vs MULTIPLIER FACTOR

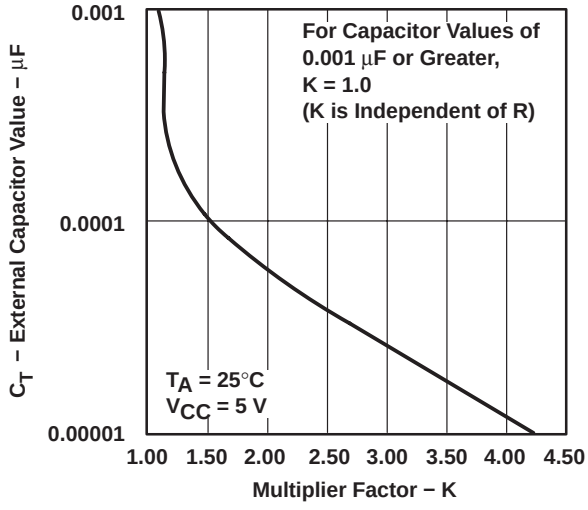


Figure 9

DISTRIBUTION OF UNITS vs OUTPUT PULSE DURATION

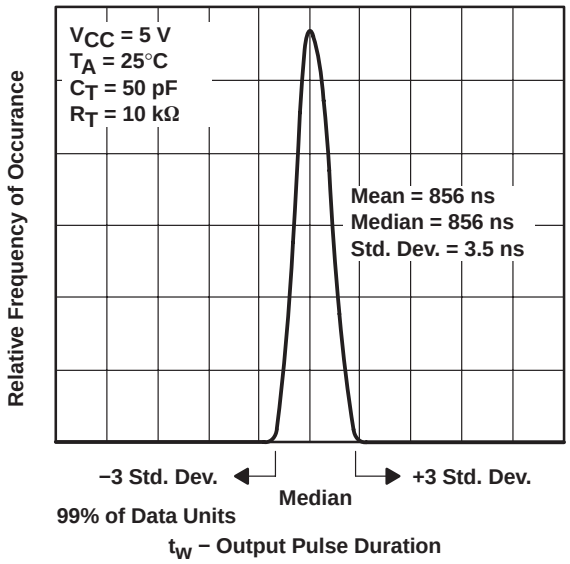


Figure 10

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9860801Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9860801Q2A SNJ54AHC 123AFK	Samples
5962-9860801QEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9860801QEA SNJ54AHC123AJ	Samples
5962-9860801QFA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9860801QFA SNJ54AHC123AW	Samples
SN74AHC123AD	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC123A	Samples
SN74AHC123ADBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA123A	Samples
SN74AHC123ADGVR	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA123A	Samples
SN74AHC123ADGVRE4	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA123A	Samples
SN74AHC123ADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC123A	Samples
SN74AHC123ADRE4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC123A	Samples
SN74AHC123AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHC123AN	Samples
SN74AHC123APWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HA123A	Samples
SN74AHC123APWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA123A	Samples
SNJ54AHC123AFK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9860801Q2A SNJ54AHC 123AFK	Samples
SNJ54AHC123AJ	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9860801QEA SNJ54AHC123AJ	Samples
SNJ54AHC123AW	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9860801QFA SNJ54AHC123AW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54AHC123A, SN74AHC123A :

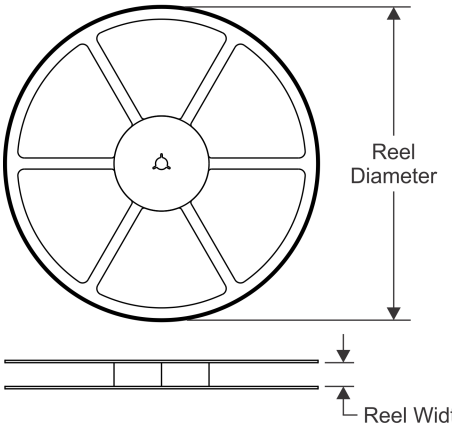
- Catalog : SN74AHC123A
- Enhanced Product : SN74AHC123A-EP, SN74AHC123A-EP
- Military : SN54AHC123A

NOTE: Qualified Version Definitions:

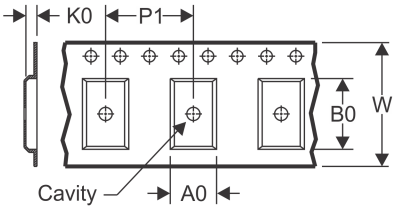
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

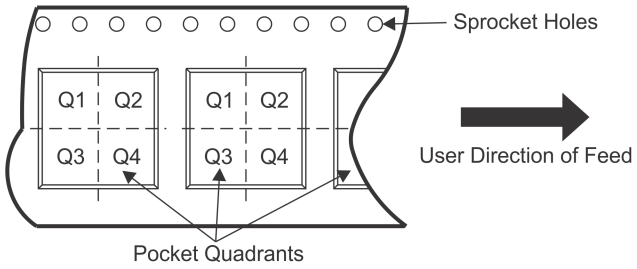


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

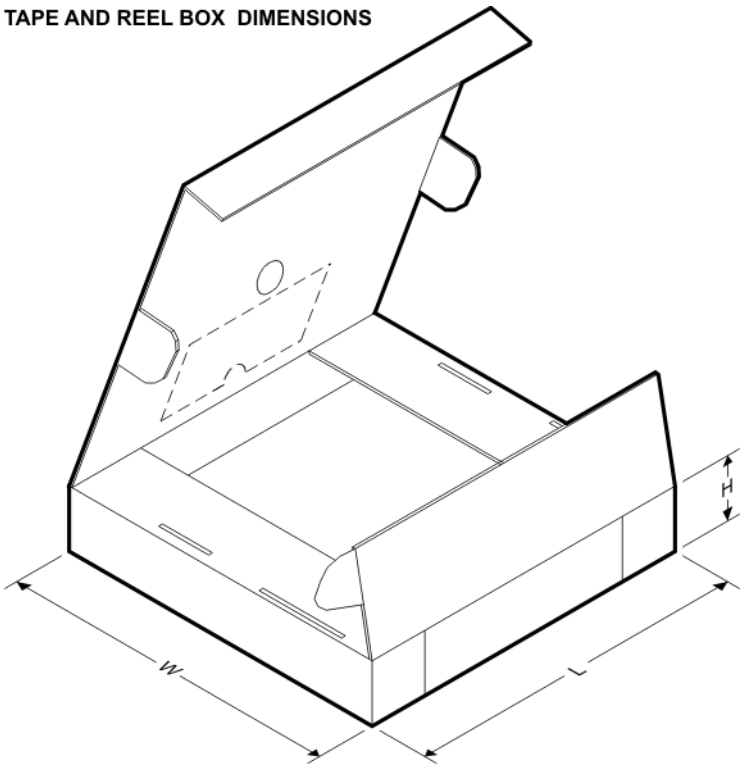
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC123ADBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC123ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC123ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHC123APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC123APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC123APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

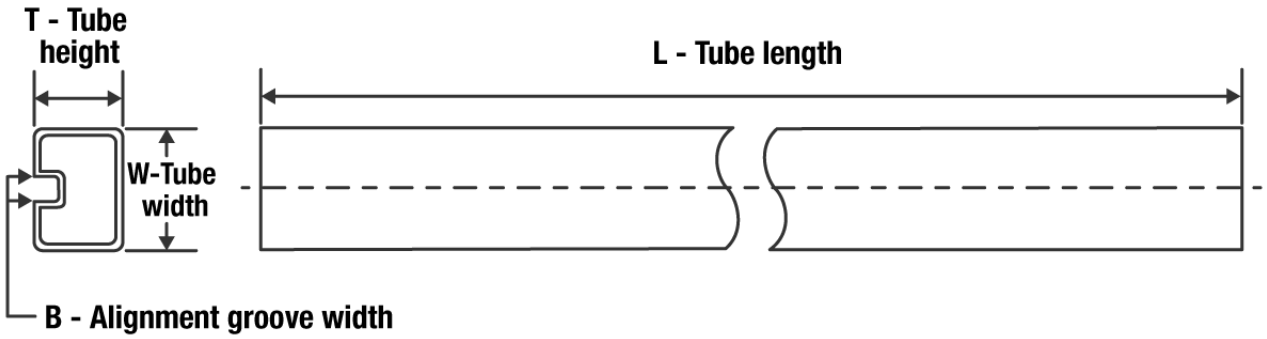
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC123ADBR	SSOP	DB	16	2000	853.0	449.0	35.0
SN74AHC123ADGVR	TVSOP	DGV	16	2000	853.0	449.0	35.0
SN74AHC123ADR	SOIC	D	16	2500	340.5	336.1	32.0
SN74AHC123APWR	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74AHC123APWR	TSSOP	PW	16	2000	853.0	449.0	35.0
SN74AHC123APWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0

TUBE

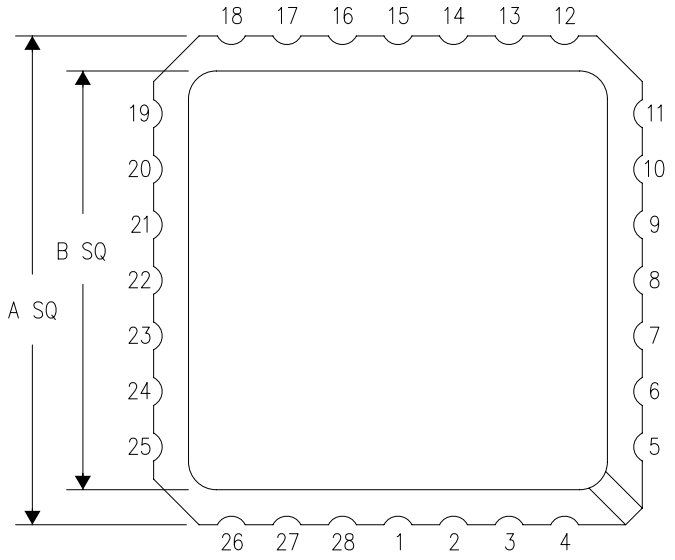


*All dimensions are nominal

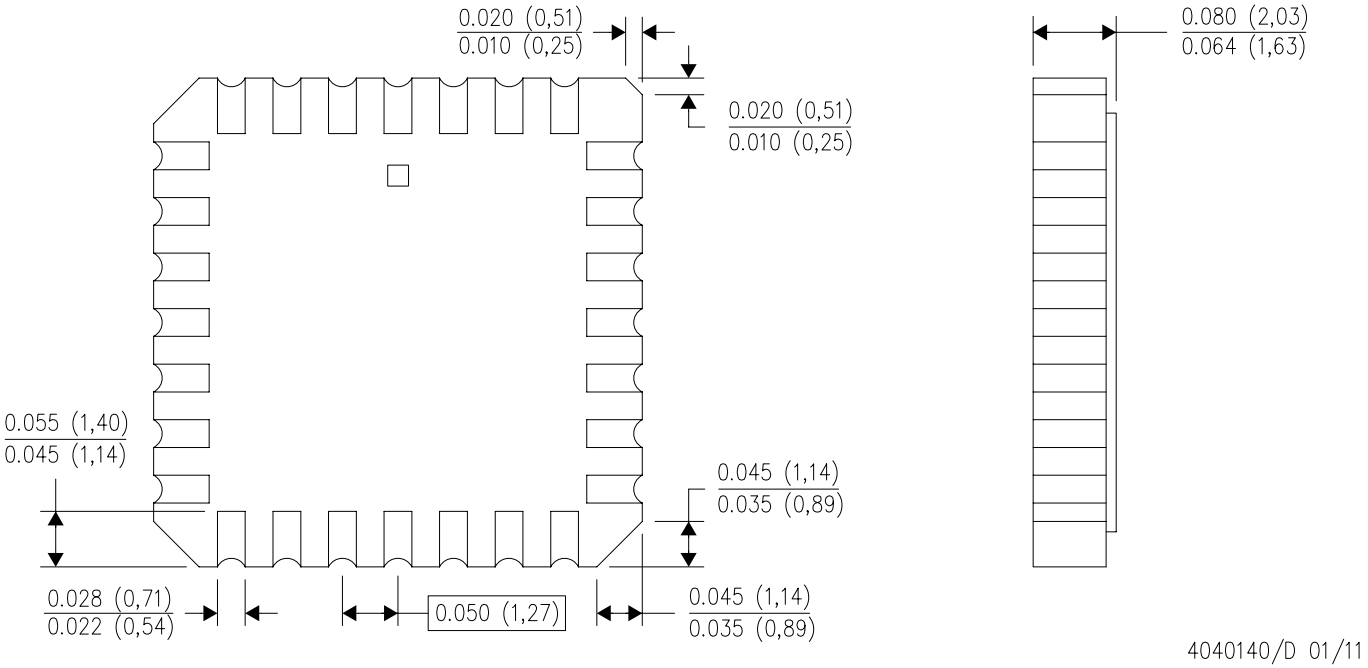
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9860801Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
SN74AHC123AD	D	SOIC	16	40	507	8	3940	4.32
SN74AHC123AN	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54AHC123AFK	FK	LCCC	20	1	506.98	12.06	2030	NA

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



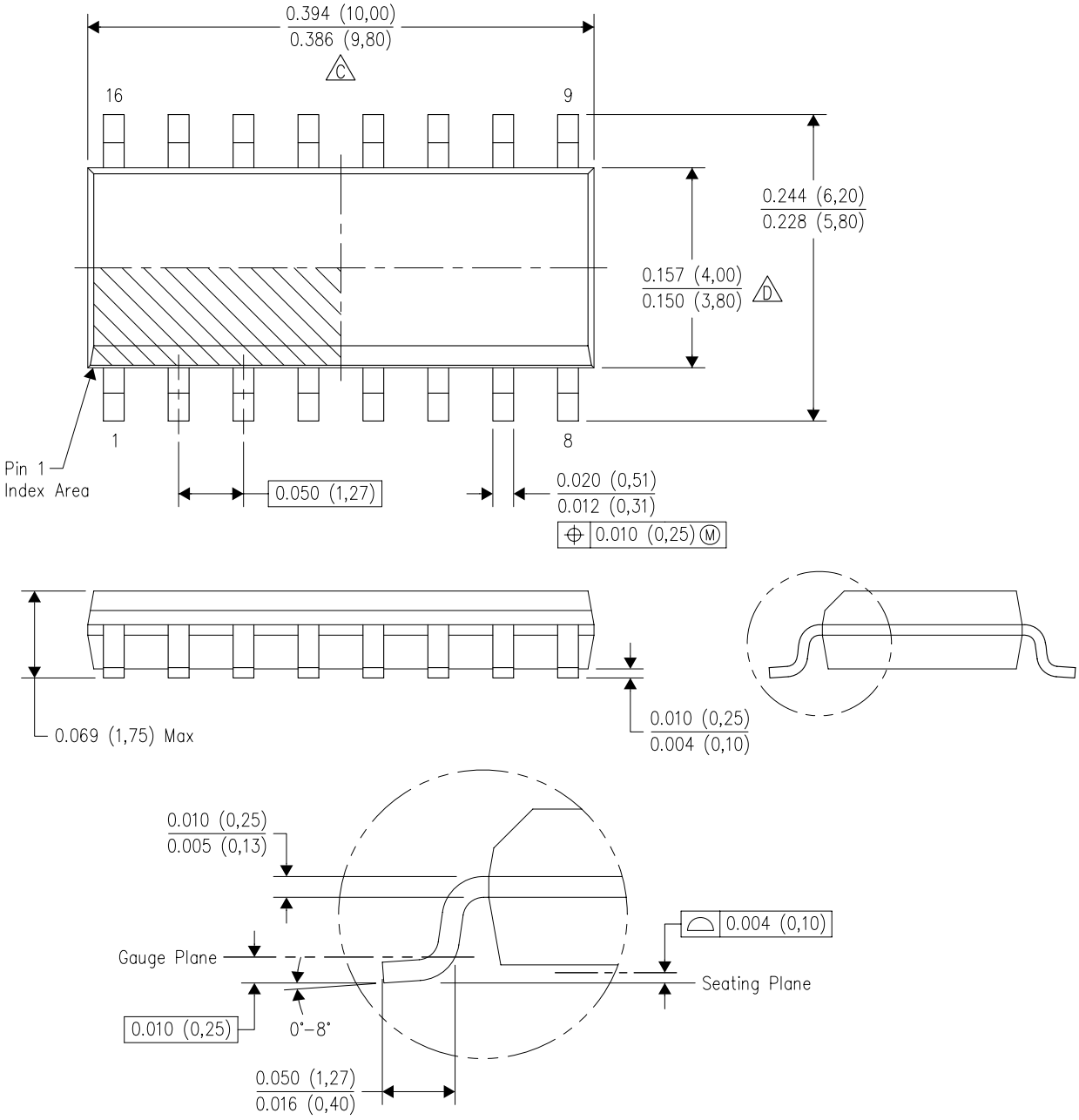
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

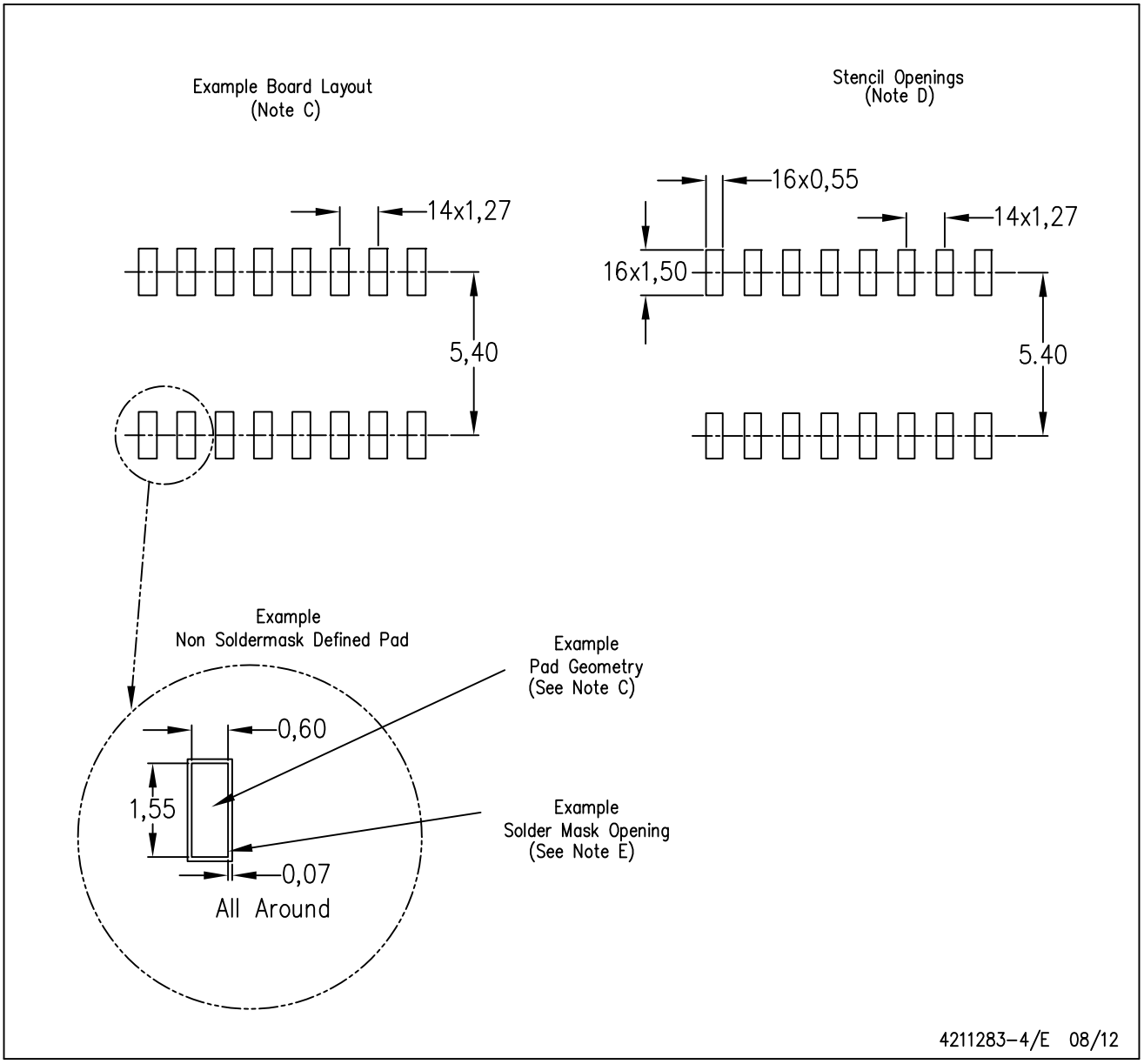
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



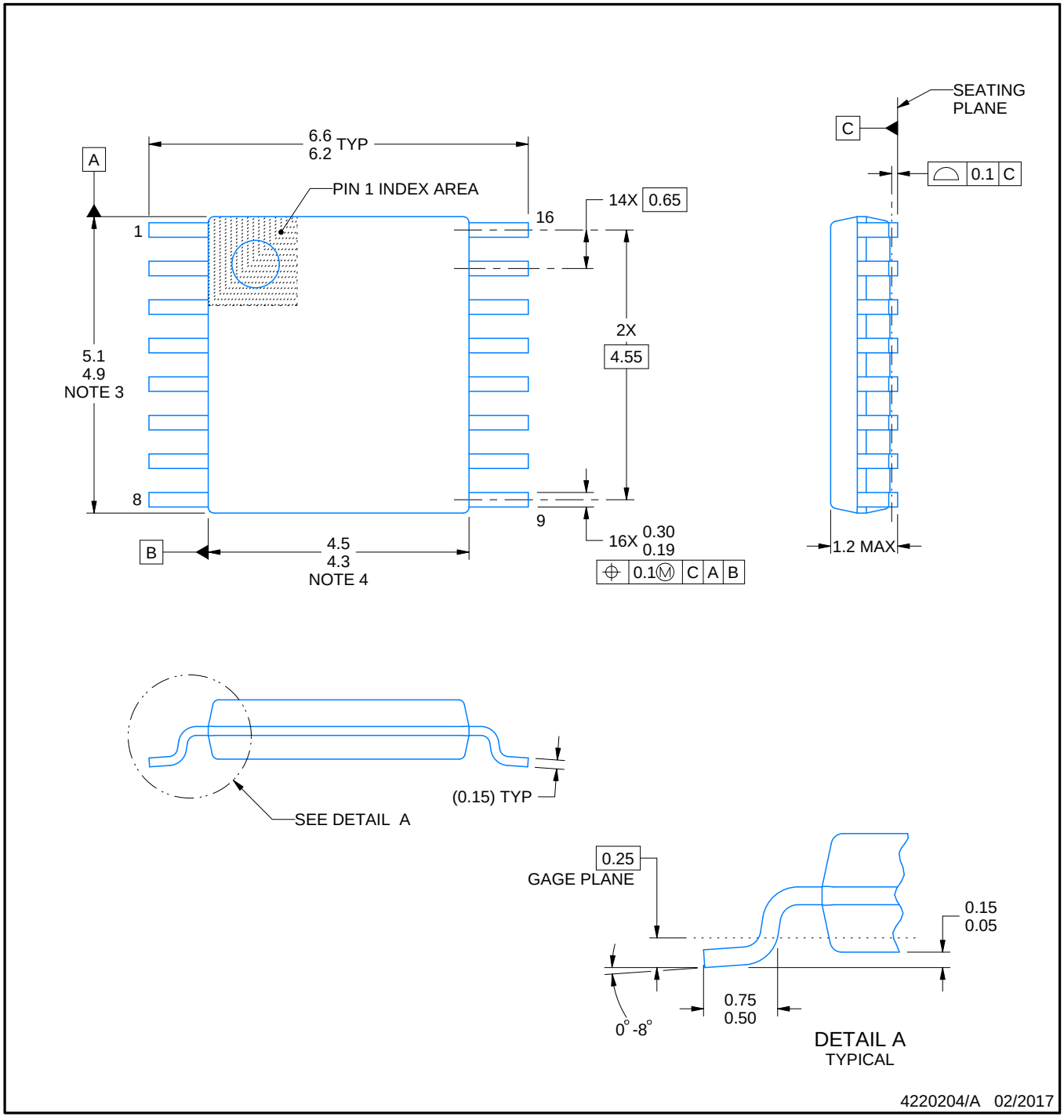
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

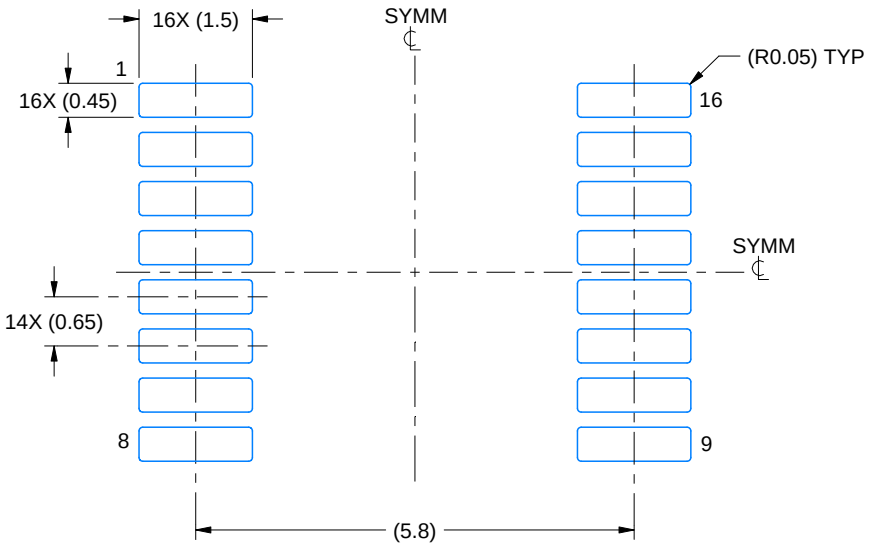
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

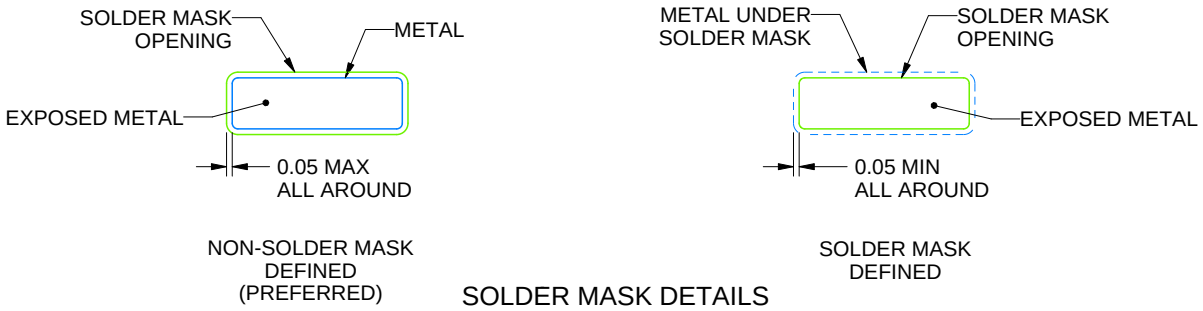


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

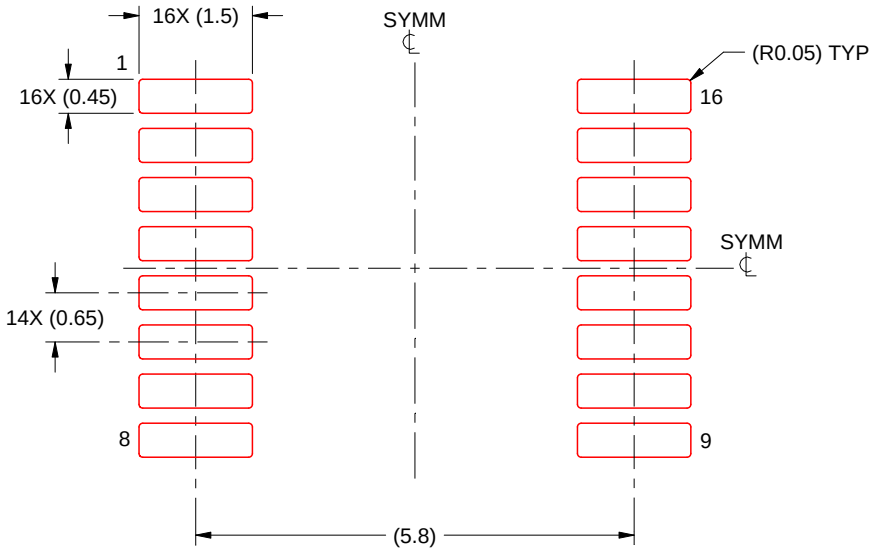


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

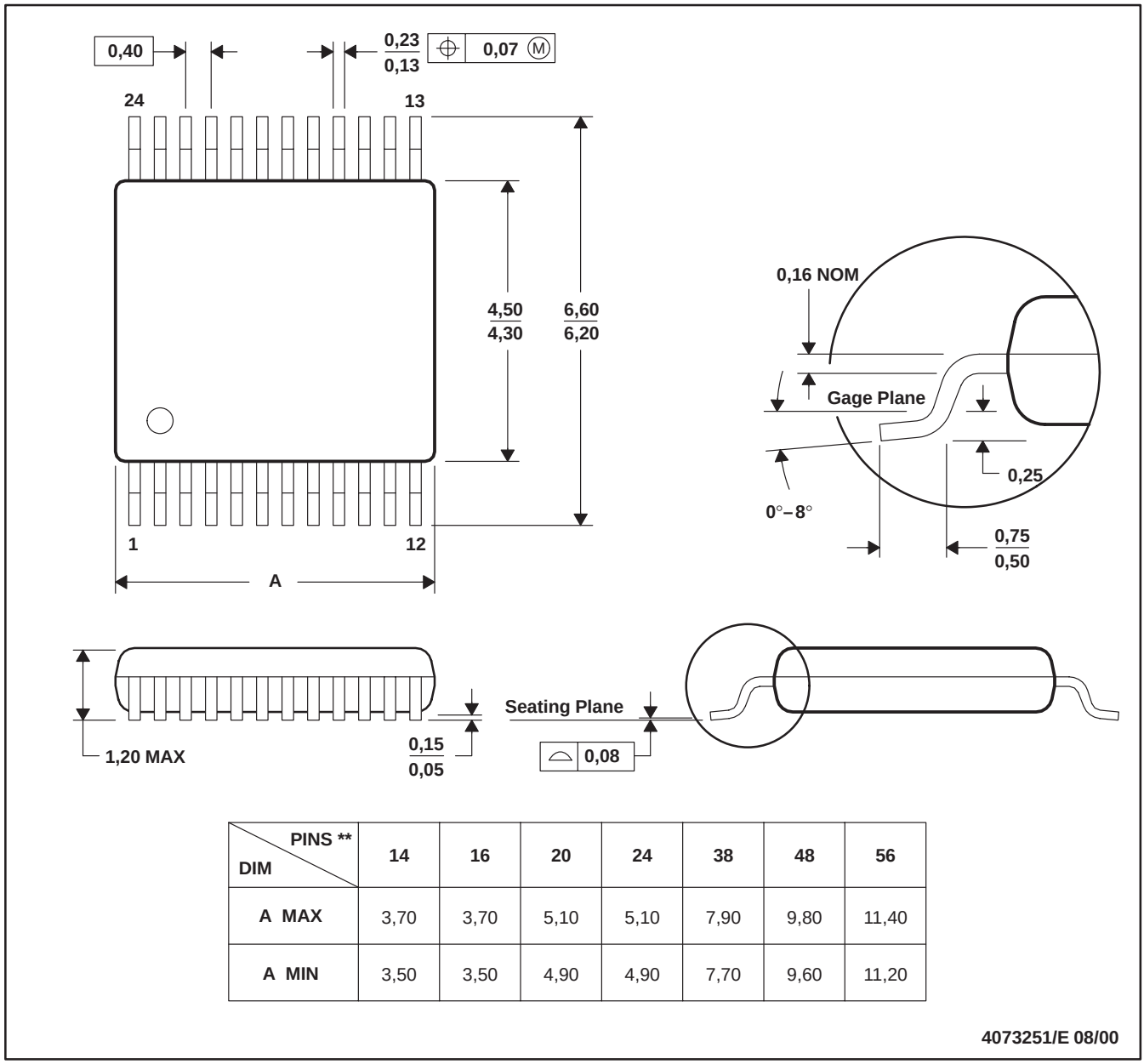
4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

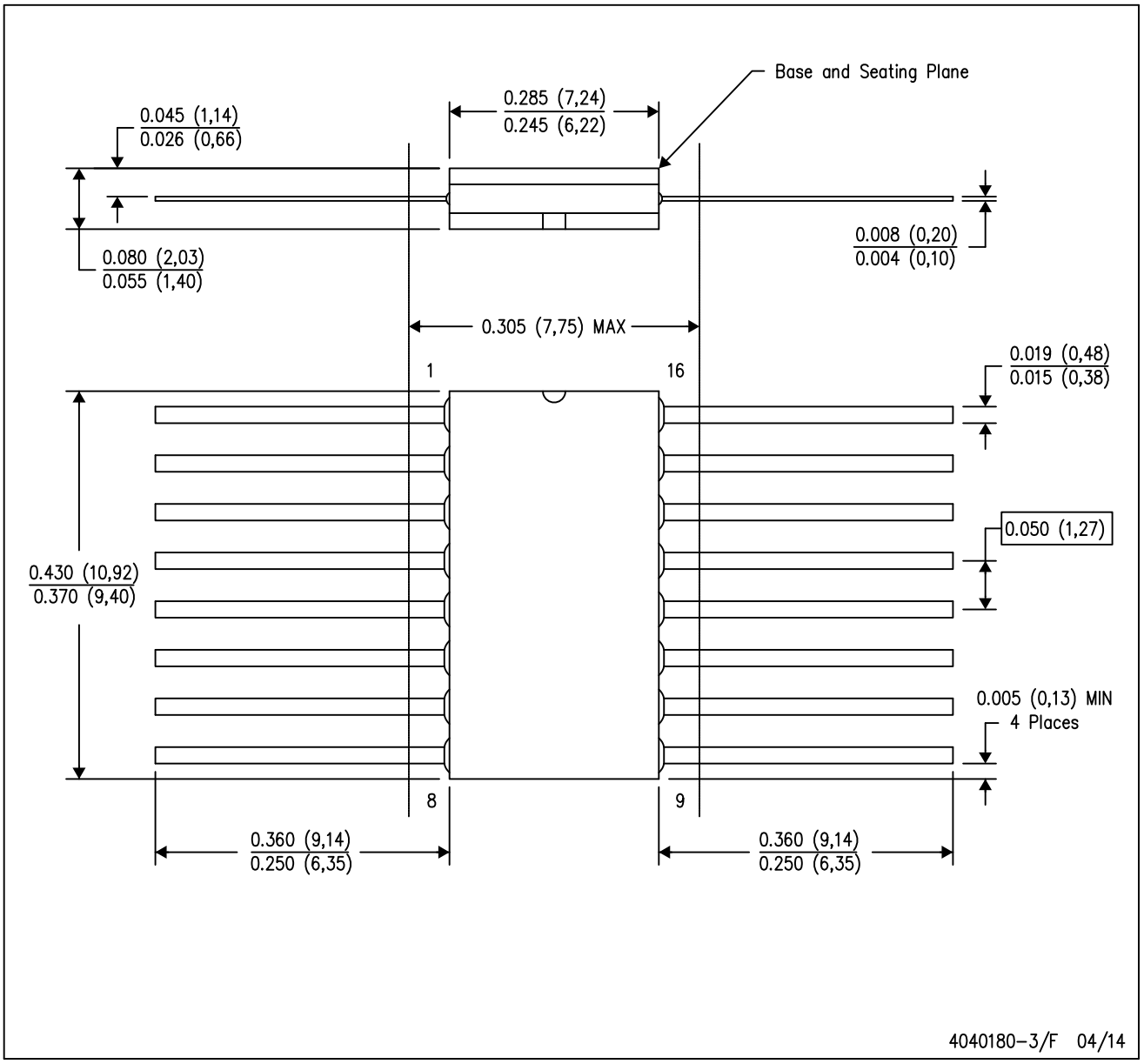


DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

W (R–GDFP–F16) CERAMIC DUAL FLATPACK

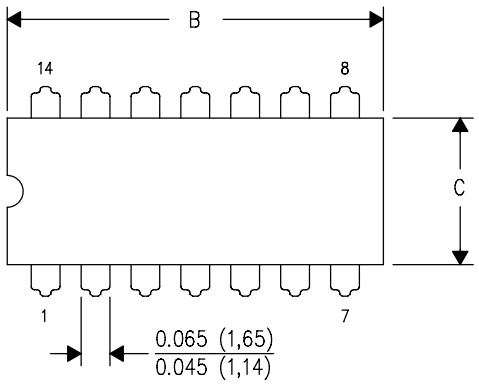


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

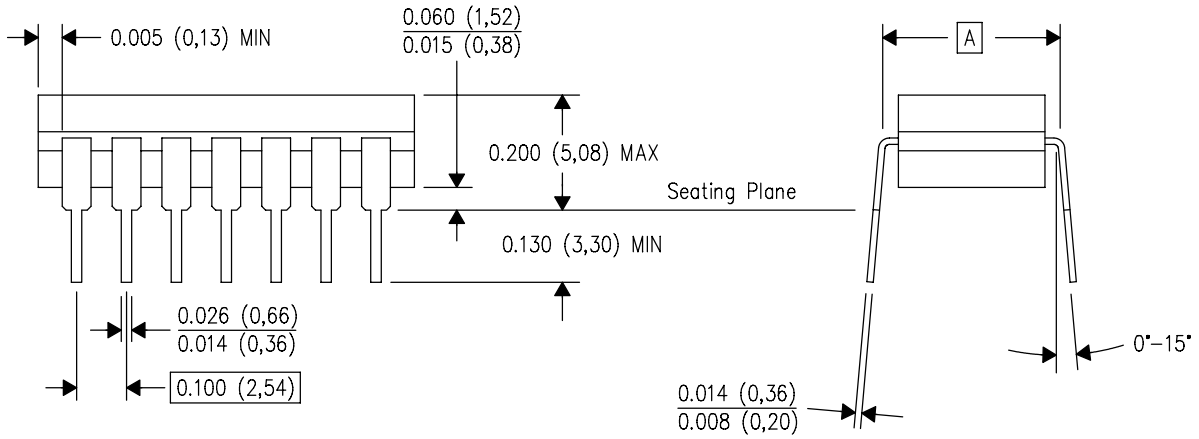
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



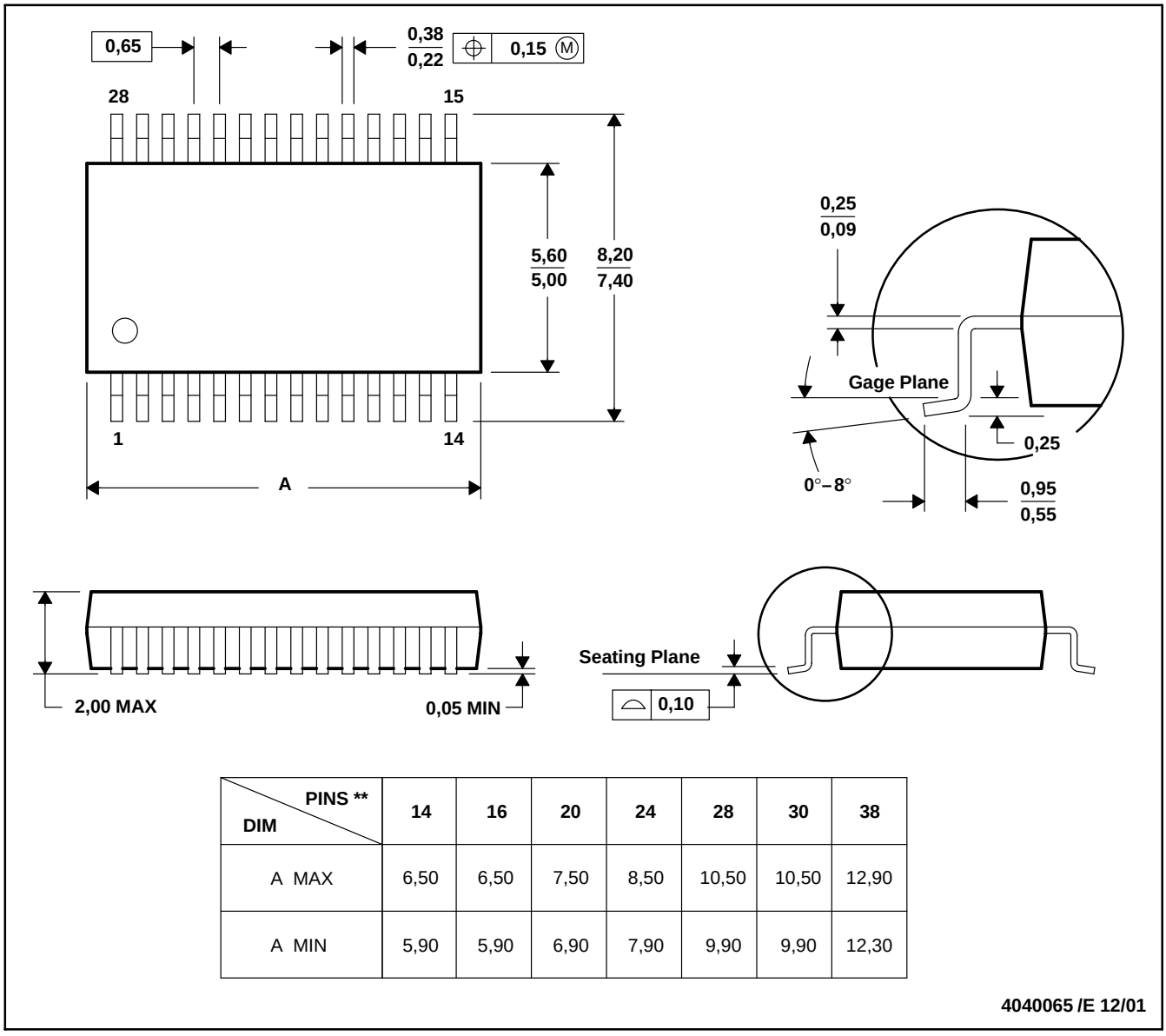
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

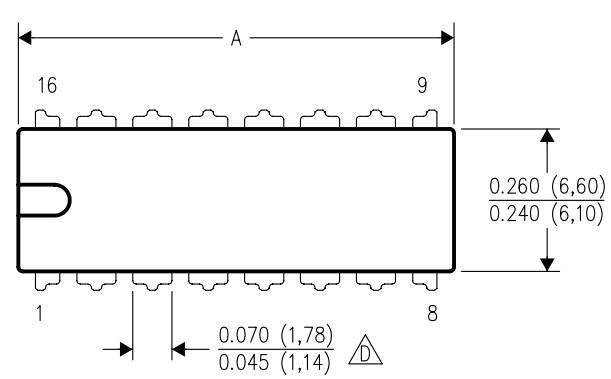
4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

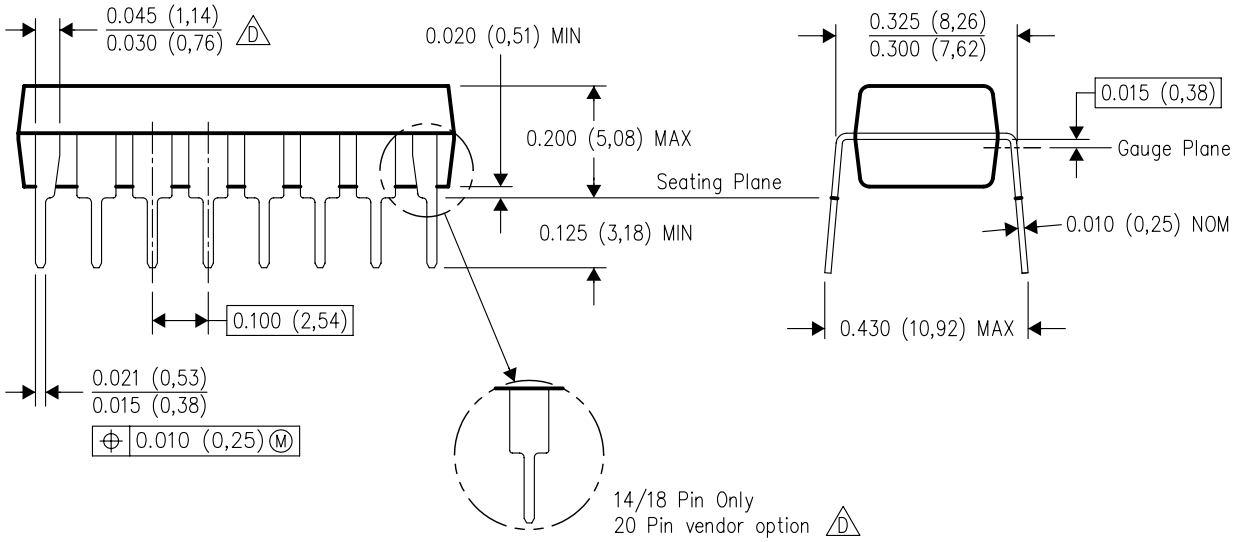
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265