LP5900 150-mA Ultra-Low-Noise LDO for RF and Analog Circuits - Requires No Bypass Capacitor

1 Features

- Input Voltage Range, 2.5 V to 5.5 V
- Output Voltage Range, 1.5 V to 4.5 V
- Stable with 0.47-µF Ceramic Input and Output Capacitors
- No Noise Bypass Capacitor Required
- Logic Controlled Enable
- Thermal-Overload and Short-Circuit Protection
- −40°C to 125°C Junction Temperature Range for Operation
- Output Current, 150 mA
- Low Output Voltage Noise, 6.5 μV_{RMS}
- PSRR, 75 dB at 1 kHz
- Output Voltage Tolerance, ±2%
- Virturally Zero I_Q (Disabled), < 1 µA
- Very Low I_Q (Enabled), 25 µA
- Start-up Time, 150 µs
- Low Dropout, 80 mV Typ.

2 Applications

- Cellular Phones
- PDA Handsets
- Wireless LAN Devices

3 Description

The LP5900 is an LDO capable of supplying 150-mA output current. Designed to meet the requirements of RF and analog circuits, the LP5900 device provides low noise, high PSRR, low quiescent current, and low line transient response figures. Using new innovative design techniques the LP5900 offers class-leading device noise performance without a noise bypass capacitor.

The device is designed to work with 0.47-µF input and output ceramic capacitors (no bypass capacitor required).

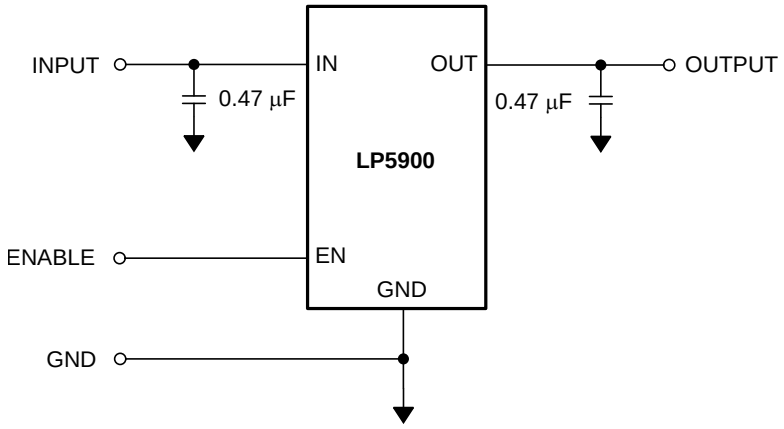
The device is available in a DSBGA (YZR) package and a WSON package; the device is also available in an extremely thin DSBGA (YPF) package. For all voltage and package options available today, see the Package Option Addendum (POA) at the end of this data sheet. For any other fixed output voltages from 1.5 V to 4.5 V in 25-mV steps and all other package options, contact your local TI Sales office.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
LP5900	DSBGA (4)	1.108 mm × 1.083 mm (MAX)
	WSON (6)	2.50 mm × 2.20 mm (NOM)

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision Q (February 2015) to Revision R — **Page**

- Changed "Linear Regulator" to "LDO" in title and first sentence of *Description* ... 1

Changes from Revision P (December 2014) to Revision Q — **Page**

- Added NC and Thermal Pad descriptions in *Pin Functions* ... 3
- Changed *Handling Ratings* to *ESD Ratings* table format; move storage temp spec to Ab Max; delete soldering info (in POA) ... 4
- Changed Unit for Line and Load regulation ... 5
- Changed I_I to I_{out} ... 7
- Changed I_I to I_{out} ... 8
- Changed I_I to I_{out} ... 9
- Added *WSON Mounting* subsection ... 16
- Added another related doc link ... 17

Changes from Revision O (April 2013) to Revision P — **Page**

- Added *Pin Configuration and Functions* section, *Handling Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section; updated pin names and thermal information ... 1

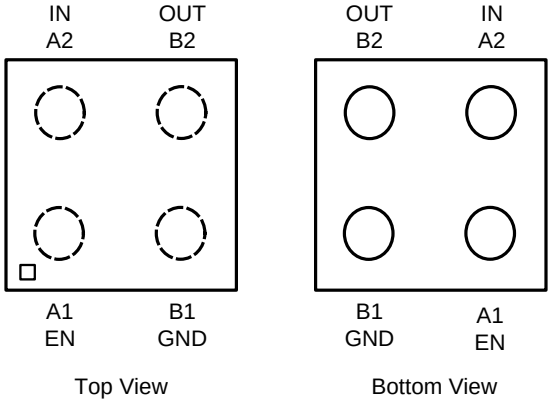
Changes from Revision N (April 2013) to Revision O — **Page**

- Changed layout of National Data Sheet to TI format ... 16

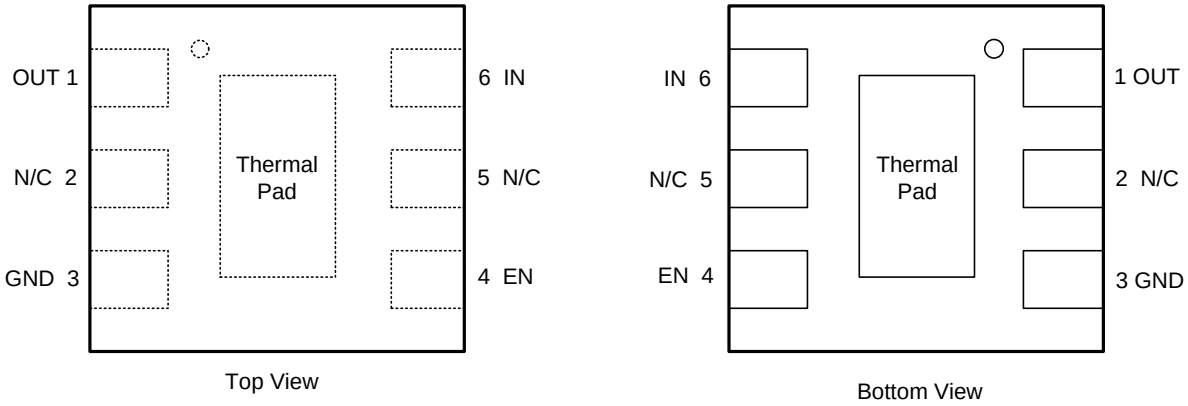
this is the ROD for SNVS358

5 Pin Configuration and Functions

YZR and YPF Packages
4-Pin DSBGA



NGF Package
6-Pin WSON with Exposed Thermal Pad



Pin Functions

PIN			TYPE	DESCRIPTION
DSBGA	WSON	NAME		
A1	4	EN	I	Enable input; disables the regulator when ≤ 0.4 V. Enables the regulator when ≥ 1.2 V. An internal 1-MΩ pull-down resistor connects this input to ground.
A2	6	IN	I	Input voltage supply. Connect a 0.47-µF capacitor at this input.
B1	3	GND	—	Common ground
B2	1	OUT	O	Output voltage. A 0.47-µF Low ESR capacitor should be connected to this pin. Connect this output to the load circuit.
—	2	NC	—	No internal connection.
—	Thermal Pad	Thermal Pad	—	The exposed thermal pad on the bottom of the packagemust be connected to a copper area on the PCB under the package. TI recommends use of thermal vias to remove heat from the package into the PCB. Connect the thermal pad to ground potential or leave floating. Do not connect the thermal pad to any potential other than the same ground potential seen at device pin 3. For additional information on using TI's non-pullback WSON package, see *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401).

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

	MIN	MAX	UNIT
Input voltage, V_{IN}	–0.3	6	V
Output voltage, V_{OUT}	–0.3	V_{IN} + 0.3	
Enable input voltage, V_{EN}	–0.3	V_{IN} + 0.3	
Continuous power dissipation(4)	Internally Limited		
Junction temperature, T_{JMAX}		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input voltage, V_{IN}	2.5	5.5	V
Enable voltage, V_{EN}	0	V_{IN} + 0.3	V
Output current, I_{OUT}(2)	0	150	mA
Junction temperature, T_J	–40	125	°C
Ambient temperature, T_A(2)	–40	85	°C

(1) All voltages are with respect to the potential at the GND pin.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})$. See *Application and Implementation*.

6.4 Thermal Information

THERMAL METRIC(1)		LP5900		UNIT
		NGF	YZR/YPF	
		6 PINS	4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	79.8	177.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	84.4	0.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.4	35.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.6	5.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20.3	35.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	11.2	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise noted, specifications apply in *Figure 16* with: $V_{IN} = V_{OUT\ (NOM)} + 1$ V, $V_{EN} = 1.2$ V, $C_{IN} = C_{OUT} = 0.47$ µF, $I_{OUT} = 1$ mA.[1][2]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage			2.5		5.5	V
ΔV_{OUT}	Output voltage tolerance	$V_{IN} = (V_{OUT(NOM)} + 1$ V) to 5.5 V, $I_{OUT} = 1$ mA to 150 mA, $-40°C \le T_J \le 125°C$		−2%		2%	
	Line regulation	$V_{IN} = (V_{OUT(NOM)} + 1$ V) to 5.5 V, $I_{OUT} = 1$ mA			0.05		%V
	Load regulation	$I_{OUT} = 1$ mA to 150 mA			0.001		%mA
I_{LOAD}	Load current	See[3]					mA
	Maximum output current	$-40°C \le T_J \le 125°C$				150	
I_Q	Quiescent current[4]	$V_{EN} = 1.2$ V, $I_{OUT} = 0$ mA			25		µA
		$V_{EN} = 1.2$ V, $I_{OUT} = 0$ mA, $-40°C \le T_J \le 125°C$				50	
		$V_{EN} = 1.2$ V, $I_{OUT} = 150$ mA			160		
		$V_{EN} = 1.2$ V, $I_{OUT} = 150$ mA, $-40°C \le T_J \le 125°C$				230	
		$V_{EN} = 0.3$ V (disabled)			0.003		
		$V_{EN} = 0.3$ V (disabled, $-40°C \le T_J \le 125°C$				1	
I_G	Ground current[5]	$I_{OUT} = 0$ mA ($V_{OUT} = 2.5$ V)			30		µA
V_{DO}	Dropout voltage[6]	$I_{OUT} = 150$ mA			80		mV
		$I_{OUT} = 150$ mA, $-40°C \le T_J \le 125°C$				150	
I_{SC}	Short-circuit current limit[7]				300		mA
PSRR	Power supply rejection ratio[8]	f = 100 Hz, $I_{OUT} = 150$ mA			85		dB
		f = 1 kHz, $I_{OUT} = 150$ mA			75		
		f = 10 kHz, $I_{OUT} = 150$ mA			65		
		f = 50 kHz, $I_{OUT} = 150$ mA			52		
		f = 100 kHz, $I_{OUT} = 150$ mA			40		
e_n	Output noise voltage[8]	BW = 10 Hz to 100 kHz, $V_{IN} = 4.2$ V	$I_{OUT} = 0$ mA		7		μV_{RMS}
			$I_{OUT} = 1$ mA		10		
			$I_{OUT} = 150$ mA		6.5		
$T_{SHUTDOWN}$	Thermal shutdown	Temperature			160		°C
		Hysteresis			20		
LOGIN INPUT THRESHOLDS							
V_{IL}	Low input threshold (V_{EN})	$V_{IN} = 2.5$ V to 5.5 V, $-40°C \le T_J \le 125°C$				0.4	V
V_{IH}	High input threshold (V_{EN})	$V_{IN} = 2.5$ V to 5.5 V, $-40°C \le T_J \le 125°C$		1.2			V
I_{EN}	Input current at EN pin[9]	$V_{EN} = 5.5$ V and $V_{IN} = 5.5$ V			5.5		µA
		$V_{EN} = 0$ V and $V_{IN} = 5.5$ V			0.001		

(1) All voltages are with respect to the potential at the GND pin.
(2) Minimum and Maximum limits are specified by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.
(3) The device maintains a stable, regulated output voltage without a load current.
(4) Quiescent current is defined here as the difference in current between the input voltage source and the load at the OUT pin.
(5) Ground current is defined here as the total current flowing to ground as a result of all input voltages applied to the device.
(6) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value. This parameter only applies to output voltages above 2.5 V.
(7) Short-circuit current is measured with OUT pulled to 0 V and IN worst case = 6 V.
(8) This specification is specified by design.
(9) There is a 1-MΩ resistor between EN pin and ground on the device.

Electrical Characteristics (continued)

Unless otherwise noted, specifications apply in *Figure 16* with: V_{IN} = $V_{OUT\ (NOM)}$ + 1 V, V_{EN} = 1.2 V, C_{IN} = C_{OUT} = 0.47 µF, I_{OUT} = 1 mA.[1][2]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TRANSIENT CHARACTERISTICS						
ΔV_{OUT}	Line transient[8]	V_{IN} = ($V_{OUT(NOM)}$) + 1 V) to ($V_{OUT(NOM)}$) + 1.6 V) in 30 µs, I_{OUT} = 1 mA, –40°C ≤ T_J ≤ 125°C	−2			mV
		V_{IN} = ($V_{OUT(NOM)}$) + 1.6 V) to ($V_{OUT(NOM)}$) + 1 V) in 30 µs, I_{OUT} = 1 mA, –40°C ≤ T_J ≤ 125°C			2	
	Load transient[8]	I_{OUT} = 1 mA to 150 mA in 10 µs, –40°C ≤ T_J ≤ 125°C	−110			mV
		I_{OUT} = 150 mA to 1 mA in 10 µs, –40°C ≤ T_J ≤ 125°C			50	
	Overshoot on start-up[8]	–40°C ≤ T_J ≤ 125°C			20	mV
	Turnon time	To 95% of $V_{OUT(NOM)}$		150	300	µs

6.6 Output and Input Capacitor, Recommended Specifications[1]

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
C_{IN}	Input capacitance	Capacitance for stability		0.47		µF
		Capacitance for stability, –40°C ≤ T_J ≤ 125°C	0.33			
C_{OUT}	Output capacitance	Capacitance for stability		0.47		
		Capacitance for stability, –40°C ≤ T_J ≤ 125°C	0.33		10	
ESR	Output/Input capacitance		5		500	mΩ

(1) The minimum capacitance must be greater than 0.33 µF over the full range of operating conditions. The capacitor tolerance must be 30% or better over the full temperature range. The full range of operating conditions for the capacitor in the application should be considered during device selection to ensure this minimum capacitance specification is met. TI recommends X7R capacitors; however, capacitor types X5R, Y5V and Z5U may be used with consideration of the application and conditions.

6.7 Typical Characteristics

Unless otherwise specified, C_{IN} = C_{OUT} = 0.47 µF, V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA , T_A = 25°C.

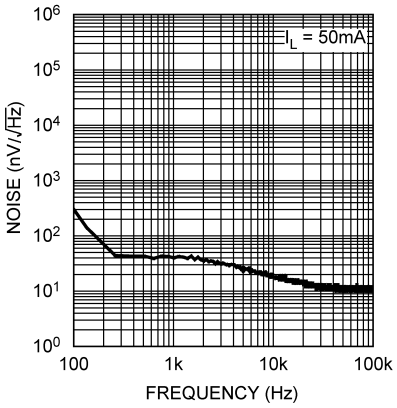


Figure 1. Output Noise Density

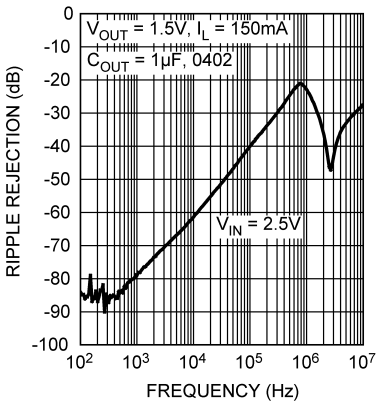


Figure 2. Power Supply Rejection Ratio

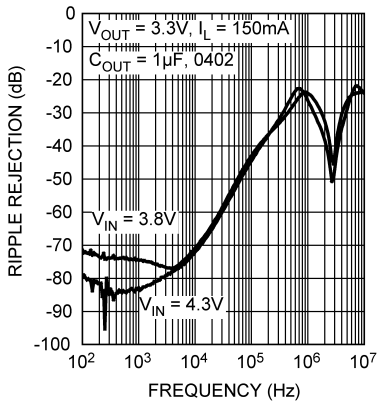


Figure 3. Power Supply Rejection Ratio

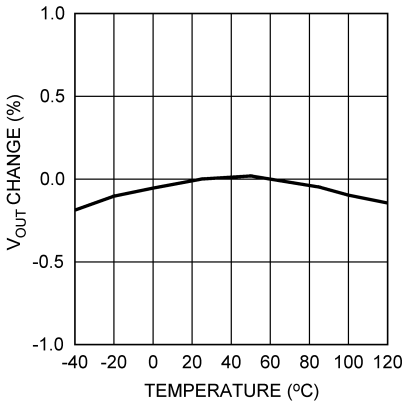


Figure 4. Output Voltage Change vs Temperature

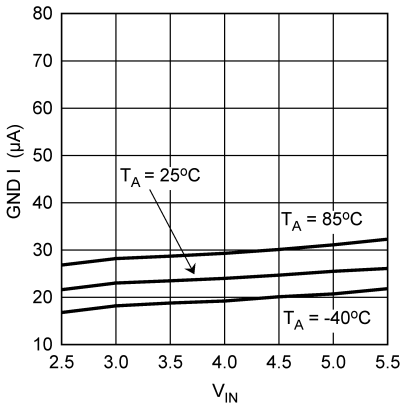


Figure 5. Ground Current vs V_{IN}, I_{LOAD} = 0 mA

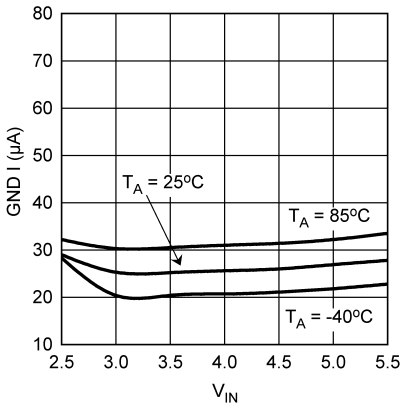


Figure 6. Ground Current vs V_{IN}, I_{LOAD} = 1 mA

Typical Characteristics (continued)

Unless otherwise specified, C_{IN} = C_{OUT} = 0.47 µF, V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA , T_A = 25°C.

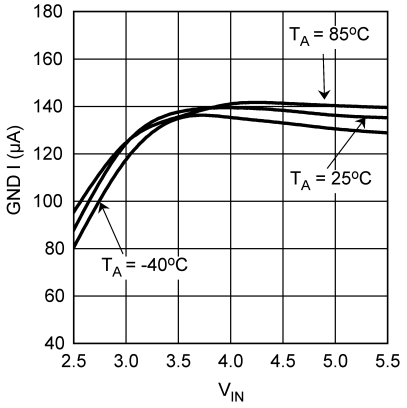


Figure 7. Ground Current vs V_{IN}, I_{LOAD} = 100 mA

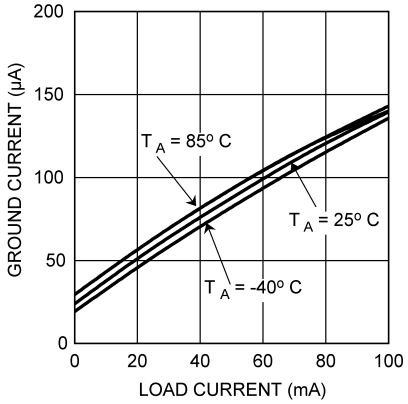


Figure 8. Ground Current vs Load Current

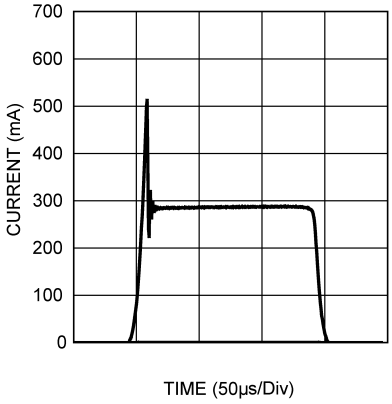


Figure 9. Short-Circuit Current

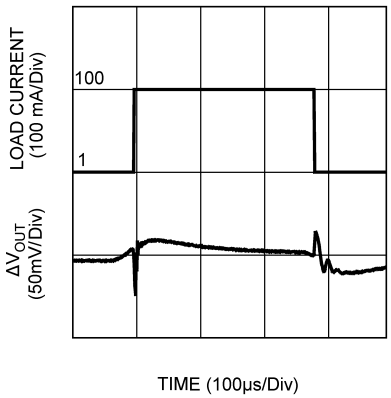


Figure 10. Load Transient

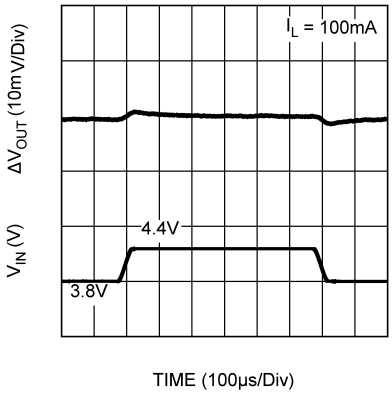


Figure 11. Line Transient

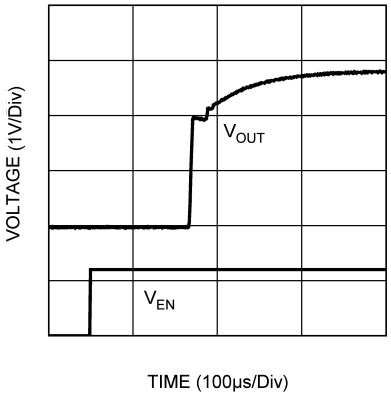


Figure 12. Enable Start-up Time, (I_{OUT}= 1 mA, V_{OUT} = 2.8 V)

Typical Characteristics (continued)

Unless otherwise specified, C_{IN} = C_{OUT} = 0.47 µF, V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA , T_A = 25°C.

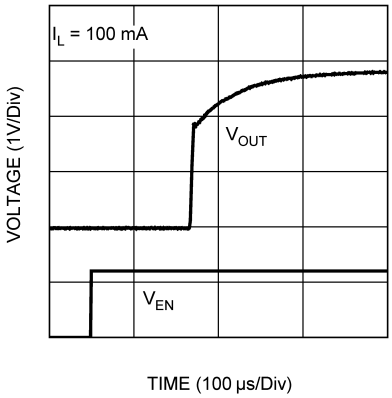


Figure 13. Enable Start-up Time, (I_{OUT}= 100 mA, V_{OUT} = 2.8 V)

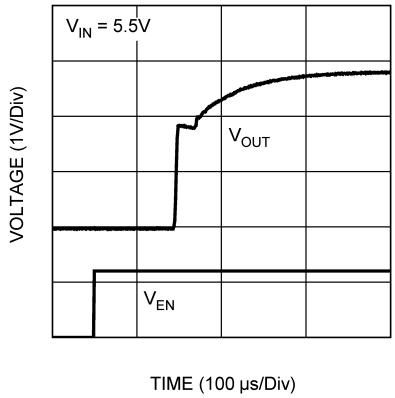


Figure 14. Enable Start-up Time, (I_{OUT}= 1 mA, V_{OUT} = 2.8 V)

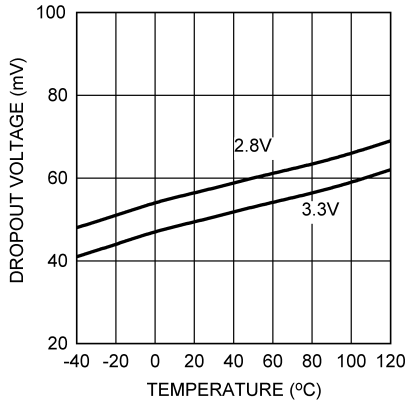


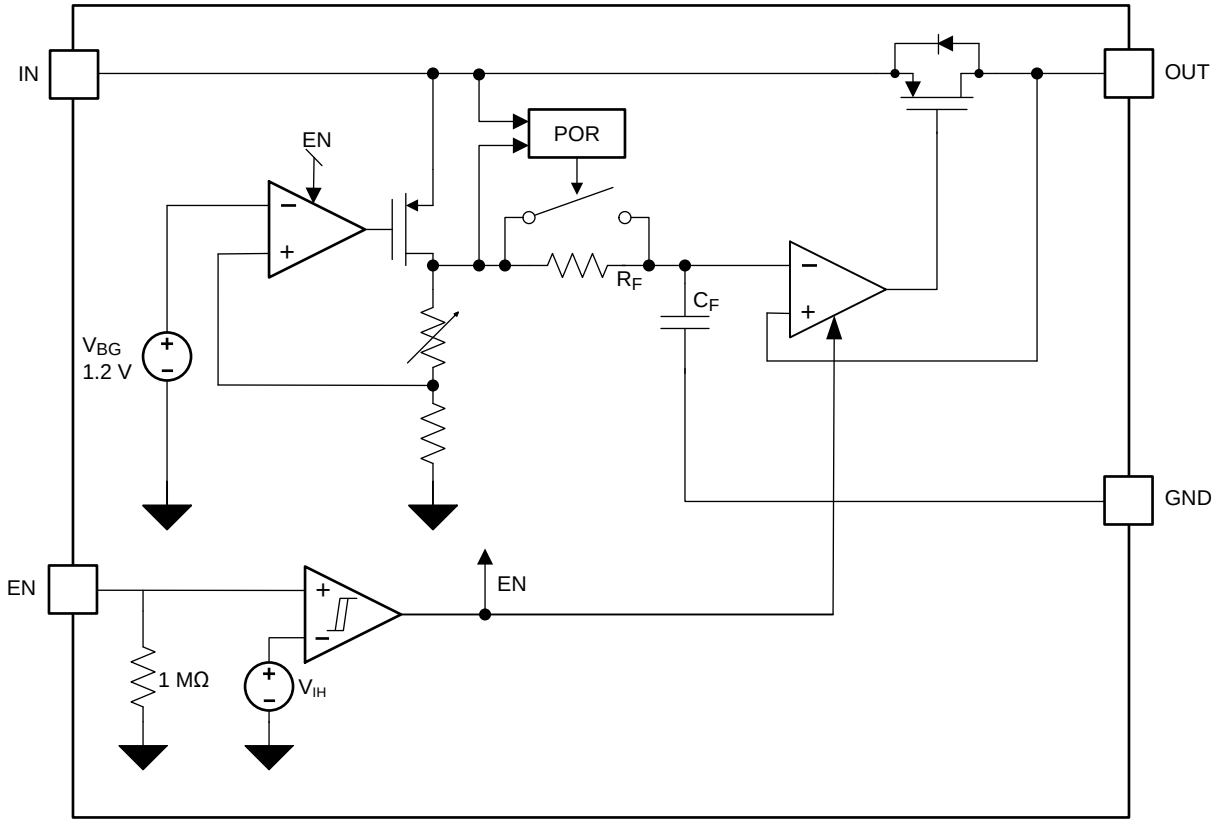
Figure 15. Dropout Over Temperature (100 mA)

7 Detailed Description

7.1 Overview

Designed to meet the needs of sensitive RF and analog circuits, the LP5900 provides low noise, high PSRR, and low quiescent current, as well as low line and load transient response figures. Using new innovative design techniques, the LP5900 offers class-leading noise performance without the need for a separate noise filter capacitor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 No-Load Stability

The LP5900 remains stable and in regulation with no external load.

7.3.2 Enable Control

The LP5900 enable (EN) pin is internally held low by a 1-MΩ resistor to GND. The EN must be higher than the V_{IH} threshold to ensure that the device is fully enabled under all operating conditions. The EN pin voltage must be lower than the V_{IL} threshold to ensure that the device is fully disabled.

7.3.3 Low Noise Output

Any internal noise at the LP5900 reference voltage is reduced by a first order low-pass RC filter before it is passed to the output buffer stage. This eliminates the need for the external bypass capacitor for noise suppression.

Feature Description (continued)

7.3.4 Thermal-Overload Protection

Thermal-overload protection disables the output when the junction temperature rises to approximately 160°C which allows the device to cool. When the junction temperature cools to approximately 140°C, the output is enabled. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

7.4 Device Functional Modes

7.4.1 Operation with Enable Control

The LP5900 may be switched ON or OFF by a logic input at the EN pin. A high voltage at this pin turns the device on. When the EN pin is low, the regulator output is off, and the device typically consumes 3 nA. However, if the application does not require the shutdown feature, the EN pin can be tied to IN pin to keep the regulator output permanently on. In this case the supply voltage must be fully established 500 µs or less to ensure correct operation of the start-up circuit. Failure to comply with this condition may cause a delayed start-up time of several seconds.

A 1 MΩ pull-down resistor ties the EN input to ground, and this ensures that the device will remain off when the EN pin is left open circuit. To ensure proper operation, the signal source used to drive the EN input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the *Electrical Characteristics* section under V_{IL} and V_{IH}.

7.4.2 Operation with Minimum Operating Input Voltage (V_{IN})

The LP5900 does not include any dedicated UVLO circuitry. The LP5900 internal circuitry is not fully functional until V_{IN} is at least 2.5 V. The output voltage is not regulated until $V_{IN} \geq (V_{OUT} + V_{DO})$.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP5900 is a linear regulator capable of supplying a 150-mA output current. Designed to meet the requirements of RF and nalog circuits, the device provides low noise, high PSRR, low quiescent current, and low line transient response figures. Using new innovative design techniques the LP5900 offers class-leading device noise performance and is designed to work with 0.47-µF input and output ceramic capacitors (no bypass capacitor is required).

8.2 Typical Application

Figure 16 shows the typical application circuit for the LP5900. Input and output capacitances may need to be increased above the 0.47-µF minimum for some applications.

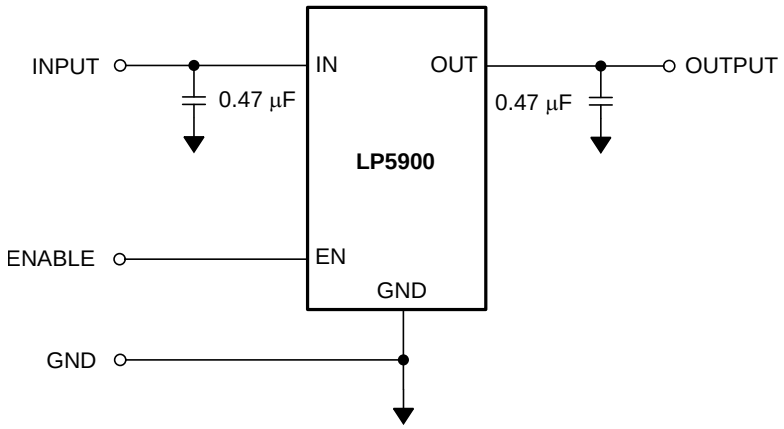


Figure 16. LP5900 Typical Application

8.2.1 Design Requirements

DESIGN PARAMETER	MIN	MAX	UNITS
Input voltage range	2.5	5.5	V
Output voltage		2.8	V
Output current		150	mA
Output capacitor range	0.47	10	µF
Input/Output capacitor ESR range	5	500	mΩ

8.2.2 Detailed Design Procedure

8.2.2.1 Power Dissipation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the device, to the ultimate heat sink, the ambient environment. Thus the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air. As stated in *Recommended Operating Conditions*, the allowable power dissipation for the device in a given package can be calculated using Equation 1:

$$P_D = \frac{(T_{JMAX} - T_A)}{R_{\theta JA}} \quad (1)$$

The actual power dissipation across the device can be represented by Equation 2:

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

This establishes the relationship between the power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

8.2.2.2 External Capacitors

Like any low-dropout regulator, the LP5900 requires external capacitors for regulator stability. The LP5900 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

8.2.2.2.1 Input Capacitor

An input capacitor is required for stability. The input capacitor should be at least equal to or greater than the output capacitor. It is recommended that a 0.47-µF capacitor be connected between the LP5900 IN pin and ground.

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: To ensure stable operation it is essential that good PCB practices are employed to minimize ground impedance and keep input inductance low. If these conditions cannot be met, or if long leads are to be used to connect the battery or other power source to the LP5900, then it is recommended to increase the input capacitor to at least 2.2 µF. Also, tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application. There are no requirements for the equivalent series resistance (ESR) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain 0.47 µF ±30% over the entire operating temperature range.

8.2.2.2.2 Output Capacitor

The LP5900 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (dielectric types X5R or X7R) in the 0.47 µF to 10 µF range, and with ESR between 5 mΩ to 500 mΩ, is suitable in the LP5900 application circuit. For this device the output capacitor should be connected between the OUT pin and a good ground connection and should be mounted within 1 cm of the device.

It may also be possible to use tantalum or film capacitors at the device output, OUT, but these are not as attractive for reasons of size and cost (see the *Capacitor Characteristics* section below).

The output capacitor must meet the requirement for the minimum value of capacitance and have an ESR value that is within the range 5 mΩ to 500 mΩ for stability.

8.2.2.2.3 Capacitor Characteristics

The LP5900 is designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values in the range of 0.47 µF to 4.7 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 0.47-µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the equivalent series resistance (ESR) requirement for stability for the LP5900.

The temperature performance of ceramic capacitors varies by type and manufacturer. Most large value ceramic capacitors (≥ 2.2 µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

A better choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within ±15% over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47 µF to 4.7 µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

8.2.3 Application Curve

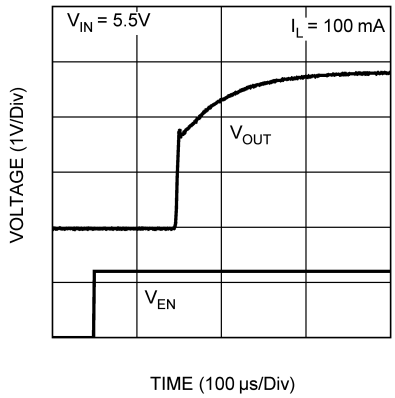


Figure 17. Enable Start-up Time, I_{OUT} = 100 mA, V_{OUT} = 2.8 V

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.5 V and 5.5 V. This input supply must be well regulated. To ensure that the LP5900 output voltage is well regulated, the input supply must be at least V_{OUT} + 1 V.

10 Layout

10.1 Layout Guidelines

The device is designed to operate from an input voltage supply range between 2.5 V and 5.5 V. This input supply must be well regulated. To ensure that the LP5900 output voltage is well regulated, the input supply must be at least V_{OUT} + 1 V.

10.2 Layout Examples

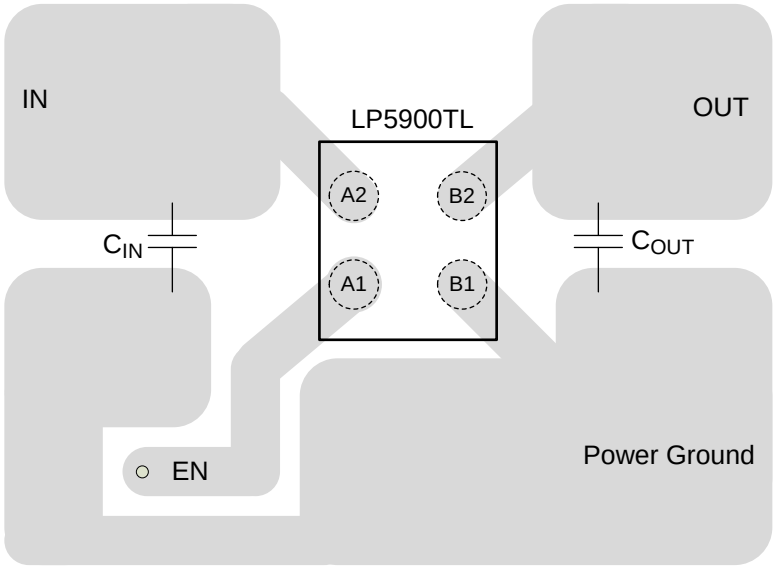


Figure 18. DSBGA Layout

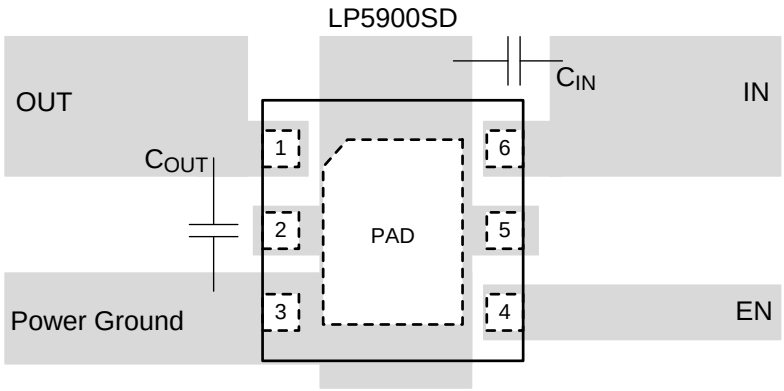


Figure 19. WSON Layout

10.3 DSBGA Mounting

The DSBGA package requires specific mounting techniques, which are detailed in *AN-1112 DSBGA Wafer Level Chip Scale Package* (SNVA009). For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

10.4 DSBGA Light Sensitivity

Exposing the DSBGA device to direct light may cause incorrect operation of the device. Light sources such as halogen lamps can affect electrical performance if they are situated in proximity to the device.

Light with wavelengths in the red and infra-red part of the spectrum has the most detrimental effect; thus, the fluorescent lighting used inside most buildings has very little effect on performance.

10.5 WSON Mounting

The 6-lead WSON package requires specific mounting techniques which are detailed in *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401). Referring to the section PCB Design Recommendations, it should be noted that the pad style which should be used with the WSON package is the NSMD (non-solder mask defined) type. Additionally, it is recommended the PCB terminal pads to be 0.2 mm longer than the package pads to create a solder fillet to improve reliability and inspection.

The exposed thermal pad on the bottom of the WSON package must be connected to a copper area on the PCB under the package. TI recommends use of thermal vias to remove heat from the package into the PCB is recommended. Connect the thermal pad to ground potential or leave floating. Do not connect the thermal pad to any potential other than the same ground potential seen at device pin 3.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

AN-1112 DSBGA Wafer Level Chip Scale Package (SNVA009)

AN-1112 AN-1112 *Leadless Leadframe Package (LLP)* (SNOA401)

IC Package Thermal Metrics application report (SPRA953)

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5900SD-1.5/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L15	Samples
LP5900SD-1.8/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L17	Samples
LP5900SD-2.0/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L18	Samples
LP5900SD-2.2/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L19	Samples
LP5900SD-2.5	NRND	WSON	NGF	6	1000	TBD	Call TI	Call TI	-40 to 125	L13	
LP5900SD-2.5/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L13	Samples
LP5900SD-2.7/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L14	Samples
LP5900SD-2.8/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L12	Samples
LP5900SD-3.0/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L20	Samples
LP5900SD-3.3/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L16	Samples
LP5900SDX-1.8/NOPB	ACTIVE	WSON	NGF	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L17	Samples
LP5900SDX-2.5/NOPB	ACTIVE	WSON	NGF	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L13	Samples
LP5900SDX-2.7/NOPB	ACTIVE	WSON	NGF	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L14	Samples
LP5900SDX-2.8/NOPB	ACTIVE	WSON	NGF	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L12	Samples
LP5900SDX-3.0/NOPB	ACTIVE	WSON	NGF	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L20	Samples
LP5900SDX-3.3/NOPB	ACTIVE	WSON	NGF	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L16	Samples
LP5900TL-1.5/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5900TL-1.8/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-1.9/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-2.0/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-2.2/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-2.3/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-2.5/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-2.6/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-2.65/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-2.7/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-2.75/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-2.8/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-2.85/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-3.0/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-3.3/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TL-4.5/NOPB	ACTIVE	DSBGA	YZR	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-1.5/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-1.8/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-2.1/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5900TLX-2.3/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-2.5/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-2.6/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-2.7/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-2.75/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-2.8/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-2.85/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-3.0/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900TLX-3.3/NOPB	ACTIVE	DSBGA	YZR	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900XR-2.8/NOPB	ACTIVE	DSBGA	YPF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP5900XRX-2.8/NOPB	ACTIVE	DSBGA	YPF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

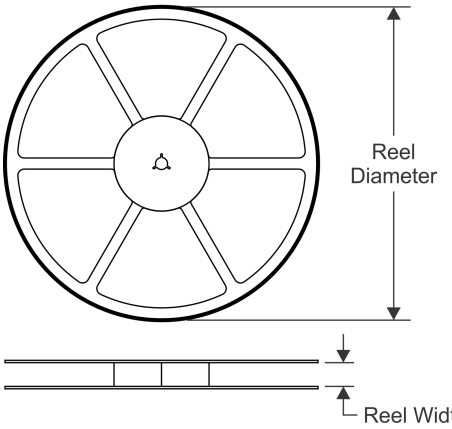
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

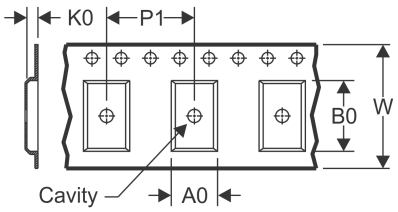
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

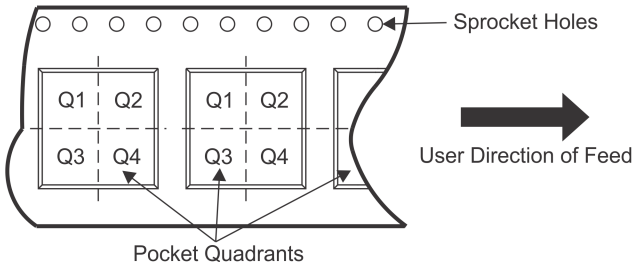


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

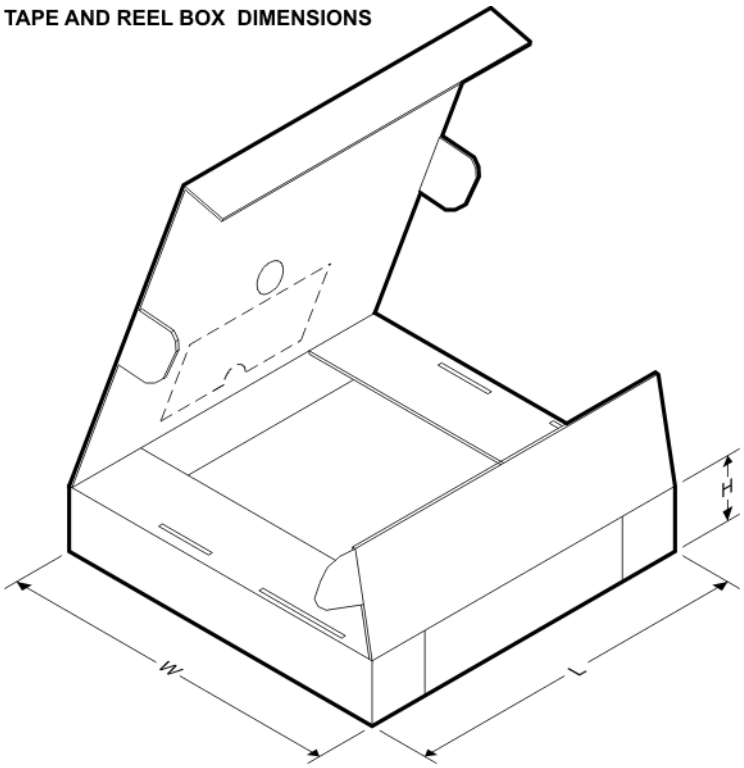


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5900SD-1.5/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SD-1.8/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SD-2.0/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SD-2.2/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SD-2.5	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SD-2.5/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SD-2.7/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SD-2.8/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SD-3.0/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SD-3.3/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SDX-1.8/NOPB	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SDX-2.5/NOPB	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SDX-2.7/NOPB	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SDX-2.8/NOPB	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SDX-3.0/NOPB	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900SDX-3.3/NOPB	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
LP5900TL-1.5/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-1.8/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5900TL-1.9/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-2.0/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-2.2/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-2.3/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-2.5/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-2.6/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-2.65/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-2.7/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-2.75/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-2.8/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-2.85/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-3.0/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-3.3/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TL-4.5/NOPB	DSBGA	YZR	4	250	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-1.5/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-1.8/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-2.1/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-2.3/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-2.5/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-2.6/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-2.7/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-2.75/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-2.8/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-2.85/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-3.0/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900TLX-3.3/NOPB	DSBGA	YZR	4	3000	178.0	8.4	1.15	1.16	0.79	4.0	8.0	Q1
LP5900XR-2.8/NOPB	DSBGA	YPF	4	250	178.0	8.4	1.16	1.2	0.4	4.0	8.0	Q1
LP5900XRX-2.8/NOPB	DSBGA	YPF	4	3000	178.0	8.4	1.16	1.2	0.4	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

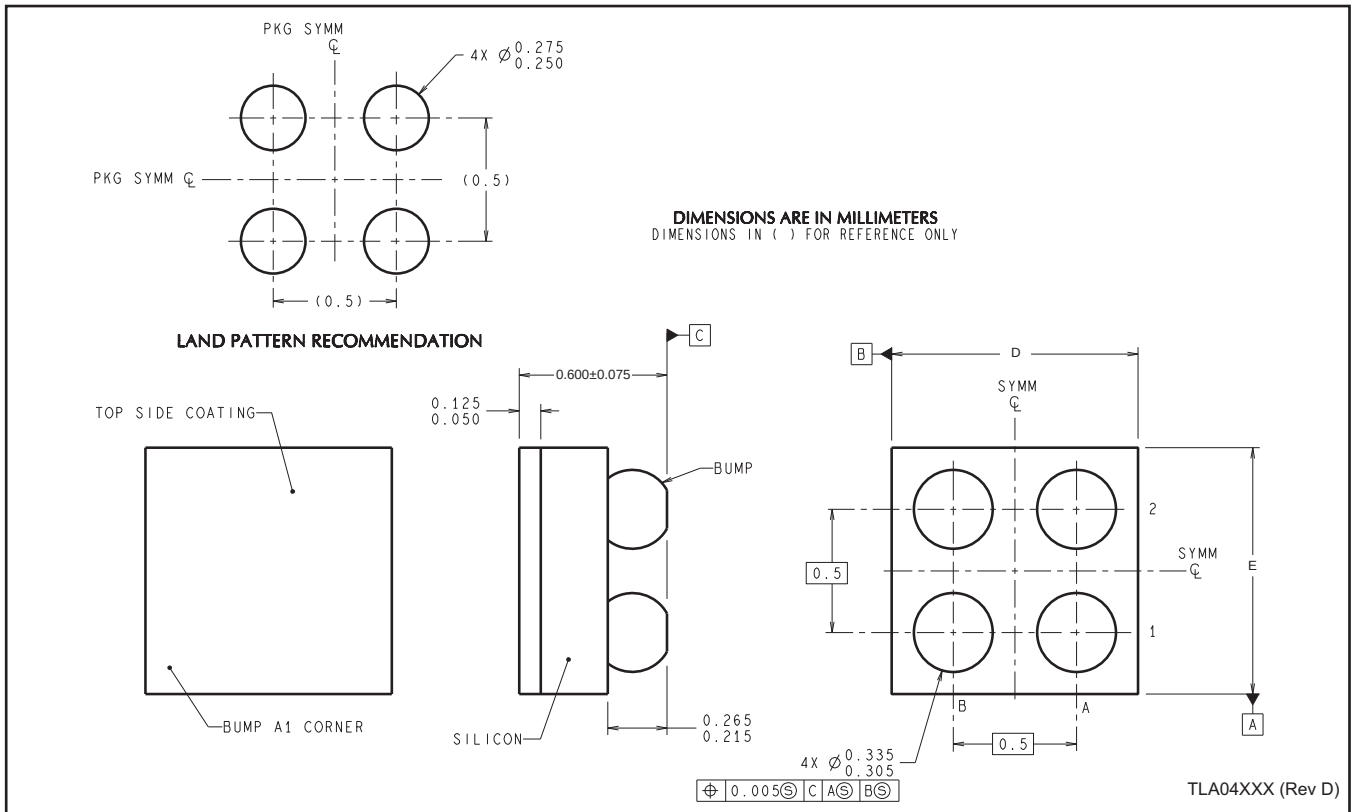


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5900SD-1.5/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LP5900SD-1.8/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LP5900SD-2.0/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LP5900SD-2.2/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LP5900SD-2.5	WSON	NGF	6	1000	210.0	185.0	35.0
LP5900SD-2.5/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LP5900SD-2.7/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LP5900SD-2.8/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LP5900SD-3.0/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LP5900SD-3.3/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
LP5900SDX-1.8/NOPB	WSON	NGF	6	4500	367.0	367.0	35.0
LP5900SDX-2.5/NOPB	WSON	NGF	6	4500	367.0	367.0	35.0
LP5900SDX-2.7/NOPB	WSON	NGF	6	4500	367.0	367.0	35.0
LP5900SDX-2.8/NOPB	WSON	NGF	6	4500	367.0	367.0	35.0
LP5900SDX-3.0/NOPB	WSON	NGF	6	4500	367.0	367.0	35.0
LP5900SDX-3.3/NOPB	WSON	NGF	6	4500	367.0	367.0	35.0
LP5900TL-1.5/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-1.8/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-1.9/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-2.0/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5900TL-2.2/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-2.3/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-2.5/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-2.6/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-2.65/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-2.7/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-2.75/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-2.8/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-2.85/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-3.0/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-3.3/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TL-4.5/NOPB	DSBGA	YZR	4	250	210.0	185.0	35.0
LP5900TLX-1.5/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-1.8/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-2.1/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-2.3/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-2.5/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-2.6/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-2.7/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-2.75/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-2.8/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-2.85/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-3.0/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900TLX-3.3/NOPB	DSBGA	YZR	4	3000	210.0	185.0	35.0
LP5900XR-2.8/NOPB	DSBGA	YPF	4	250	210.0	185.0	35.0
LP5900XRX-2.8/NOPB	DSBGA	YPF	4	3000	210.0	185.0	35.0

YZR0004



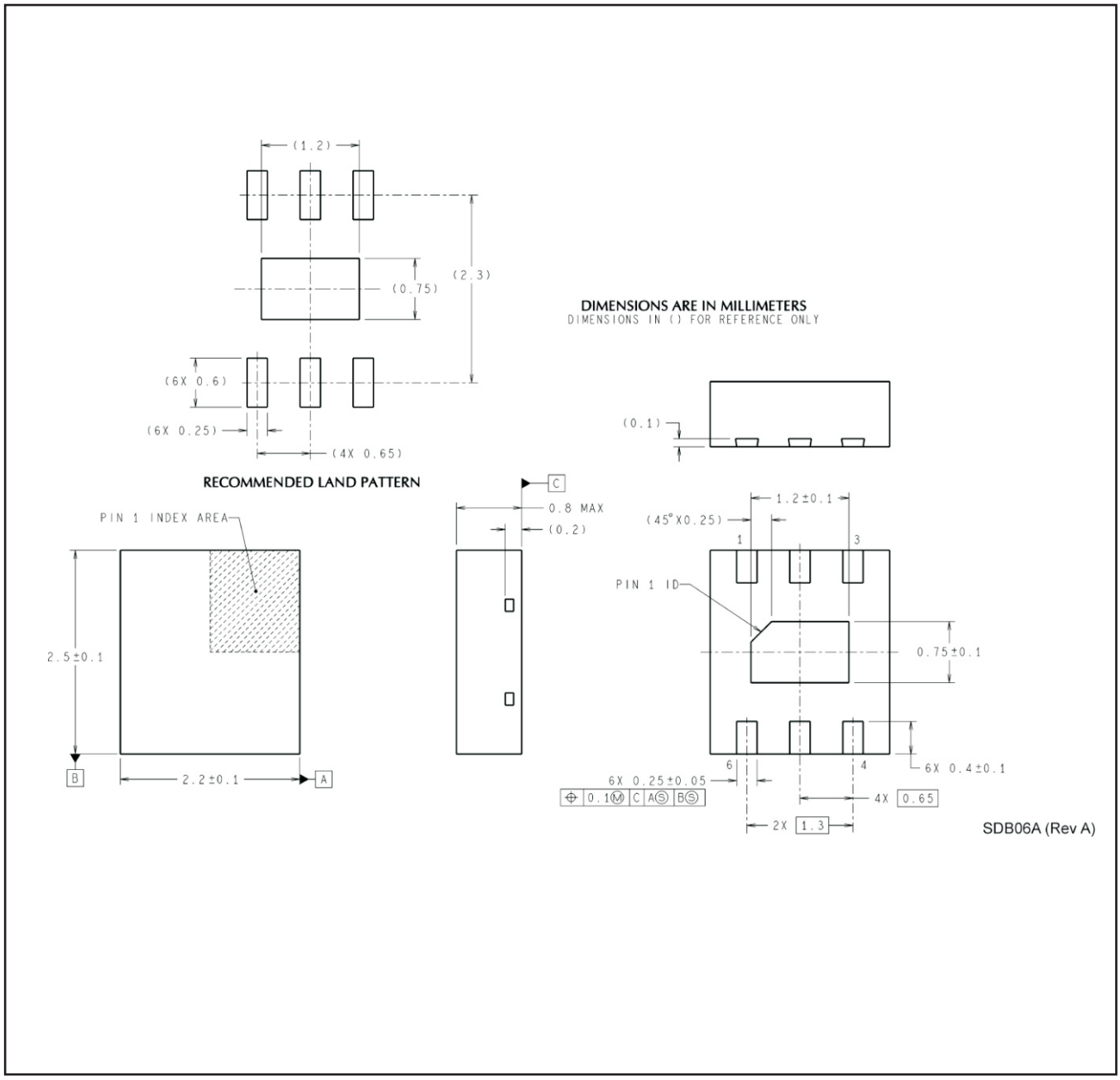
D: Max = 1.108 mm, Min =1.047 mm

E: Max = 1.083 mm, Min =1.022 mm

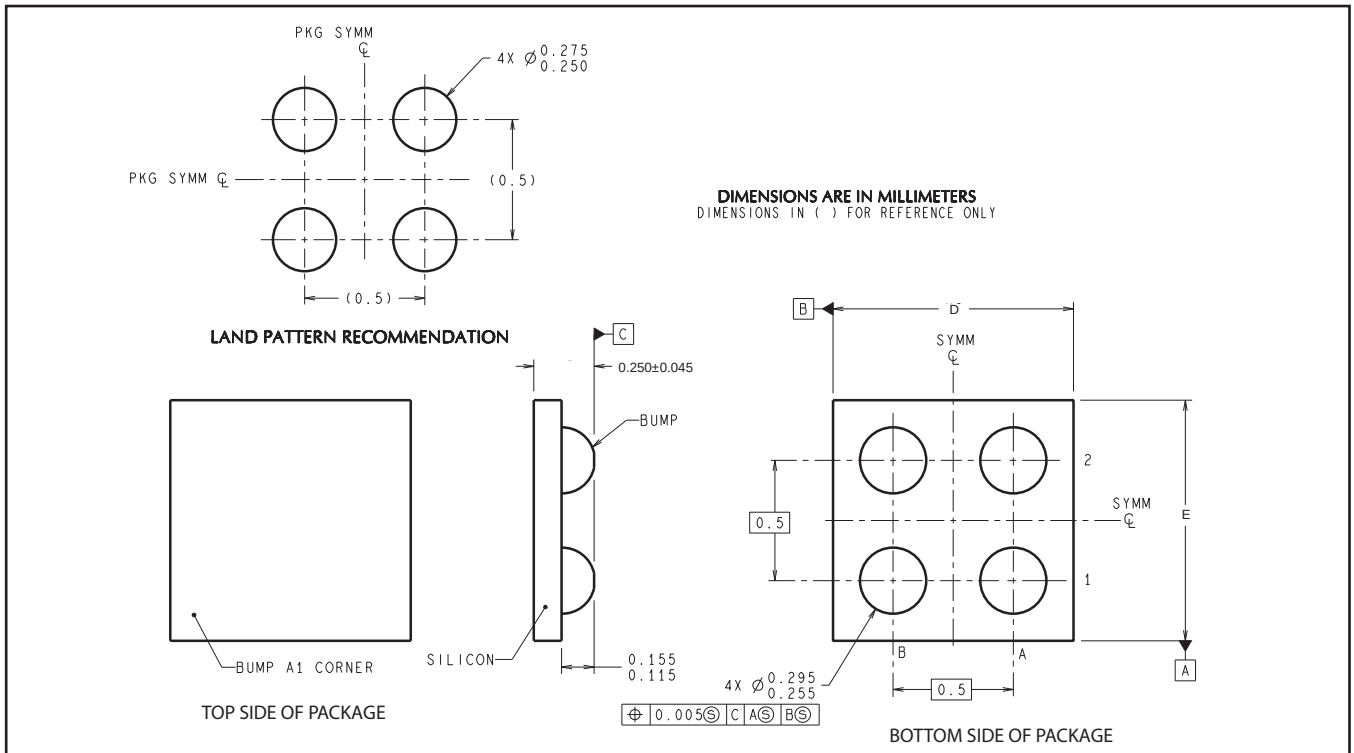
4215042/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

NGF0006A


(1.2)
(2.3)
(0.75)
(6X 0.6)
(6X 0.25)
(4X 0.65)
RECOMMENDED LAND PATTERN
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY
(0.1)
PIN 1 INDEX AREA
2.5±0.1
2.2±0.1
B
A
C
0.8 MAX
(0.2)
1.2±0.1
(45°X0.25)
1
3
PIN 1 ID
0.75±0.1
6
4
6X 0.4±0.1
6X 0.25±0.05
0.10 M C A S B S
4X 0.65
2X 1.3
SDB06A (Rev A)

YPF0004



D: Max = 1.108 mm, Min =1.047 mm

E: Max = 1.083 mm, Min =1.022 mm

4215204/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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