

## Low Dropout Regulator - Adjustable Current Limit

### 5 V to 20 V

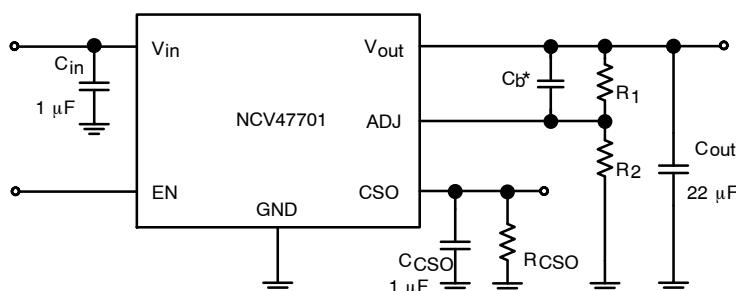
The NCV47701 is a 350 mA output current integrated low dropout regulator designed for use in harsh automotive environments. It includes wide operating temperature and input voltage ranges. The device is offered with adjustable voltage versions available in 3% output voltage accuracy. It has a high peak input voltage tolerance and reverse input voltage protection. It also provides overcurrent protection, overtemperature protection and enable for control of the state of the output voltage. The integrated current sense feature provides diagnosis and system protection functionality. The current limit of the device is adjustable by resistor connected to CSO pin. Voltage on CSO pin is proportional to output current.

#### Features

- Adjustable Voltage Version (from 5 V to 20 V)  $\pm 3\%$  Output Voltage for  $\pm 6\%$  Output Voltage Accuracy see NCV47700 Specification
- Enable Input (5 V Logic Compatible Thresholds) for 3.3 V Logic Compatible Thresholds see NCV47710 or NCV47711 Specification
- Adjustable Current Limit (from 10 mA to 350 mA) with 10% accuracy
- Protection Features:
  - ◆ Current Limitation
  - ◆ Thermal Shutdown
  - ◆ Reverse Input Voltage
- This is a Pb-Free Device

#### Typical Applications

- Audio and Infotainment System
- Instrument Cluster
- Navigation
- Satellite Radio



\*Required if usage of low ESR output capacitor  $C_{out}$  is demand, see Regulator Stability Considerations section.

Figure 1. Application Schematic



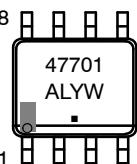
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#### MARKING DIAGRAMS



SOIC-8  
Exposed Pad  
PD SUFFIX  
CASE 751AC

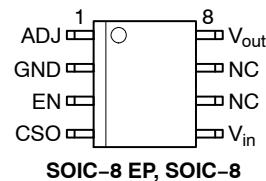


SOIC-8  
D SUFFIX  
CASE 751



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

#### PIN CONNECTIONS



#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

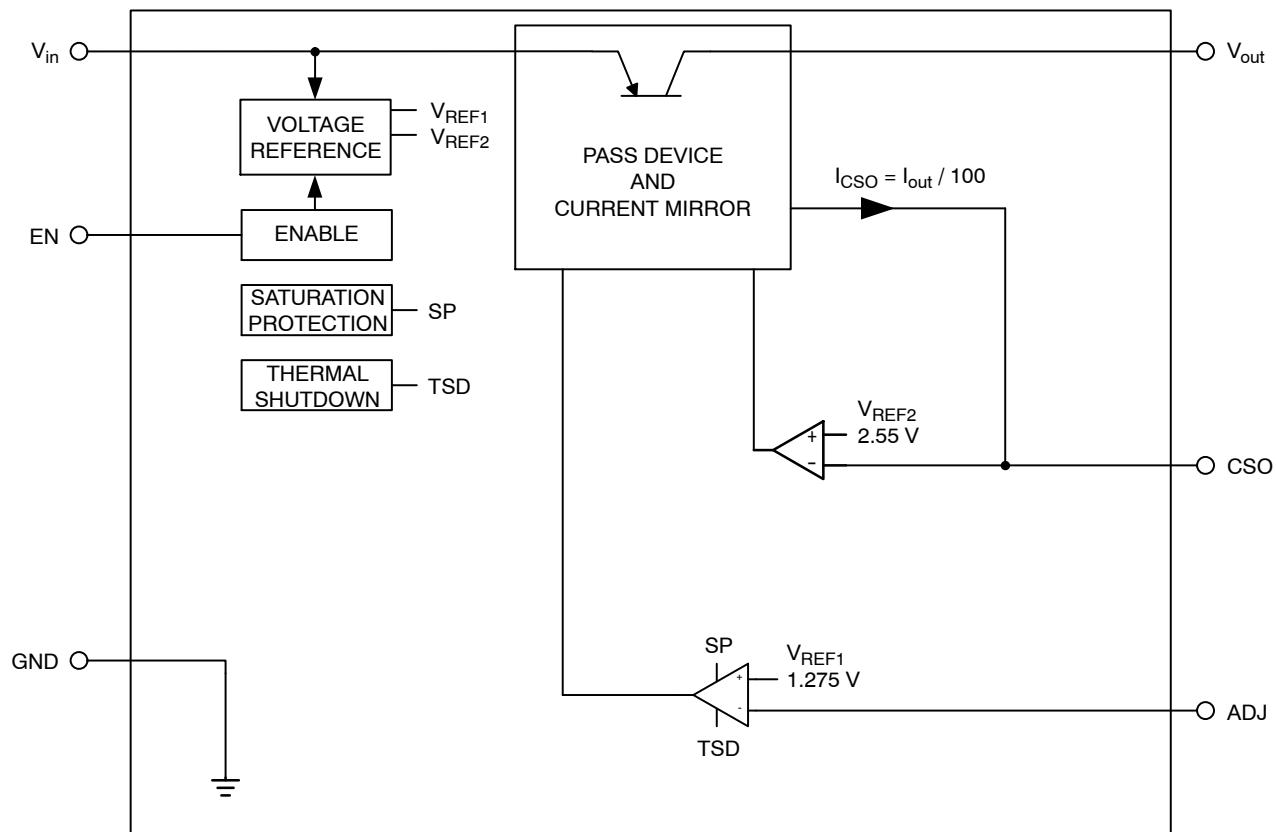


Figure 2. Simplified Block Diagram

## PIN FUNCTION DESCRIPTION

Pin No. SOIC-8 EP	Pin No. SOIC-8	Pin Name	Description
1	1	ADJ	Adjustable Voltage Setting Input. See Application Section for more details.
2	2	GND	Power Supply Ground.
3	3	EN	Enable Input; low level disables the IC.
4	4	CSO	Current Sense Output, Current Limit setting and Output Current value information. See Application Section for more details.
5	5	V <sub>in</sub>	Positive Power Supply Input.
6	6	NC	Not Connected
7	7	NC	Not Connected
8	8	V <sub>out</sub>	Regulated Output Voltage.
EPAD	-	EPAD	Connect to ground potential or leave unconnected.

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Rating	Symbol	Min	Max	Unit
Input Voltage	$V_{in}$	-42	45	V
Enable Input Voltage	$V_{EN}$	-42	45	V
Adjustable Input Voltage	$V_{ADJ}$	-0.3	10	V
CSO Voltage	$V_{CSO}$	-0.3	7	V
Output Voltage	$V_{out}$	-1	40	V
Junction Temperature	$T_J$	-40	150	°C
Storage Temperature	$T_{STG}$	-55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

## ESD CAPABILITY (Note 2)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	$ESD_{HBM}$	-2	2	kV
ESD Capability, Machine Model	$ESD_{MM}$	-200	200	V

2. This device series incorporates ESD protection and is tested by the following methods:

ESD Human Body Model tested per AEC-Q100-002 (JS-001-2010)

ESD Machine Model tested per AEC-Q100-003 (EIA/JESD22-A115)

Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes  $< 50\text{mm}^2$  due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS-002-2014.

## LEAD SOLDERING TEMPERATURE AND MSL (Note 3)

Rating	Symbol	Min	Max	Unit
Moisture Sensitivity Level	MSL	2 1		-

3. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

## THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SOIC-8 EP (single layer PCB) Thermal Resistance, Junction-to-Air (Note 4) Thermal Reference, Junction-to-Lead (Note 4)	$R_{\theta JA}$ $R_{\psi JL}$	70 19	°C/W
Thermal Characteristics, SOIC-8 EP (4 layers PCB) Thermal Resistance, Junction-to-Air (Note 4) Thermal Reference, Junction-to-Lead (Note 4)	$R_{\theta JA}$ $R_{\psi JL}$	29 12	°C/W
Thermal Characteristics, SOIC-8 (single layer PCB) Thermal Resistance, Junction-to-Air (Note 4) Thermal Reference, Junction-to-Lead (Note 4)	$R_{\theta JA}$ $R_{\psi JL}$	121 42	°C/W
Thermal Characteristics, SOIC-8 (4 layers PCB) Thermal Resistance, Junction-to-Air (Note 4) Thermal Reference, Junction-to-Lead (Note 4)	$R_{\theta JA}$ $R_{\psi JL}$	77 52	°C/W

4. Values based on copper area of  $645\text{ mm}^2$  (or  $1\text{ in}^2$ ) of 1 oz copper thickness and FR4 PCB substrate. Single layer – according to JEDEC51.3, 4 layers – according to JEDEC51.7.

## RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Input Voltage (Note 5)	$V_{in}$	5.5	40	V
Output Current Limit (Note 6)	$I_{LIM}$	10	350	mA
Junction Temperature	$T_J$	-40	150	°C
Nominal Output Voltage	$V_{out\_nom}$	5.0	20	V
Current Sense Output (CSO) Capacitor	$C_{CSO}$	1.0	4.7	μF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Minimum  $V_{in} = 5.5\text{ V}$  or  $(V_{out\_nom} + 0.5\text{ V})$ , whichever is higher.
6. Corresponding  $R_{CSO}$  is in range from  $25\text{ kΩ}$  down to  $728\text{ Ω}$ .

**ELECTRICAL CHARACTERISTICS**  $V_{in} = 13.5$  V,  $V_{EN} = 5$  V,  $R_{CSO} = 0$   $\Omega$ ,  $C_{CSO} = 1$   $\mu$ F,  $C_{in} = 1$   $\mu$ F,  $C_{out} = 22$   $\mu$ F,  $ESR = 1.5$   $\Omega$ , Min and Max values are valid for temperature range  $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$  unless otherwise noted and are guaranteed by test design or statistical correlation. Typical values are referenced to  $T_J = 25^\circ\text{C}$ .

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
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#### REGULATOR OUTPUT

Output Voltage (Accuracy %)	$V_{in} = (V_{out\_nom} + 1$ V) to 40 V, $I_{out} = 5$ mA to 350 mA	$V_{out}$	-3	-	3	%
Line Regulation	$V_{in} = (V_{out\_nom} + 1$ V) to $(V_{out\_nom} + 20$ V), $I_{out} = 5$ mA	$Reg_{line}$	-	0.1	1.0	%
Load Regulation	$I_{out} = 5$ mA to 350 mA	$Reg_{load}$	-	0.14	1.4	%
Dropout Voltage (Note 7)	$I_{out} = 150$ mA, $V_{DO} = V_{in} - V_{out}$	$V_{DO}$	-	250	500	mV

#### DISABLE AND QUIESCENT CURRENTS

Disable Current	$V_{EN} = 0$ V $V_{EN} = 0$ V, $T_J = 25^\circ\text{C}$	$I_{DIS}$	-	-	85	$10$ $-\mu\text{A}$ $\text{nA}$
Quiescent Current, $I_q = I_{in} - I_{out}$	$I_{out} = 1$ mA, $V_{in} = (V_{out\_nom} + 8.5$ V)	$I_q$	-	150	230	$\mu\text{A}$
Quiescent Current, $I_q = I_{in} - I_{out}$	$I_{out} = 350$ mA, $V_{in} = (V_{out\_nom} + 8.5$ V)	$I_q$	-	23	50	mA

#### CURRENT LIMIT PROTECTION

Current Limit	$V_{out} = 0.9 \times V_{out\_nom}$ , $V_{in} = (V_{out\_nom} + 8.5$ V)	$I_{LIM}$	400	-	-	mA
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#### PSRR & NOISE

Power Supply Ripple Rejection	$f = 100$ Hz, 0.5 $V_{p-p}$ , $I_{out} = 5$ mA, $C_{in} = \text{none}$	$PSRR$	-	70	-	$\text{dB}$
Output Noise Voltage	$f = 10$ Hz to 100 kHz, $C_b = 10$ nF, $I_{out} = 5$ mA	$V_n$	-	100	-	$\mu\text{V}_{\text{rms}}$

#### ENABLE

Enable Input Threshold Voltage Logic Low (OFF) Logic High (ON)	$V_{out} \leq 0.1$ V $V_{out} \geq 0.9 \times V_{out\_nom}$	$V_{th(EN)}$	0.8 -	2.4 2.7	- 3.5	V
Enable Input Current	$V_{EN} = 5$ V	$I_{EN}$	2.0	8.0	20	$\mu\text{A}$
Turn On Time from Enable ON to 90% of $V_{out\_nom}$	$I_{out} = 100$ mA, $C_b = 10$ nF, $R_1 = 82$ k $\Omega$ , $R_2 = 27$ k $\Omega$	$t_{on}$	-	1.6	-	ms

#### OUTPUT CURRENT SENSE

CSO Voltage Level at Current Limit	$V_{out} = 0.9 \times V_{out\_nom}$ , ( $V_{out\_nom} = 5$ V) $R_{CSO} = 1$ k $\Omega$	$V_{CSO\_llim}$	2.346 (-8 %)	2.55	2.754 (+8 %)	V
CSO Transient Voltage Level	$C_{CSO} = 4.7$ $\mu$ F, $R_{CSO} = 1$ k $\Omega$ , $I_{out}$ pulse from 10 mA to 350 mA, $t_r = 1$ $\mu$ s	$V_{CSO}$	-	-	3.0	V
CSO Current to Output Current Ratio (Note 8)	$V_{CSO} = 2$ V, $I_{out} = 10$ mA to 350 mA, ( $V_{out\_nom} = 5$ V)	$I_{CSO}/I_{out}$	- (-10%)	(1/100)	- (+10%)	-
CSO Current at No Load Current	$V_{CSO} = 0$ V, $I_{out} = 0$ mA, ( $V_{out\_nom} = 5$ V)	$I_{CSO\_off}$	-	-	10	$\mu\text{A}$

#### REVERSE CURRENT

Reverse Current (Note 9)	$V_{in} = 12$ V, $V_{out} = 14$ V	$I_{out\_rev}$	-40	-25	-	mA
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#### THERMAL SHUTDOWN

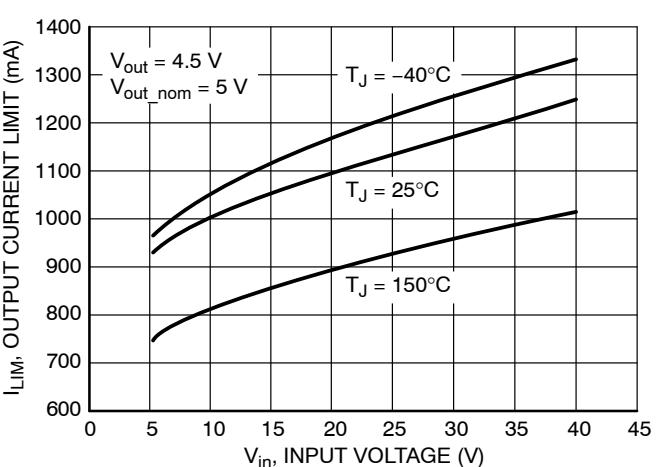
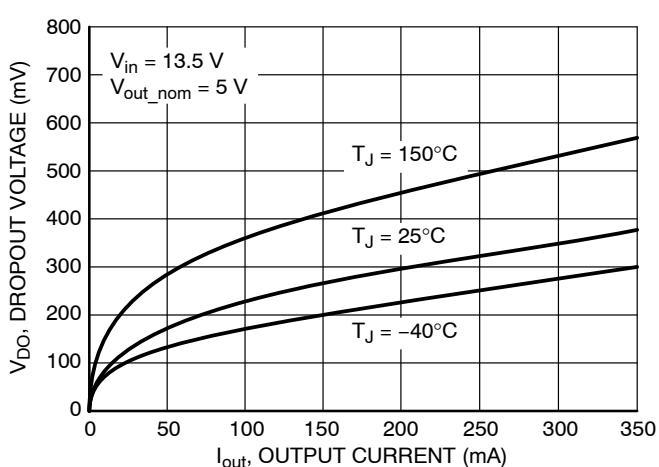
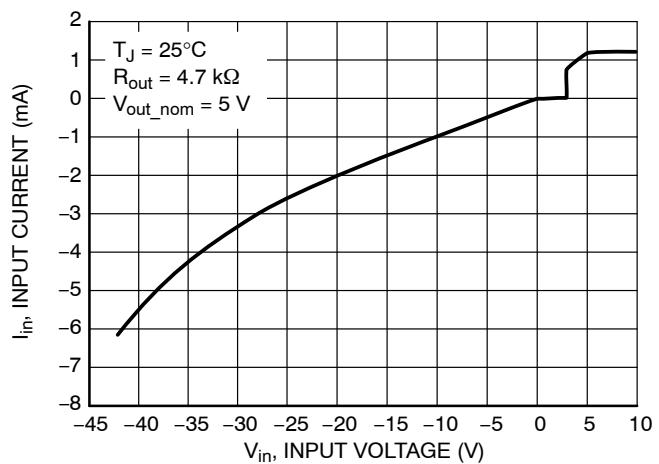
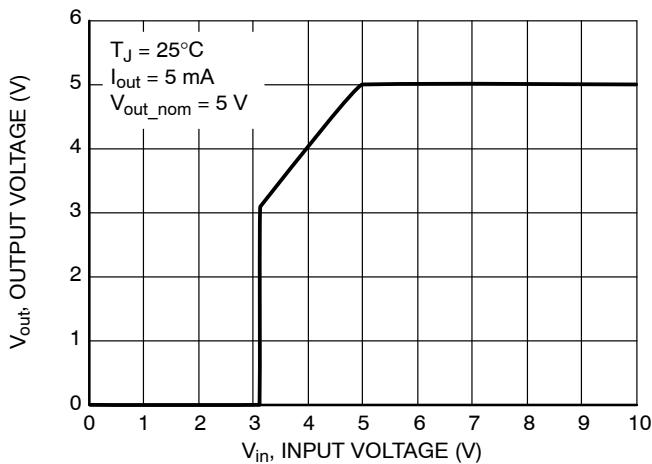
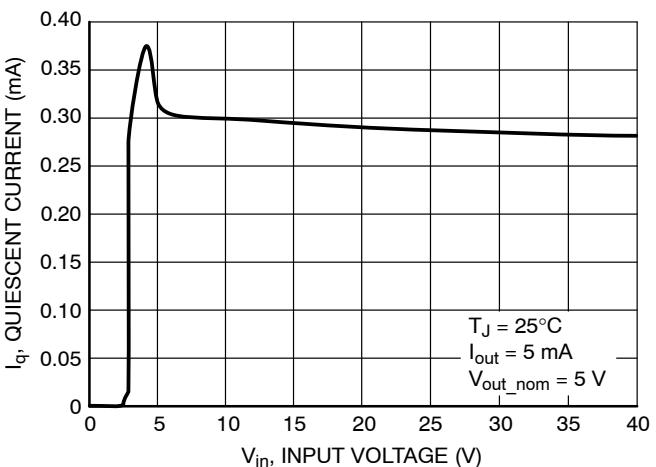
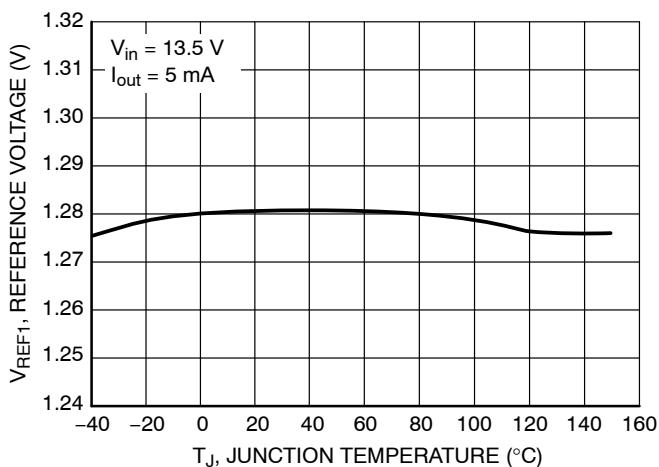
Thermal Shutdown Temperature	$I_{out} = 5$ mA	$T_{SD}$	150	-	195	$^\circ\text{C}$
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7. Measured when the output voltage  $V_{out}$  has dropped -2% from the nominal value obtained at  $V_{in} = V_{out\_nom} + 8.5$  V.

8. Not guaranteed in dropout.

9. Values based on design and/or characterization.

## TYPICAL CHARACTERISTICS



## TYPICAL CHARACTERISTICS

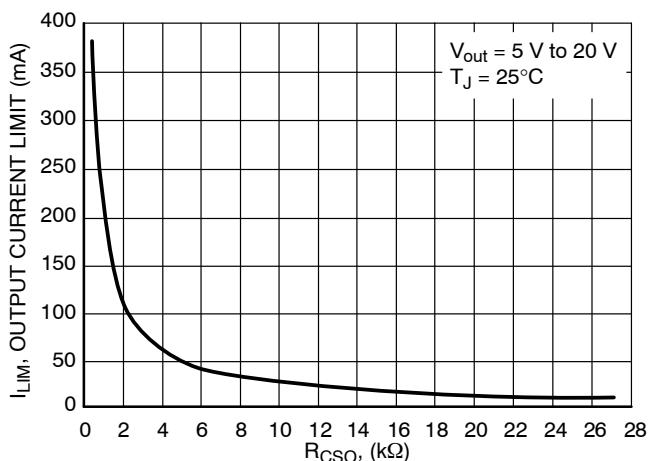
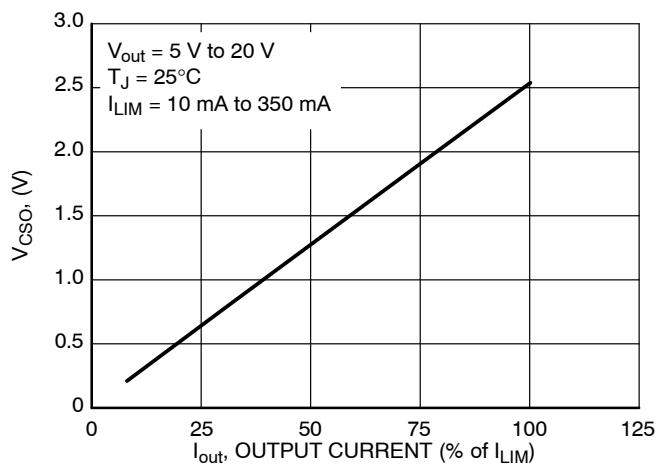
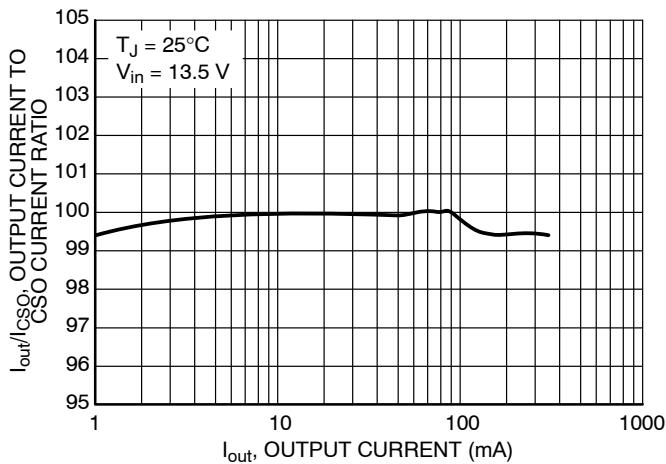
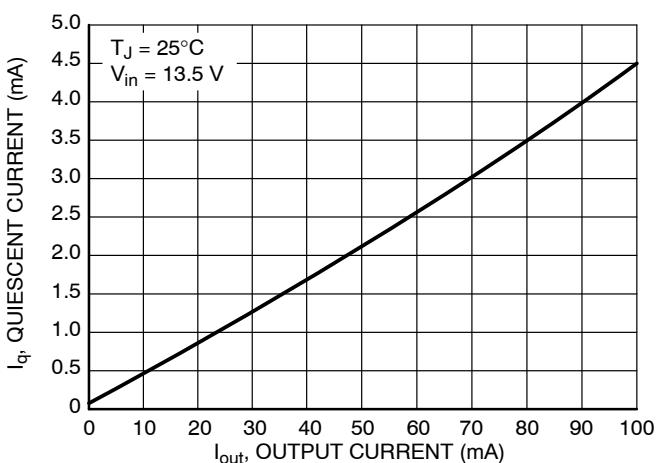
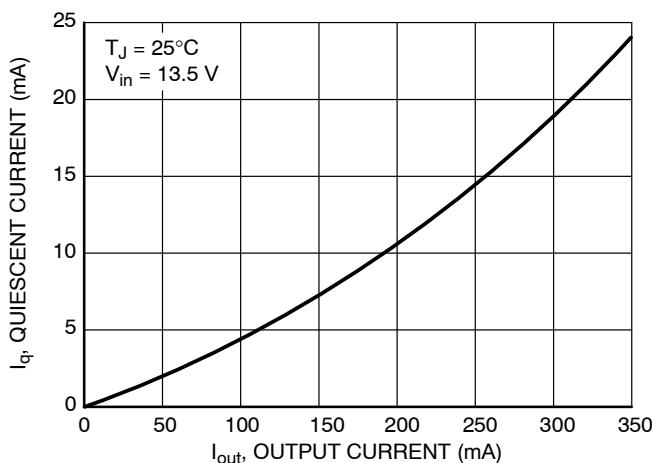
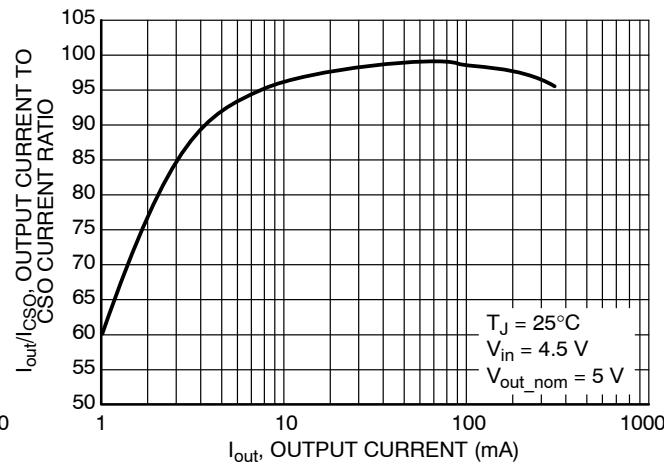
Figure 9. Output Current Limit vs.  $R_{CS0}$ Figure 10. Output Current (% of  $I_{LIM}$ ) vs. CSO Voltage

Figure 11. Output Current to CSO Current Ratio vs. Output Current



## TYPICAL CHARACTERISTICS

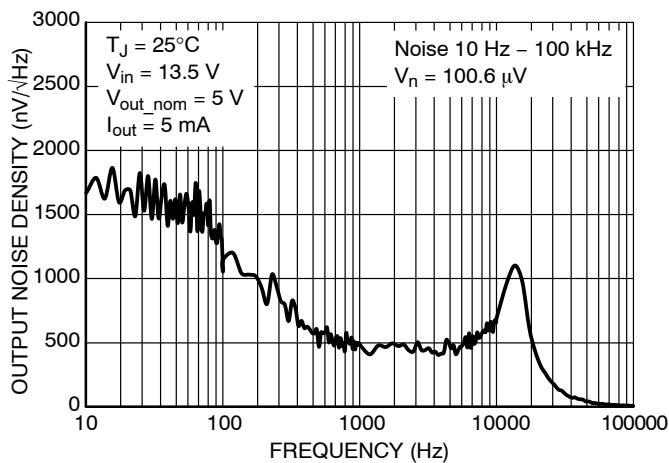


Figure 15. Output Noise Density vs. Frequency

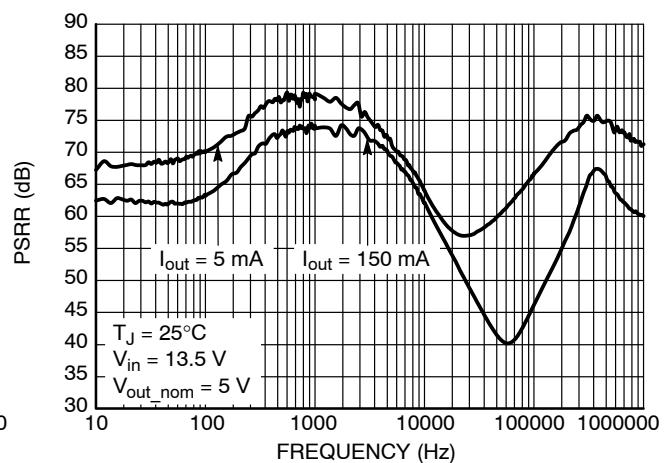
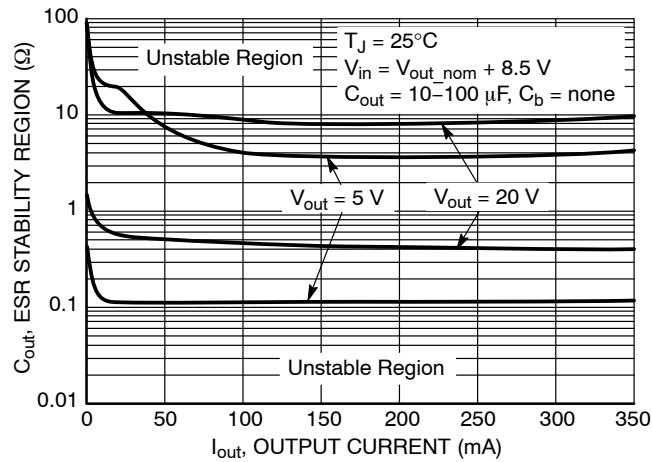


Figure 16. PSRR vs. Frequency

Figure 17.  $C_{out}$  ESR Stability Region vs. Output Current

**DEFINITIONS****General**

All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

**Output Voltage**

The output voltage parameter is defined for specific temperature, input voltage and output current values or specified over Line, Load and Temperature ranges.

**Line Regulation**

The change in output voltage for a change in input voltage measured for specific output current over operating ambient temperature range.

**Load Regulation**

The change in output voltage for a change in output current measured for specific input voltage over operating ambient temperature range.

**Dropout Voltage**

The input to output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. It is measured when the output voltage  $V_{out}$  has dropped -2% from the nominal value obtained at  $V_{in} = V_{out\_nom} + 8.5$  V. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

**Quiescent and Disable Currents**

Quiescent Current ( $I_q$ ) is the difference between the input current (measured through the LDO input pin) and the output load current. If Enable pin is set to LOW the regulator

reduces its internal bias and shuts off the output, this term is called the disable current ( $I_{DIS}$ ).

**Current Limit**

Current Limit is value of output current by which output voltage drops below 90% of its nominal value.

**PSRR**

Power Supply Rejection Ratio is defined as ratio of output voltage and input voltage ripple. It is measured in decibels (dB).

**Line Transient Response**

Typical output voltage overshoot and undershoot response when the input voltage is excited with a given slope.

**Load Transient Response**

Typical output voltage overshoot and undershoot response when the output current is excited with a given slope between low-load and high-load conditions.

**Thermal Protection**

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 175°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

**Maximum Package Power Dissipation**

The power dissipation level is maximum allowed power dissipation for particular package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

## APPLICATIONS INFORMATION

**Circuit Description**

The NCV47701 is an integrated low dropout regulator that provides a regulated voltage at 350 mA to the output. It is enabled with an input to the enable pin. The regulator voltage is provided by a PNP pass transistor controlled by an error amplifier with a bandgap reference, which gives it the lowest possible dropout voltage. The output current capability is 350 mA, and the base drive quiescent current is controlled to prevent oversaturation when the input voltage is low or when the output is overloaded. The integrated current sense feature provides diagnosis and system protection functionality. The current limit of the device is adjustable by resistor connected to CSO pin. Voltage on CSO pin is proportional to output current. The regulator is protected by both current limit and thermal shutdown. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures.

**Regulator**

The error amplifier compares the reference voltage to a sample of the output voltage ( $V_{out}$ ) and drives the base of a PNP series pass transistor via a buffer. The reference is a bandgap design to give it a temperature-stable output. Saturation control of the PNP is a function of the load current and input voltage. Oversaturation of the output power device is prevented, and quiescent current in the ground pin is minimized.

**Regulator Stability Considerations**

The input capacitor ( $C_{in}$ ) is necessary to stabilize the input impedance to avoid voltage line influences. The output capacitor ( $C_{out}$ ) helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures ( $-25^{\circ}\text{C}$  to  $-40^{\circ}\text{C}$ ), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information. The value for the output capacitor  $C_{out}$ , shown in Figure 1 should work for most applications; see also Figure 17 for output stability at various load and Output Capacitor ESR conditions. Stable region of ESR in Figure 17 shows ESR values at which the LDO output voltage does not have any permanent oscillations at any dynamic changes of output load current. Marginal ESR is the value at which the output voltage waving is fully damped during four periods after the load change and no oscillation is further observable.

ESR characteristics were measured with ceramic capacitors and additional series resistors to emulate ESR. Low duty cycle pulse load current technique has been used to maintain junction temperature close to ambient temperature.

**Calculating Bypass Capacitor**

If usage of low ESR ceramic capacitors is demanded, connect the bypass capacitor  $C_b$  between Adjustable Input pin and  $V_{out}$  pin according to Applications circuit at Figure 1. Parallel combination of bypass capacitor  $C_b$  with the feedback resistor  $R_1$  contributes in the device transfer function as an additional zero and affects the device loop stability, therefore its value must be optimized. Attention to the Output Capacitor value and its ESR must be paid. See also Stability in High Speed Linear LDO Regulators Application Note, AND8037/D for more information. Optimal value of bypass capacitor is given by following expression:

$$C_b = \frac{1}{2 \times \pi \times f_z \times R_1} \quad (\text{eq. 1})$$

where

$R_1$  – the upper feedback resistor

$f_z$  – the frequency of the zero added into the device transfer function by  $R_1$  and  $C_b$  external components.

Set the  $R_1$  resistor according to output voltage requirement. Choose the  $f_z$  with regard on the output capacitance  $C_{out}$ , refer to the table below.

$C_{out}$ ( $\mu\text{F}$ )	10	22	47	100
$f_z$ range (kHz)	3.3–48.2	1.5–33	1.5–33	2.2–22

Ceramic capacitors and its part numbers listed below have been used as low ESR output capacitors  $C_{out}$  from the table above to define the frequency ranges of additional zero required for stability:

GRM31CR71C106KAC7 (10  $\mu\text{F}$ , 16 V, X7R, 1206)

GRM32ER71C226KE18 (22  $\mu\text{F}$ , 16 V, X7R, 1210)

GRM32ER61C476ME15 (47  $\mu\text{F}$ , 16 V, X5R, 1210)

GRM32ER60J107ME20 (100  $\mu\text{F}$ , 6.3 V, X5R, 1210)

**Enable Input**

The enable pin is used to turn the regulator on or off. By holding the pin down to a voltage less than 0.8 V, the output of the regulator will be turned off. When the voltage on the enable pin is greater than 3.5 V, the output of the regulator will be enabled to power its output to the regulated output voltage. The enable pin may be connected directly to the input pin to give constant enable to the output regulator.

**Setting the Output Voltage**

The output voltage range can be set between 5 V and 20 V. This is accomplished with an external resistor divider feeding back the voltage to the IC back to the error amplifier by the voltage adjust pin ADJ. The internal reference voltage is set to a temperature stable reference ( $V_{REF1}$ ) of 1.275 V.

The output voltage is calculated from the following formula. Ignoring the bias current into the ADJ pin:

$$V_{\text{out}} = V_{\text{REF1}} \left( 1 + \frac{R_1}{R_2} \right) \quad (\text{eq. 2})$$

Use  $R_2 < 50 \text{ k}\Omega$  to avoid significant voltage output errors due to ADJ bias current.

Designers should consider the tolerance of  $R_1$  and  $R_2$  during the design phase.

### Setting the Output Current Limit

The output current limit can be set between 10 mA and 350 mA by external resistor  $R_{\text{CSO}}$  (see Figure 1). Capacitor  $C_{\text{CSO}}$  of 1  $\mu\text{F}$  in parallel with  $R_{\text{CSO}}$  is required for stability of current limit control circuitry (see Figure 1).

$$V_{\text{CSO}} = I_{\text{out}} \left( R_{\text{CSO}} \times \frac{1}{100} \right) \quad (\text{eq. 3})$$

$$I_{\text{LIM}} = \frac{100}{1} \times \frac{2.55}{R_{\text{CSO}}} \quad (\text{eq. 4})$$

$$R_{\text{CSO}} = \frac{100}{1} \times \frac{2.55}{I_{\text{LIM}}} \quad (\text{eq. 5})$$

Where

$R_{\text{CSO}}$	- current limit setting resistor
$V_{\text{CSO}}$	- voltage at CSO pin proportional to $I_{\text{out}}$
$I_{\text{LIM}}$	- current limit value
$I_{\text{out}}$	- output current actual value

CSO pin provides information about output current actual value. The CSO voltage is proportional to output current according to Equation 3.

Once output current reaches its limit value ( $I_{\text{LIM}}$ ) set by external resistor  $R_{\text{CSO}}$  than voltage at CSO pin is typically 2.55 V. Calculations of  $I_{\text{LIM}}$  or  $R_{\text{CSO}}$  values can be done using equations Equation 4 and Equation 5, respectively.

### Thermal Considerations

As power in the NCV47701 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV47701 has good thermal conductivity through the PCB, the junction temperature will be relatively low with

high power applications. The maximum dissipation the NCV47701 can handle is given by:

$$P_{\text{D}(\text{MAX})} = \frac{[T_{\text{J}(\text{MAX})} - T_{\text{A}}]}{R_{\theta\text{JA}}} \quad (\text{eq. 6})$$

Since  $T_{\text{J}}$  is not recommended to exceed 150°C, then the NCV47701 soldered on 645 mm<sup>2</sup>, 1 oz copper area, FR4 can dissipate up to 1.8 W (SOIC-8 EP) or 1 W (SOIC-8) and up to 4.3 W (SOIC-8 EP) or 1.6 W (SOIC-8) for 4 layers PCB (all layers are 1 oz) when the ambient temperature ( $T_{\text{A}}$ ) is 25°C. See Figure 18 for  $R_{\theta\text{JA}}$  versus PCB area. The power dissipated by the NCV47701 can be calculated from the following equations:

$$P_{\text{D}} = V_{\text{in}}(I_{\text{q}}@I_{\text{out}}) + I_{\text{out}}(V_{\text{in}} - V_{\text{out}}) \quad (\text{eq. 7})$$

or

$$V_{\text{in}(\text{MAX})} \approx \frac{P_{\text{D}(\text{MAX})} + (V_{\text{out}} \times I_{\text{out}})}{I_{\text{out}} + I_{\text{q}}} \quad (\text{eq. 8})$$

### Hints

$V_{\text{in}}$  and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV47701 and make traces as short as possible.

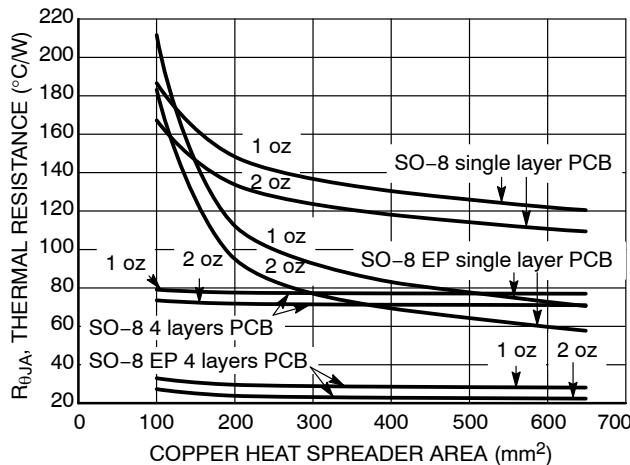


Figure 18. Thermal Resistance vs. PCB Copper Area

### ORDERING INFORMATION

Device	Output Voltage	Marking	Package	Shipping <sup>†</sup>
NCV47701PDAJR2G	Adjustable	47701	SOIC-8 EP (Pb-Free)	2500 / Tape & Reel
NCV47701DAJR2G	Adjustable	47701	SOIC-8 (Pb-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**MECHANICAL CASE OUTLINE**  
PACKAGE DIMENSIONS

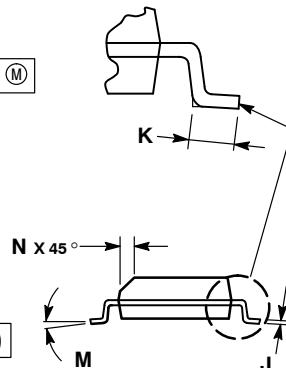
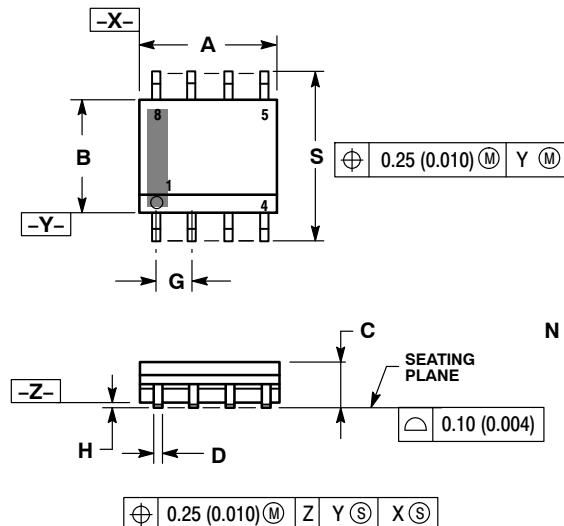
**onsemi**<sup>TM</sup>



SCALE 1:1

**SOIC-8 NB**  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011

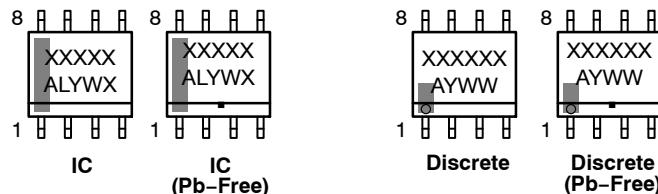


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

**GENERIC  
MARKING DIAGRAM\***



XXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SCALE 6:1 (mm/inches)

**STYLES ON PAGE 2**

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DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

STYLE 1: PIN 1. Emitter 2. Collector 3. Collector 4. Emitter 5. Emitter 6. Base 7. Base 8. Emitter	STYLE 2: PIN 1. Collector, Die #1 2. Collector, #1 3. Collector, #2 4. Collector, #2 5. Base, #2 6. Emitter, #2 7. Base, #1 8. Emitter, #1	STYLE 3: PIN 1. Drain, Die #1 2. Drain, #1 3. Drain, #2 4. Drain, #2 5. Gate, #2 6. Source, #2 7. Gate, #1 8. Source, #1	STYLE 4: PIN 1. Anode 2. Anode 3. Anode 4. Anode 5. Anode 6. Anode 7. Anode 8. Common Cathode
STYLE 5: PIN 1. Drain 2. Drain 3. Drain 4. Drain 5. Gate 6. Gate 7. Source 8. Source	STYLE 6: PIN 1. Source 2. Drain 3. Drain 4. Source 5. Source 6. Gate 7. Gate 8. Source	STYLE 7: PIN 1. Input 2. External Bypass 3. Third Stage Source 4. Ground 5. Drain 6. Gate 3 7. Second Stage Vd 8. First Stage Vd	STYLE 8: PIN 1. Collector, Die #1 2. Base, #1 3. Base, #2 4. Collector, #2 5. Collector, #2 6. Emitter, #2 7. Emitter, #1 8. Collector, #1
STYLE 9: PIN 1. Emitter, Common 2. Collector, Die #1 3. Collector, Die #2 4. Emitter, Common 5. Emitter, Common 6. Base, Die #2 7. Base, Die #1 8. Emitter, Common	STYLE 10: PIN 1. Ground 2. Bias 1 3. Output 4. Ground 5. Ground 6. Bias 2 7. Input 8. Ground	STYLE 11: PIN 1. Source 1 2. Gate 1 3. Source 2 4. Gate 2 5. Drain 2 6. Drain 2 7. Drain 1 8. Drain 1	STYLE 12: PIN 1. Source 2. Source 3. Source 4. Gate 5. Drain 6. Drain 7. Drain 8. Drain
STYLE 13: PIN 1. N.C. 2. Source 3. Source 4. Gate 5. Drain 6. Drain 7. Drain 8. Drain	STYLE 14: PIN 1. N-Source 2. N-Gate 3. P-Source 4. P-Gate 5. P-Drain 6. P-Drain 7. N-Drain 8. N-Drain	STYLE 15: PIN 1. Anode 1 2. Anode 1 3. Anode 1 4. Anode 1 5. Cathode, Common 6. Cathode, Common 7. Cathode, Common 8. Cathode, Common	STYLE 16: PIN 1. Emitter, Die #1 2. Base, Die #1 3. Emitter, Die #2 4. Base, Die #2 5. Collector, Die #2 6. Collector, Die #2 7. Collector, Die #1 8. Collector, Die #1
STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC	STYLE 18: PIN 1. Anode 2. Anode 3. Source 4. Gate 5. Drain 6. Drain 7. Cathode 8. Cathode	STYLE 19: PIN 1. Source 1 2. Gate 1 3. Source 2 4. Gate 2 5. Drain 2 6. Mirror 2 7. Drain 1 8. Mirror 1	STYLE 20: PIN 1. Source (N) 2. Gate (N) 3. Source (P) 4. Gate (P) 5. Drain 6. Drain 7. Drain 8. Drain
STYLE 21: PIN 1. Cathode 1 2. Cathode 2 3. Cathode 3 4. Cathode 4 5. Cathode 5 6. Common Anode 7. Common Anode 8. Cathode 6	STYLE 22: PIN 1. I/O Line 1 2. Common Cathode/VCC 3. Common Cathode/VCC 4. I/O Line 3 5. Common Anode/GND 6. I/O Line 4 7. I/O Line 5 8. Common Anode/GND	STYLE 23: PIN 1. Line 1 IN 2. Common Anode/GND 3. Common Anode/GND 4. Line 2 IN 5. Line 2 OUT 6. Common Anode/GND 7. Common Anode/GND 8. Line 1 OUT	STYLE 24: PIN 1. Base 2. Emitter 3. Collector/Anode 4. Collector/Anode 5. Cathode 6. Cathode 7. Collector/Anode 8. Collector/Anode
STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT	STYLE 26: PIN 1. GND 2. dv/dt 3. Enable 4. ILIMIT 5. Source 6. Source 7. Source 8. VCC	STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN	STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBUCK 7. VBUCK 8. VIN
STYLE 29: PIN 1. Base, Die #1 2. Emitter, #1 3. Base, #2 4. Emitter, #2 5. Collector, #2 6. Collector, #2 7. Collector, #1 8. Collector, #1	STYLE 30: PIN 1. Drain 1 2. Drain 1 3. Gate 2 4. Source 2 5. Source 1/Drain 2 6. Source 1/Drain 2 7. Source 1/Drain 2 8. Gate 1		

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®

ON



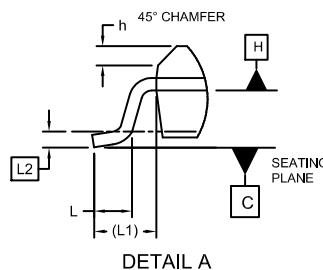
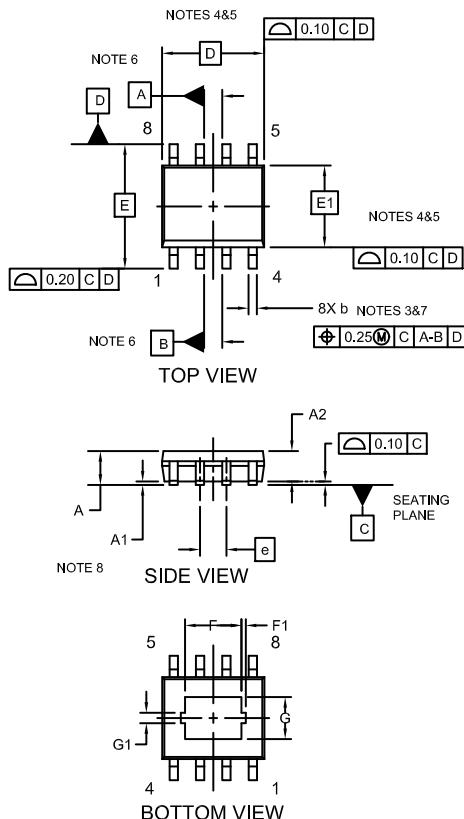
SCAL F 1:1

**SOIC-8 EP**  
CASE 751AC  
ISSUE D

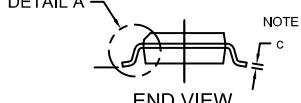
DATE 02 APR 2019

## NOTES:

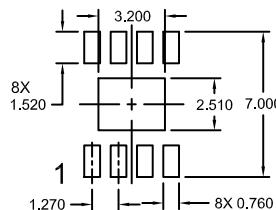
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION, ALLOWABLE PROTRUSION SHALL BE 0.004 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS, MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



#### DETAIL A



END VIEW

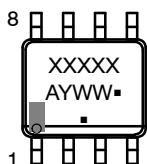


**RECOMMENDED**

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.35	1.55	1.75
A1	--	0.05	0.10
A2	1.35	1.50	1.65
b	0.31	0.41	0.51
c	0.17	0.21	0.23
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
F	2.24	2.72	3.20
F1	0.15	0.20	0.25
G	1.55	2.03	2.51
G1	0.41	0.46	0.51
h	0.25	0.38	0.50
L	0.40	0.84	1.27
L1	1.04 REF		
L2	0.25 REF		
Ø	0°	4°	8°

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERPMB.

## GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present and may be in either location. Some products may not follow the Generic Marking.

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