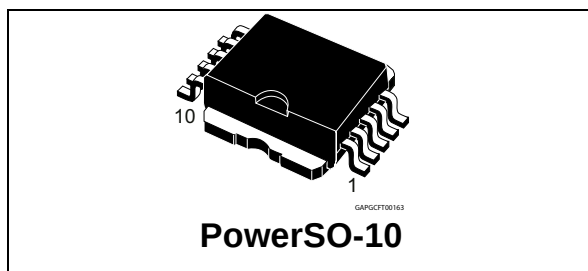


## Single-channel high-side driver with analog current sense for 24 V automotive applications

Datasheet — production data



### Features

|                              |           |                 |
|------------------------------|-----------|-----------------|
| Max transient supply voltage | $V_{CC}$  | 58 V            |
| Operating voltage range      | $V_{CC}$  | 8 V to 36 V     |
| Typ on-state resistance      | $R_{ON}$  | 6 m $\Omega$    |
| Current limitation (typ)     | $I_{LIM}$ | 115 A           |
| Off-state supply current     | $I_S$     | 2 $\mu A^{(1)}$ |

1. Typical value with all loads connected.

- AEC-Q100 qualified
- General
  - Very low standby current
  - 3 V CMOS compatible input
  - Optimized electromagnetic emission
  - Very low electromagnetic susceptibility
  - Compliance with 2002/95/EC European directive
  - Fault reset standby pin (FR\_Stby)
- Diagnostic functions
  - Proportional load current sense
  - Current sense precision for wide range currents
  - Off-state open-load detection
  - Output short to  $V_{CC}$  detection
  - Overload and short to ground latch-off
  - Thermal shutdown latch-off
  - Very low current sense leakage



- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of  $V_{CC}$
  - Thermal shutdown
  - Reverse battery protected with self switch of the PowerMOS
  - Electrostatic discharge protection

### Application

- All types of resistive, inductive and capacitive loads

### Description

The VN5T006ASP-E is a device made using STMicroelectronics® VIPower® technology, intended for driving resistive or inductive loads with one side connected to ground. Active  $V_{CC}$  pin voltage clamp protects the device against low energy spikes.

This device integrates an analog current sense which delivers a current proportional to the load current. Fault conditions such as overload, overtemperature or short to  $V_{CC}$  are reported via the current sense pin.

Output current limitation protects the device in overload condition. The device latches off in case of overload or thermal shutdown.

The device is reset by a low-level pass on the fault reset standby pin.

A permanent low level on the inputs and fault reset standby pin disables all outputs and sets the device in standby mode.

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Figure 2. Configuration diagram (top view)

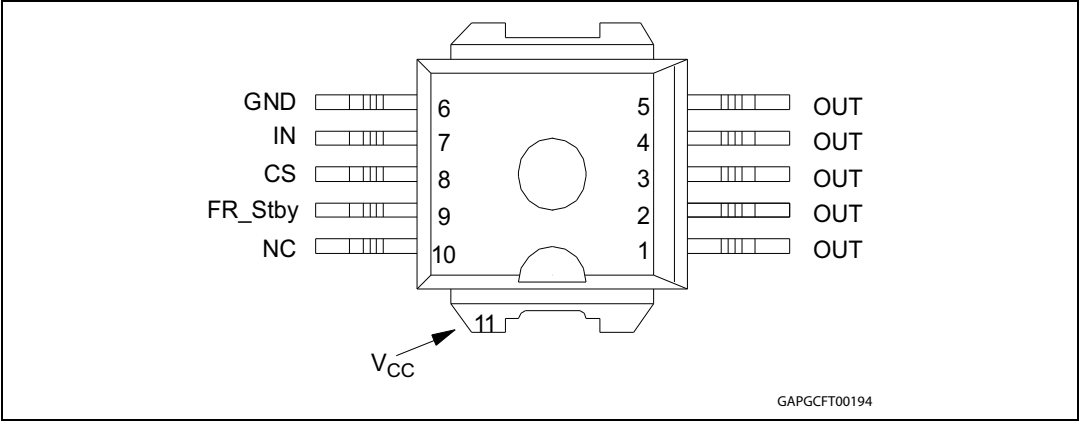


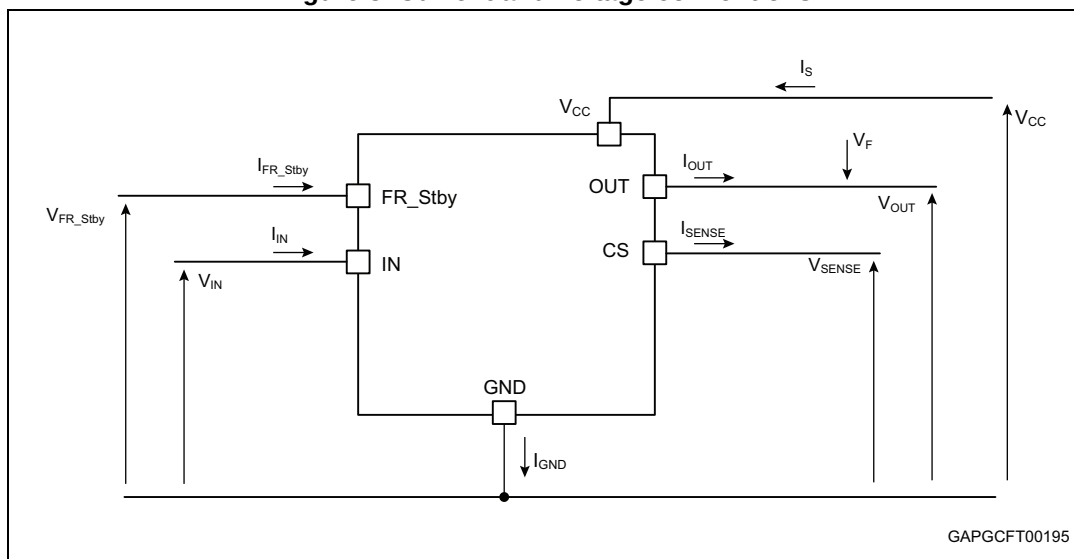
Table 2. Suggested connections for unused and not connected pins

| Connection / pin | CS                     | N.C.             | OUT         | IN                     | FR_Stby                |
|------------------|------------------------|------------------|-------------|------------------------|------------------------|
| Floating         | Not allowed            | X <sup>(1)</sup> | X           | X                      | X                      |
| To ground        | Through 10 KΩ resistor | X                | Not allowed | Through 10 KΩ resistor | Through 10 KΩ resistor |

1. X: do not care.

## 2 Electrical specifications

Figure 3. Current and voltage conventions



### 2.1 Absolute maximum ratings

Stressing the device above the ratings listed in [Table 3](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions reported in this section for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

| Symbol         | Parameter                                                                                                                                                        | Value                      | Unit          |
|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|---------------|
| $V_{CC}$       | DC supply voltage                                                                                                                                                | 58                         | V             |
| $-V_{CC}$      | Reverse DC supply voltage                                                                                                                                        | -32                        | V             |
| $I_{OUT}$      | DC output current                                                                                                                                                | Internally limited         | A             |
| $-I_{OUT}$     | Reverse DC output current                                                                                                                                        | 90                         | A             |
| $I_{IN}$       | DC input current                                                                                                                                                 | -1 to 10                   | mA            |
| $I_{FR\_Stby}$ | Fault reset standby DC input current                                                                                                                             | -1 to 1.5                  | mA            |
| $V_{CSENSE}$   | Current sense maximum voltage                                                                                                                                    | $V_{CC} - 58$ to $+V_{CC}$ | V             |
| $E_{MAX}$      | Maximum switching energy<br>( $L = 10$ mH; $V_{bat} = 32$ V; $T_{jstart} = 150^{\circ}\text{C}$ ; $I_{OUT} = 8.9$ A)                                             | 880                        | mJ            |
| $L_{SMAX}$     | Maximum stray inductance in short circuit condition<br>$V_{bat} = 32$ V; $R_L = 300$ m $\Omega$ ; $T_{jstart} = 150^{\circ}\text{C}$ ; $I_{OUT} = I_{limH\_max}$ | 40                         | $\mu\text{H}$ |

Table 3. Absolute maximum ratings (continued)

| Symbol           | Parameter                                                             | Value      | Unit |
|------------------|-----------------------------------------------------------------------|------------|------|
| V <sub>ESD</sub> | Electrostatic discharge<br>(human body model: R = 1.5 KΩ; C = 100 pF) |            |      |
|                  | – IN                                                                  | 4000       | V    |
|                  | – CS                                                                  | 2000       | V    |
|                  | – FR_Stby                                                             | 4000       | V    |
|                  | – OUT                                                                 | 5000       | V    |
|                  | – V <sub>CC</sub>                                                     | 5000       | V    |
| V <sub>ESD</sub> | Charge device model (CDM-AEC-Q100-011)                                | 750        | V    |
| T <sub>J</sub>   | Junction operating temperature                                        | -40 to 150 | °C   |
| T <sub>stg</sub> | Storage temperature                                                   | -55 to 150 | °C   |

## 2.2 Thermal data

Table 4. Thermal data

| Symbol                | Parameter                                                     | Value                         | Unit |
|-----------------------|---------------------------------------------------------------|-------------------------------|------|
| R <sub>thj-case</sub> | Thermal resistance junction-case (max.) (with one channel on) | 0.8                           | °C/W |
| R <sub>thj-amb</sub>  | Thermal resistance junction-ambient (max.)                    | See <a href="#">Figure 27</a> | °C/W |

## 2.3 Electrical characteristics

8 V < V<sub>CC</sub> < 36 V; -40°C < T<sub>j</sub> < 150°C, unless otherwise specified.

**Table 5. Power section**

| Symbol               | Parameter                           | Test conditions                                                                                                            | Min. | Typ.             | Max. | Unit |
|----------------------|-------------------------------------|----------------------------------------------------------------------------------------------------------------------------|------|------------------|------|------|
| V <sub>CC</sub>      | Operating supply voltage            |                                                                                                                            | 8    | 24               | 36   | V    |
| V <sub>USD</sub>     | Undervoltage shutdown               |                                                                                                                            |      | 3.5              | 5    | V    |
| V <sub>USDhyst</sub> | Undervoltage shutdown hysteresis    |                                                                                                                            |      | 0.5              |      | V    |
| R <sub>ON</sub>      | On-state resistance <sup>(2)</sup>  | I <sub>OUT</sub> = 10 A; T <sub>j</sub> = 25°C;<br>8 V < V <sub>CC</sub> < 36 V                                            |      | 6                |      | mΩ   |
|                      |                                     | I <sub>OUT</sub> = 10 A; T <sub>j</sub> = 150°C;<br>8 V < V <sub>CC</sub> < 36 V                                           |      |                  | 12   |      |
| R <sub>ON REV</sub>  | Reverse battery on-state resistance | V <sub>CC</sub> = -24 V; I <sub>OUT</sub> = -10 A;<br>T <sub>j</sub> = 25°C                                                |      |                  | 6    | mΩ   |
| V <sub>clamp</sub>   | Clamp voltage                       | I <sub>S</sub> = 20 mA                                                                                                     | 58   | 64               | 70   | V    |
| I <sub>S</sub>       | Supply current                      | Off-state: V <sub>CC</sub> = 24 V; T <sub>j</sub> = 25°C;<br>V <sub>IN</sub> = V <sub>OUT</sub> = V <sub>SENSE</sub> = 0 V |      | 2 <sup>(1)</sup> | 5    | μA   |
|                      |                                     | On-state: V <sub>CC</sub> = 24 V; V <sub>IN</sub> = 5 V;<br>I <sub>OUT</sub> = 0 A                                         |      | 3                | 6    | mA   |
| I <sub>L(off1)</sub> | Off-state output current            | V <sub>IN</sub> = V <sub>OUT</sub> = 0 V; V <sub>CC</sub> = 24 V;<br>T <sub>j</sub> = 25°C                                 | 0    | 0.01             | 3    | μA   |
|                      |                                     | V <sub>IN</sub> = V <sub>OUT</sub> = 0 V; V <sub>CC</sub> = 24 V;<br>T <sub>j</sub> = 125°C                                | 0    |                  | 5    |      |

1. PowerMOS leakage included.

**Table 6. Switching (V<sub>CC</sub> = 24 V; T<sub>j</sub> = 25°C)**

| Symbol                                 | Parameter                                        | Test conditions        | Min. | Typ. | Max. | Unit |
|----------------------------------------|--------------------------------------------------|------------------------|------|------|------|------|
| t <sub>d(on)</sub>                     | Turn-on delay time                               | R <sub>L</sub> = 2.4 Ω | —    | 32   | —    | μs   |
| t <sub>d(off)</sub>                    | Turn-off delay time                              | R <sub>L</sub> = 2.4 Ω | —    | 67   | —    | μs   |
| dV <sub>OUT</sub> /dt <sub>(on)</sub>  | Turn-on voltage slope                            | R <sub>L</sub> = 2.4 Ω | 0.7  |      |      | V/μs |
| dV <sub>OUT</sub> /dt <sub>(off)</sub> | Turn-off voltage slope                           | R <sub>L</sub> = 2.4 Ω | 0.46 |      |      | V/μs |
| W <sub>ON</sub>                        | Switching energy losses during t <sub>won</sub>  | R <sub>L</sub> = 2.4 Ω | —    | 4.15 | —    | mJ   |
| W <sub>OFF</sub>                       | Switching energy losses during t <sub>woff</sub> | R <sub>L</sub> = 2.4 Ω | —    | 2.7  | —    | mJ   |

Table 7. Logic inputs

| Symbol               | Parameter                              | Test conditions                       | Min. | Typ. | Max. | Unit          |
|----------------------|----------------------------------------|---------------------------------------|------|------|------|---------------|
| $V_{IL}$             | Low-level input voltage                |                                       |      |      | 0.9  | V             |
| $I_{IL}$             | Low-level input current                | $V_{IN} = 0.9\text{ V}$               | 1    |      |      | $\mu\text{A}$ |
| $V_{IH}$             | High-level input voltage               |                                       | 2.1  |      |      | V             |
| $I_{IH}$             | High-level input current               | $V_{IN} = 2.1\text{ V}$               |      |      | 10   | $\mu\text{A}$ |
| $V_{I(hyst)}$        | Input hysteresis voltage               |                                       | 0.25 |      |      | V             |
| $V_{ICL}$            | Input clamp voltage                    | $I_{IN} = 1\text{ mA}$                | 5.5  |      | 7    | V             |
|                      |                                        | $I_{IN} = -1\text{ mA}$               |      | -0.7 |      |               |
| $V_{FR\_Stby\_L}$    | Low-level fault-reset-standby voltage  |                                       |      |      | 0.9  | V             |
| $I_{FR\_Stby\_L}$    | Low-level fault-reset-standby current  | $V_{FR\_Stby} = 0.9\text{ V}$         | 1    |      |      | $\mu\text{A}$ |
| $V_{FR\_Stby\_H}$    | High-level fault-reset-standby voltage |                                       | 2.1  |      |      | V             |
| $I_{FR\_Stby\_H}$    | High-level fault-reset-standby current | $V_{FR\_Stby} = 2.1\text{ V}$         |      |      | 10   | $\mu\text{A}$ |
| $V_{FR\_Stby(hyst)}$ | Fault-reset-standby hysteresis voltage |                                       | 0.25 |      |      | V             |
| $V_{FR\_Stby\_CL}$   | Fault-reset-standby clamp voltage      | $I_{FR\_Stby} = 15\text{ mA (10 ms)}$ | 11   |      | 15   | V             |
|                      |                                        | $I_{FR\_Stby} = -1\text{ mA}$         |      | -0.7 |      |               |
| $t_{reset}$          | Overload latch-off reset time          | See <a href="#">Figure 4</a>          | 2    |      | 24   | $\mu\text{s}$ |
| $t_{stby}$           | Standby delay                          | See <a href="#">Figure 5</a>          | 120  |      | 1200 | $\mu\text{s}$ |

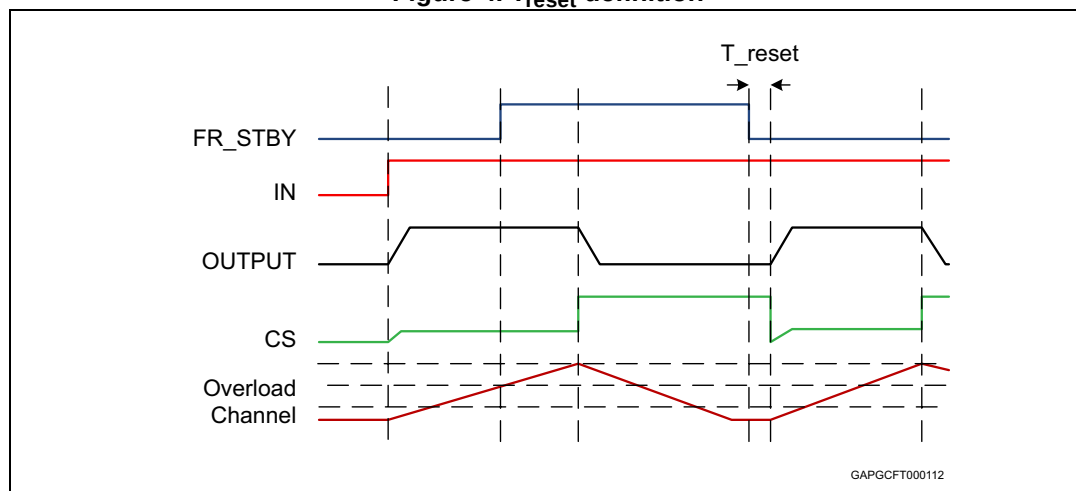
Figure 4.  $T_{reset}$  definition

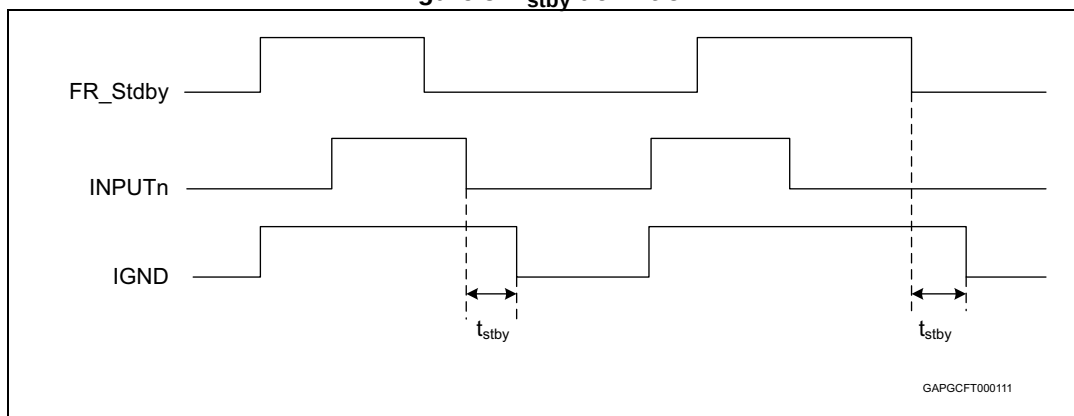
Figure 5.  $T_{stby}$  definition

Table 8. Protections and diagnostics

| Symbol      | Parameter                                    | Test conditions                                                       | Min.          | Typ.          | Max.          | Unit |
|-------------|----------------------------------------------|-----------------------------------------------------------------------|---------------|---------------|---------------|------|
| $I_{limH}$  | DC short-circuit current                     | $V_{CC} = 24\text{ V}$                                                | 81            | 115           | 162           | A    |
|             |                                              | $5\text{ V} < V_{CC} < 36\text{ V}$                                   |               |               | 162           | A    |
| $I_{limL}$  | Short-circuit current during thermal cycling | $V_{CC} = 24\text{ V}; T_R < T_j < T_{TSD}$                           |               | 29            |               | A    |
| $T_{TSD}$   | Shutdown temperature                         |                                                                       | 150           | 175           | 200           | °C   |
| $T_R$       | Reset temperature                            |                                                                       | $T_{RS} + 1$  | $T_{RS} + 5$  |               | °C   |
| $T_{RS}$    | Thermal reset of status                      |                                                                       | 135           |               |               | °C   |
| $T_{HYST}$  | Thermal hysteresis ( $T_{TSD} - T_R$ )       |                                                                       |               | 7             |               | °C   |
| $V_{DEMAG}$ | Turn-off output voltage clamp                | $I_{OUT} = 10\text{ A}; V_{IN} = 0\text{ V}; L = 6\text{ mH}$         | $V_{CC} - 58$ | $V_{CC} - 64$ | $V_{CC} - 70$ | V    |
| $V_{ON}$    | Output voltage drop limitation               | $I_{OUT} = 1\text{ A}; T_j = -40^\circ\text{C to } 150^\circ\text{C}$ |               | 25            |               | mV   |

Table 9. Current sense (8 V < V<sub>CC</sub> < 36 V)

| Symbol                                         | Parameter                            | Test conditions                                                                                                                 | Min.         | Typ.  | Max.           | Unit |
|------------------------------------------------|--------------------------------------|---------------------------------------------------------------------------------------------------------------------------------|--------------|-------|----------------|------|
| K <sub>0</sub>                                 | I <sub>OUT</sub> /I <sub>SENSE</sub> | I <sub>OUT</sub> = 0.6 A; V <sub>SENSE</sub> = 0.5 V;<br>T <sub>j</sub> = -40°C to 150°C<br>T <sub>j</sub> = 25°C to 150°C      | 3930<br>5035 | 11250 | 19850<br>17055 |      |
| dK <sub>0</sub> /K <sub>0</sub> <sup>(1)</sup> | Current sense ratio drift            | I <sub>OUT</sub> = 0.6 A; V <sub>SENSE</sub> = 0.5 V;<br>T <sub>j</sub> = -40°C to 150°C                                        | -30          |       | 30             | %    |
| K <sub>1</sub>                                 | I <sub>OUT</sub> /I <sub>SENSE</sub> | I <sub>OUT</sub> = 1.6 A; V <sub>SENSE</sub> = 1 V;<br>T <sub>j</sub> = -40°C to 150°C;<br>T <sub>j</sub> = 25°C to 150°C       | 5600<br>6215 | 10750 | 16940<br>14660 |      |
| dK <sub>1</sub> /K <sub>1</sub> <sup>(1)</sup> | Current sense ratio drift            | I <sub>OUT</sub> = 1.6 A; V <sub>SENSE</sub> = 1 V;<br>T <sub>j</sub> = -40°C to 150°C                                          | -28          |       | 25             | %    |
| K <sub>2</sub>                                 | I <sub>OUT</sub> /I <sub>SENSE</sub> | I <sub>OUT</sub> = 2.4 A; V <sub>SENSE</sub> = 1 V;<br>T <sub>j</sub> = -40°C to 150°C<br>T <sub>j</sub> = 25°C to 150°C        | 6030<br>6200 | 10370 | 15865<br>13635 |      |
| dK <sub>2</sub> /K <sub>2</sub> <sup>(1)</sup> | Current sense ratio drift            | I <sub>OUT</sub> = 2.4 A; V <sub>SENSE</sub> = 1 V;<br>T <sub>j</sub> = -40°C to 150°C                                          | -26          |       | 23             | %    |
| K <sub>3</sub>                                 | I <sub>OUT</sub> /I <sub>SENSE</sub> | I <sub>OUT</sub> = 3 A; V <sub>SENSE</sub> = 2 V;<br>T <sub>j</sub> = -40°C to 150°C<br>T <sub>j</sub> = 25°C to 150°C          | 6040<br>6040 | 10070 | 15285<br>13090 |      |
| dK <sub>3</sub> /K <sub>3</sub> <sup>(1)</sup> | Current sense ratio drift            | I <sub>OUT</sub> = 3 A; V <sub>SENSE</sub> = 2 V;<br>T <sub>j</sub> = -40°C to 150°C                                            | -25          |       | 22             | %    |
| K <sub>4</sub>                                 | I <sub>OUT</sub> /I <sub>SENSE</sub> | I <sub>OUT</sub> = 6 A; V <sub>SENSE</sub> = 4 V;<br>T <sub>j</sub> = -40°C to 150°C<br>T <sub>j</sub> = 25°C to 150°C          | 5845<br>6000 | 8670  | 13630<br>10895 |      |
| dK <sub>4</sub> /K <sub>4</sub> <sup>(1)</sup> | Current sense ratio drift            | I <sub>OUT</sub> = 6 A; V <sub>SENSE</sub> = 4 V;<br>T <sub>j</sub> = -40°C to 150°C                                            | -20          |       | 20             | %    |
| K <sub>5</sub>                                 | I <sub>OUT</sub> /I <sub>SENSE</sub> | I <sub>OUT</sub> = 10 A; V <sub>SENSE</sub> = 4 V;<br>T <sub>j</sub> = -40°C to 150°C<br>T <sub>j</sub> = 25°C to 150°C         | 5920<br>6730 | 8400  | 11520<br>9765  |      |
| dK <sub>5</sub> /K <sub>5</sub> <sup>(1)</sup> | Current sense ratio drift            | I <sub>OUT</sub> = 10 A; V <sub>SENSE</sub> = 4 V;<br>T <sub>j</sub> = -40°C to 150°C                                           | -15          |       | 15             | %    |
| K <sub>6</sub>                                 | I <sub>OUT</sub> /I <sub>SENSE</sub> | I <sub>OUT</sub> = 20 A; V <sub>SENSE</sub> = 4 V;<br>T <sub>j</sub> = -40°C to 150°C                                           | 6960         | 8330  | 10090          |      |
| dK <sub>6</sub> /K <sub>6</sub> <sup>(1)</sup> | Current sense ratio drift            | I <sub>OUT</sub> = 20 A; V <sub>SENSE</sub> = 4 V;<br>T <sub>j</sub> = -40°C to 150°C                                           | -8           |       | 8              | %    |
| dK/K <sub>BULB1</sub> <sup>(1)</sup>           | Current sense ratio drift            | I <sub>OUT</sub> = 0.6 A to 6 A; I <sub>CAL</sub> = 3 A;<br>V <sub>SENSE</sub> = 0.5 V;<br>T <sub>j</sub> = -40°C to 150°C      | -30          |       | 50             | %    |
| dK/K <sub>BULB2</sub> <sup>(1)</sup>           | Current sense ratio drift            | I <sub>OUT</sub> = 1.6 A to 4.2 A;<br>I <sub>OUTCAL</sub> = 3 A; V <sub>SENSE</sub> = 2 V;<br>T <sub>j</sub> = -40°C to 150°C   | -30          |       | 26             | %    |
| dK/K <sub>BULB3</sub> <sup>(1)</sup>           | Current sense ratio drift            | I <sub>OUT</sub> = 0.6 A to 2.4 A;<br>I <sub>OUTCAL</sub> = 1.6 A; V <sub>SENSE</sub> = 2 V;<br>T <sub>j</sub> = -40°C to 150°C | -27          |       | 25             | %    |

Table 9. Current sense (8 V < V<sub>CC</sub> < 36 V) (continued)

| Symbol                 | Parameter                                                                                  | Test conditions                                                                                                                                                                                  | Min. | Typ. | Max. | Unit |
|------------------------|--------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| I <sub>SENSE0</sub>    | Analog sense leakage current                                                               | I <sub>OUT</sub> = 0 A; V <sub>SENSE</sub> = 0 V;<br>V <sub>IN</sub> = 0 V; T <sub>j</sub> = -40°C to 150°C                                                                                      | 0    |      | 1    | μA   |
|                        |                                                                                            | I <sub>OUT</sub> = 0 A; V <sub>SENSE</sub> = 0 V;<br>V <sub>IN</sub> = 5 V; T <sub>j</sub> = -40°C to 150°C                                                                                      | 0    |      | 2    |      |
| V <sub>SENSE</sub>     | Max analog sense output voltage                                                            | I <sub>OUT</sub> = 40 A; R <sub>SENSE</sub> = 3.9 KΩ                                                                                                                                             | 5    |      |      | V    |
| V <sub>SENSEH</sub>    | Analog sense output voltage in fault condition <sup>(2)</sup>                              | V <sub>CC</sub> = 24 V; R <sub>SENSE</sub> = 3.9 KΩ                                                                                                                                              |      | 8    |      | V    |
| I <sub>SENSEH</sub>    | Analog sense output current in fault condition <sup>(2)</sup>                              | V <sub>CC</sub> = 24 V; V <sub>SENSE</sub> = 5 V                                                                                                                                                 |      | 9    | 12   | mA   |
| t <sub>DSENSE2H</sub>  | Delay response time from rising edge of IN pin                                             | V <sub>SENSE</sub> < 4 V; 1 A < I <sub>OUT</sub> < 40 A;<br>I <sub>SENSE</sub> = 90% of I <sub>SENSEMAX</sub><br>(see <a href="#">Figure 7</a> )                                                 |      | 300  | 600  | μs   |
| Δt <sub>DSENSE2H</sub> | Delay response time between rising edge of output current and rising edge of current sense | V <sub>SENSE</sub> < 4 V;<br>I <sub>SENSE</sub> = 90% of I <sub>SENSEMAX</sub> ,<br>I <sub>OUT</sub> = 90% of I <sub>OUTMAX</sub><br>I <sub>OUTMAX</sub> = 10 A (see <a href="#">Figure 10</a> ) |      |      | 450  | μs   |
| t <sub>DSENSE2L</sub>  | Delay response time from falling edge of IN pin                                            | V <sub>SENSE</sub> < 4 V; 1 A < I <sub>OUT</sub> < 40 A;<br>I <sub>SENSE</sub> = 10 % of I <sub>SENSEMAX</sub><br>(see <a href="#">Figure 7</a> )                                                |      | 5    | 20   | μs   |

1. Parameter guaranteed by design; it is not tested.
2. Fault condition includes: power limitation, overtemperature and open-load in OFF-state condition.

Table 10. Open-load detection (FR\_Stby = 5 V)

| Symbol               | Parameter                                                           | Test conditions                                                                             | Min. | Typ. | Max. | Unit |
|----------------------|---------------------------------------------------------------------|---------------------------------------------------------------------------------------------|------|------|------|------|
| V <sub>OL</sub>      | Open-load Off-state voltage detection threshold                     | V <sub>IN</sub> = 0 V; 8 V < V <sub>CC</sub> < 36 V                                         | 2    |      | 4    | V    |
| t <sub>DSTKON</sub>  | Output short-circuit to V <sub>CC</sub> detection delay at turn-off | See <a href="#">Figure 8</a>                                                                | 180  |      | 1800 | μs   |
| I <sub>L(off2)</sub> | Off-state output current at V <sub>OUT</sub> = 4 V                  | V <sub>IN</sub> = 0 V; V <sub>SENSE</sub> = 0 V;<br>V <sub>OUT</sub> rising from 0 V to 4 V | -120 |      | 0    | μA   |

Table 10. Open-load detection (FR\_Stby = 5 V) (continued)

| Symbol           | Parameter                                                                      | Test conditions                                                                        | Min. | Typ. | Max. | Unit          |
|------------------|--------------------------------------------------------------------------------|----------------------------------------------------------------------------------------|------|------|------|---------------|
| $t_{d\_vol}$     | Delay response from output rising edge to $V_{SENSE}$ rising edge in open-load | $V_{OUT} = 4\text{ V}$ ; $V_{IN} = 0\text{ V}$ ;<br>$V_{SENSE} = 90\%$ of $V_{SENSEH}$ |      |      | 20   | $\mu\text{s}$ |
| $t_{DFRSTK\_ON}$ | Output short circuit to $V_{CC}$ detection delay at $FR_{STBY}$ activation     | See Figure 6; Input <sub>1,2</sub> = low                                               |      |      | 50   | $\mu\text{s}$ |

Figure 6. Output stuck to  $V_{CC}$  detection delay time at  $FR_{STBY}$  activation

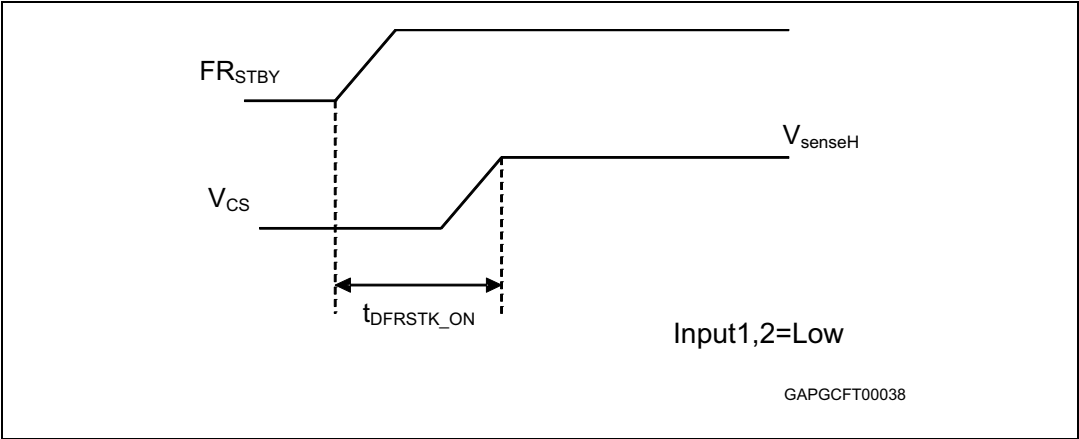


Figure 7. Current sense delay characteristics

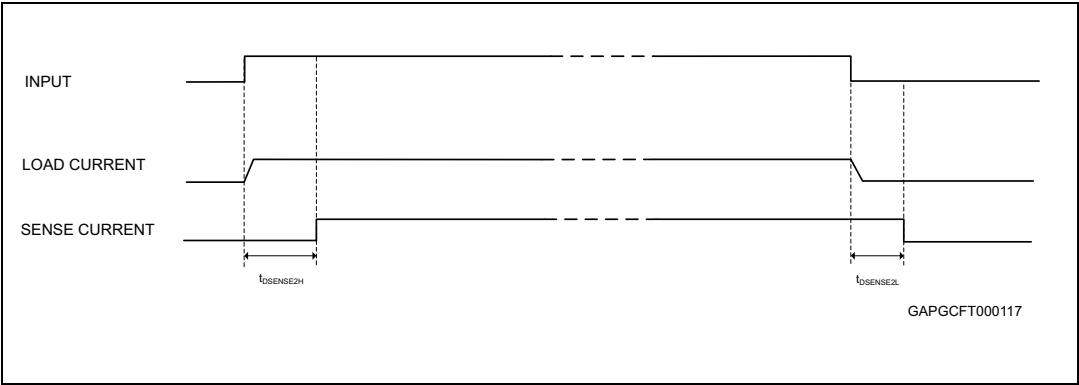


Figure 8. Open-load off-state delay timing

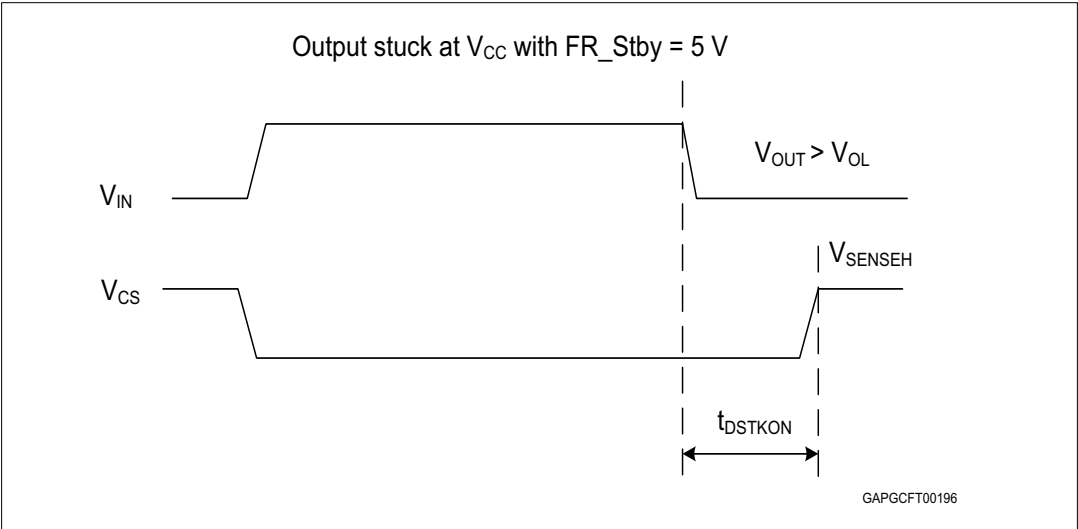


Figure 9. Switching characteristics

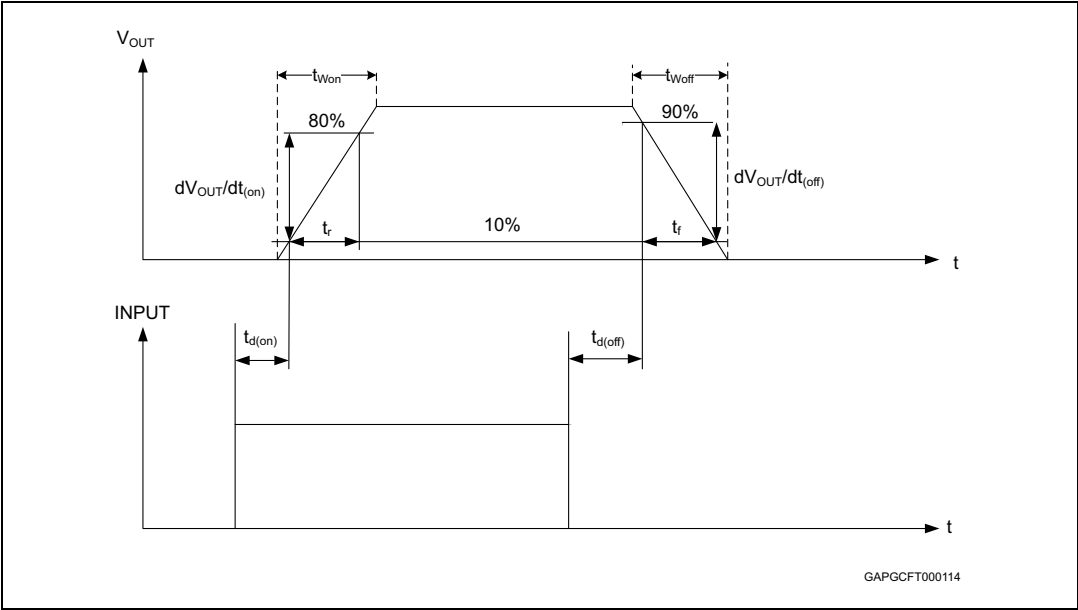


Figure 10. Delay response time between rising edge of output current and rising edge of current sense

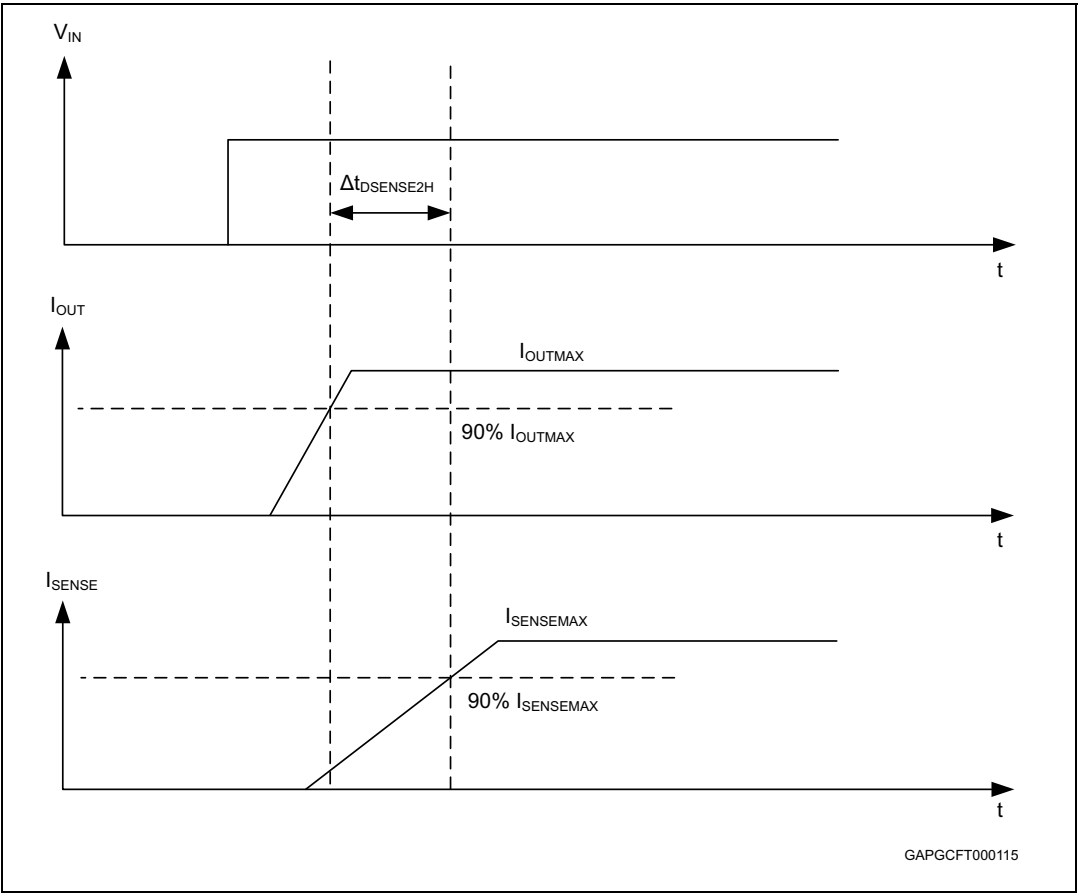


Figure 11. Output voltage drop limitation

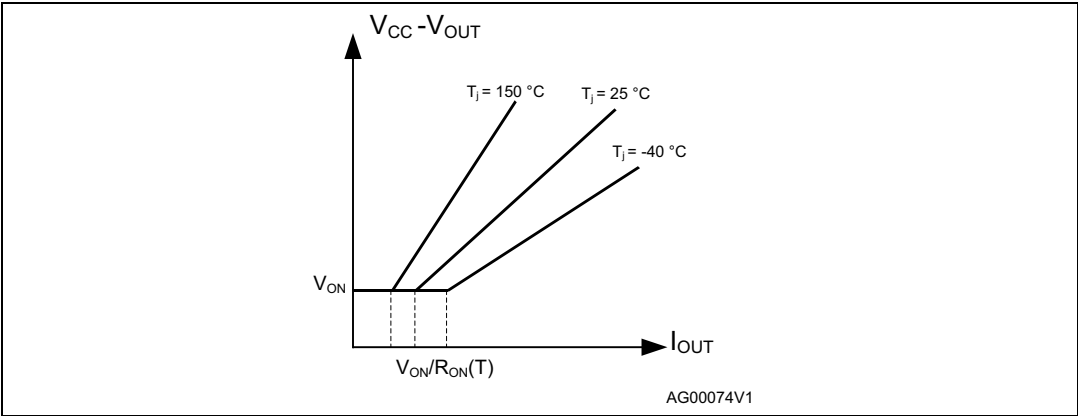


Figure 12. Device behavior in overload condition

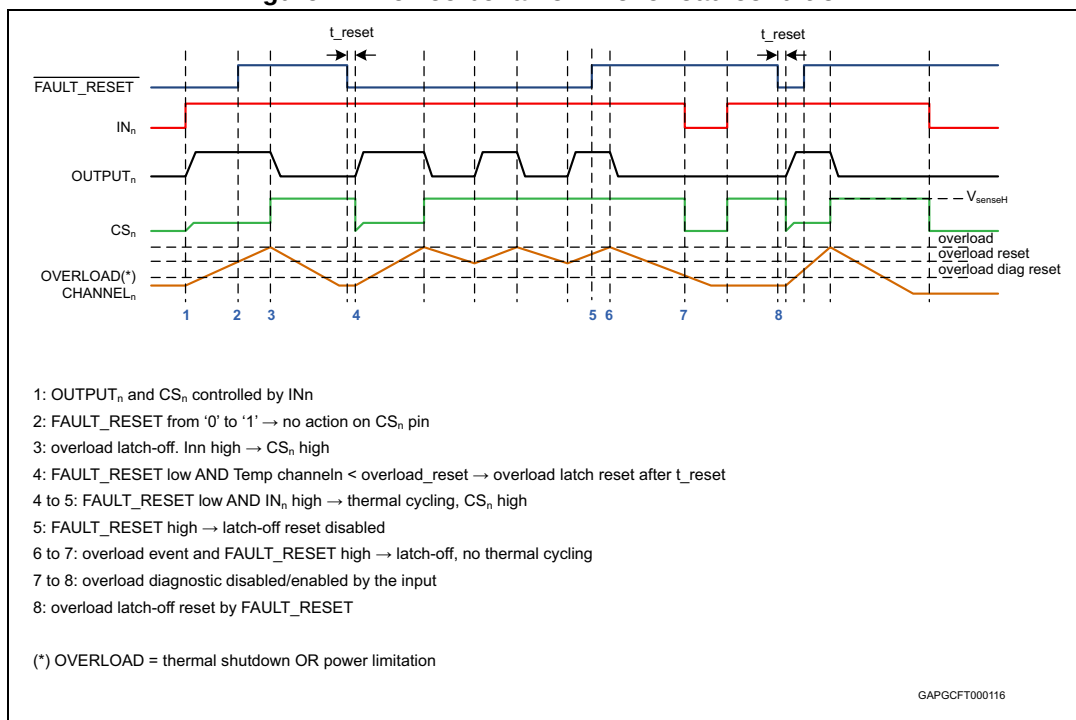


Table 11. Truth table

| Conditions                         | Fault reset standby | Input | Output   | Sense               |
|------------------------------------|---------------------|-------|----------|---------------------|
| Standby                            | L                   | L     | X        | 0                   |
| Normal operation                   | X                   | L     | L        | 0                   |
|                                    | X                   | H     | H        | Nominal             |
| Overload                           | X                   | L     | L        | 0                   |
|                                    | X                   | H     | H        | > Nominal           |
| Overtemperature / short to ground  | X                   | L     | L        | 0                   |
|                                    | L                   | H     | Cycling  | V <sub>SENSEH</sub> |
|                                    | H                   | H     | Latched  | V <sub>SENSEH</sub> |
| Undervoltage                       | X                   | X     | L        | 0                   |
| Short to V <sub>BAT</sub>          | L                   | L     | H        | 0                   |
|                                    | H                   | L     | H        | V <sub>SENSEH</sub> |
|                                    | X                   | H     | H        | < Nominal           |
| Open-load Off-state (with pull-up) | L                   | L     | H        | 0                   |
|                                    | H                   | L     | H        | V <sub>SENSEH</sub> |
|                                    | X                   | H     | H        | 0                   |
| Negative output voltage clamp      | X                   | L     | Negative | 0                   |

**Table 12. Electrical transient requirements (part 1)**

| ISO 7637-2:<br>2004(E)<br>Test pulse | Test levels <sup>(1)</sup> |         | Number of<br>pulses or<br>test times | Burst cycle/pulse<br>repetition time |        | Delays and<br>impedance  |
|--------------------------------------|----------------------------|---------|--------------------------------------|--------------------------------------|--------|--------------------------|
|                                      | III                        | IV      |                                      |                                      |        |                          |
| 1                                    | - 450 V                    | - 600 V | 5000<br>pulses                       | 0.5 s                                | 5 s    | 1 ms, 50 $\Omega$        |
| 2a                                   | + 37 V                     | + 50 V  | 5000<br>pulses                       | 0.2 s                                | 5 s    | 50 $\mu$ s, 2 $\Omega$   |
| 3a                                   | - 150 V                    | - 200 V | 1h                                   | 90 ms                                | 100 ms | 0.1 $\mu$ s, 50 $\Omega$ |
| 3b                                   | + 150 V                    | + 200 V | 1h                                   | 90 ms                                | 100 ms | 0.1 $\mu$ s, 50 $\Omega$ |
| 4                                    | - 12 V                     | - 16 V  | 1 pulse                              |                                      |        | 100 ms, 0.01 $\Omega$    |
| 5b <sup>(2)</sup>                    | + 123 V                    | + 174 V | 1 pulse                              |                                      |        | 350 ms, 1 $\Omega$       |

1. The above test levels must be considered referred to  $V_{CC} = 24.5V$  except for pulse 5b

2. Valid in case of external load dump clamp: 58V maximum referred to ground.

**Table 13. Electrical transient requirements (part 2)**

| ISO 7637-2:<br>2004(E)<br>Test pulse | Test level results |                  |
|--------------------------------------|--------------------|------------------|
|                                      | III                | IV               |
| 1                                    | C                  | C <sup>(1)</sup> |
| 2a                                   | C                  | C                |
| 3a                                   | C                  | C                |
| 3b <sup>(2)</sup>                    | E                  | E                |
| 3b <sup>(3)</sup>                    | C                  | C                |
| 4                                    | C                  | C                |
| 5b <sup>(4)</sup>                    | C                  | C                |

1. With  $R_{LOAD} < 24 \Omega$ .

2. Without capacitor between  $V_{CC}$  and GND.

3. With 10 nF between  $V_{CC}$  and GND.

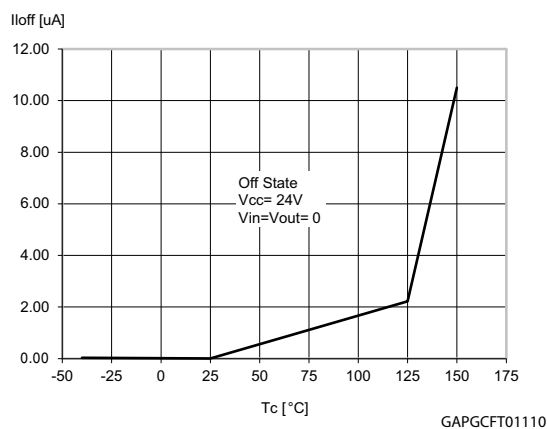
4. External load dump clamp: 58 V maximum, referred to ground.

**Table 14. Electrical transient requirements (part 3)**

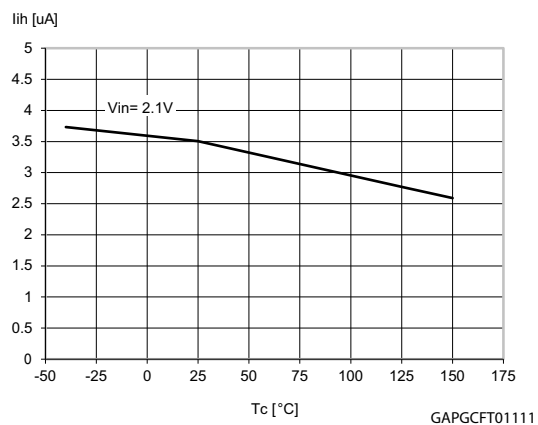
| Class | Contents                                                                                                                                                                 |
|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| C     | All functions of the device are performed as designed after exposure to disturbance.                                                                                     |
| E     | One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device. |

## 2.4 Electrical characteristics curves

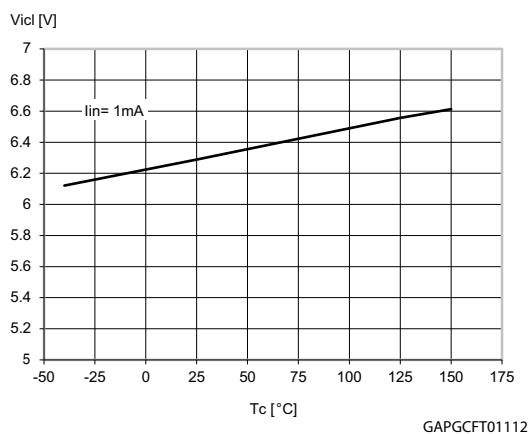
**Figure 13. Off-state output current**



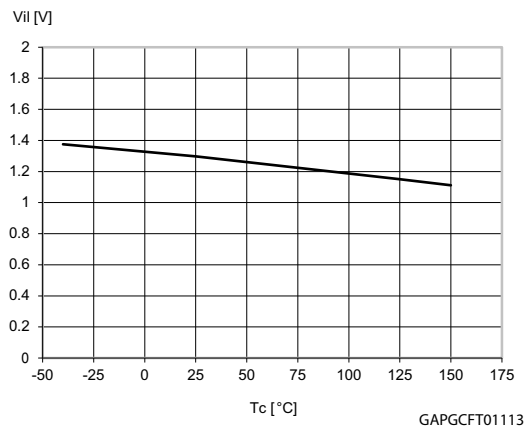
**Figure 14. High level input current**



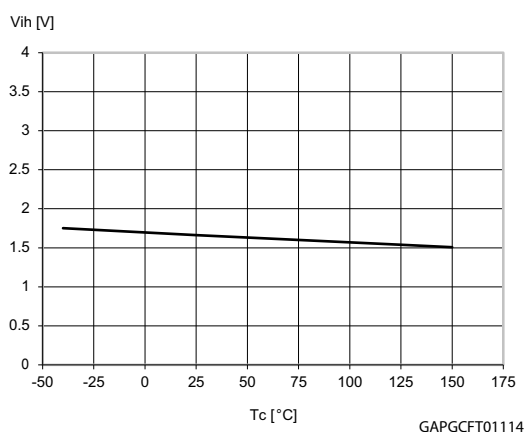
**Figure 15. Input clamp voltage**



**Figure 16. Input low level voltage**



**Figure 17. Input high level voltage**



**Figure 18. Input hysteresis voltage**

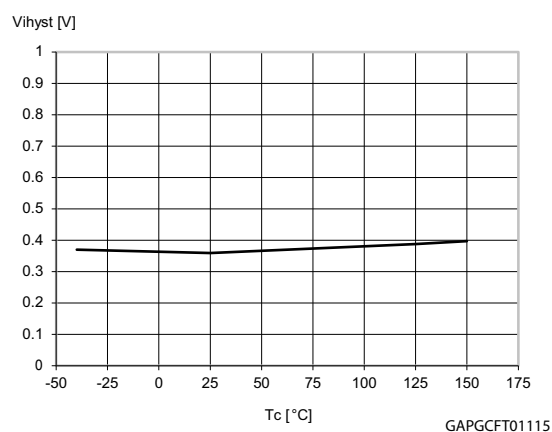


Figure 19. On state resistance vs  $T_{case}$

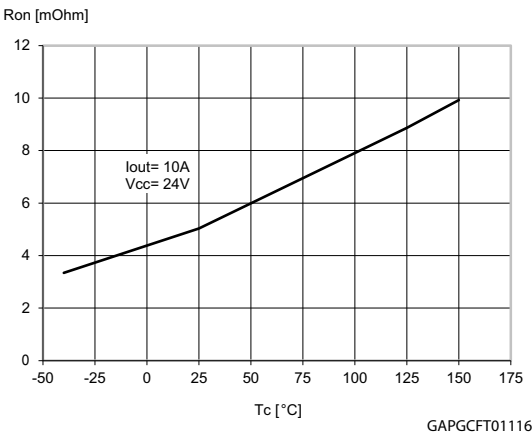


Figure 20. On state resistance vs  $V_{CC}$

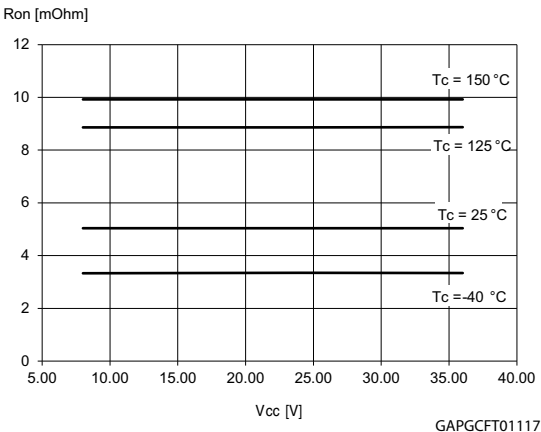


Figure 21.  $I_{LIMH}$  vs  $T_{case}$

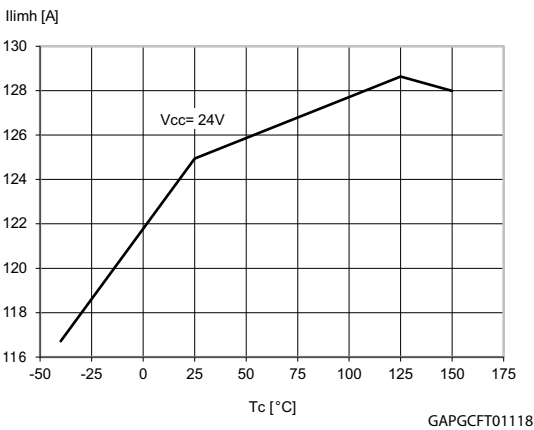


Figure 22. Turn-On voltage slope

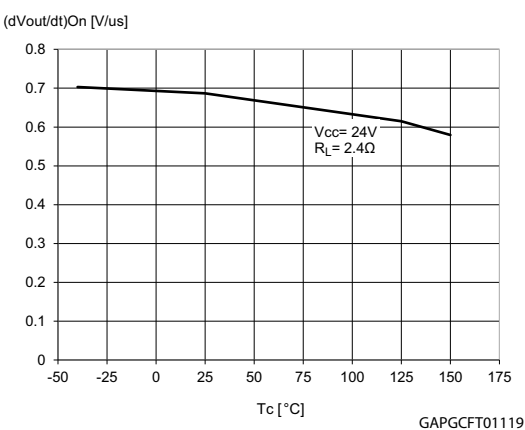
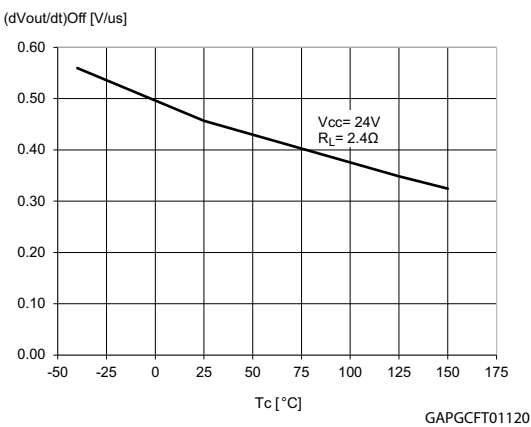
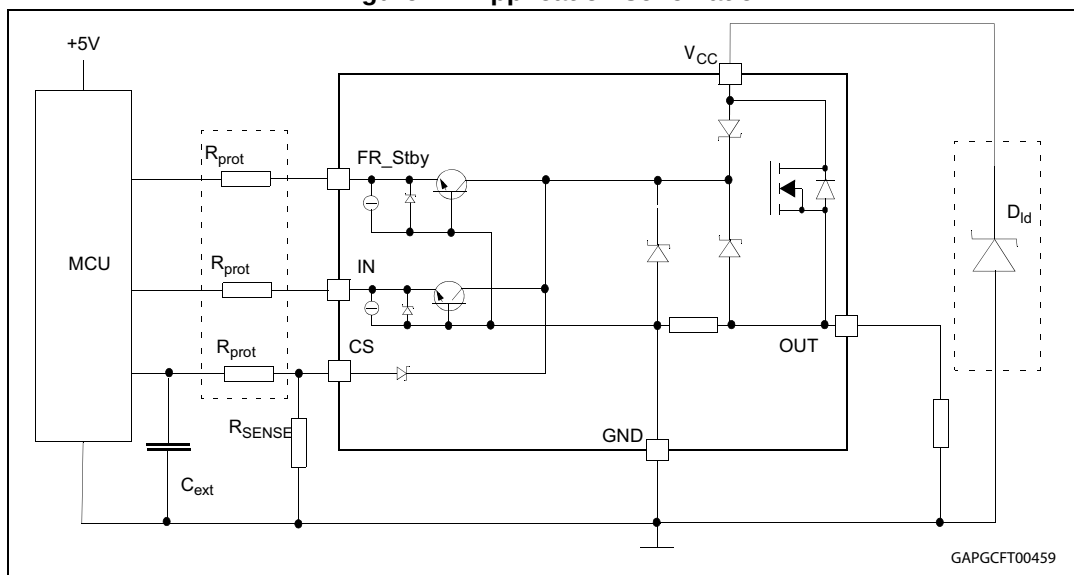


Figure 23. Turn-Off voltage slope



### 3 Application information

**Figure 24. Application schematic**



### 3.1 Load dump protection

D<sub>ld</sub> is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V<sub>CC</sub> max DC rating. The same applies if the device is subject to transients on the V<sub>CC</sub> line that are greater than the ones shown in the ISO 7637-2 2004 (E) table.

### 3.2 MCU I/Os protection

When negative transients are present on the  $V_{CC}$  line, the control pins is pulled negative. ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the microcontroller I/O pins from latching-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (input levels compatibility) with the latch-up limit of microcontroller I/Os.

### Equation 1

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH}) / I_{IHmax}$$

Calculation example:

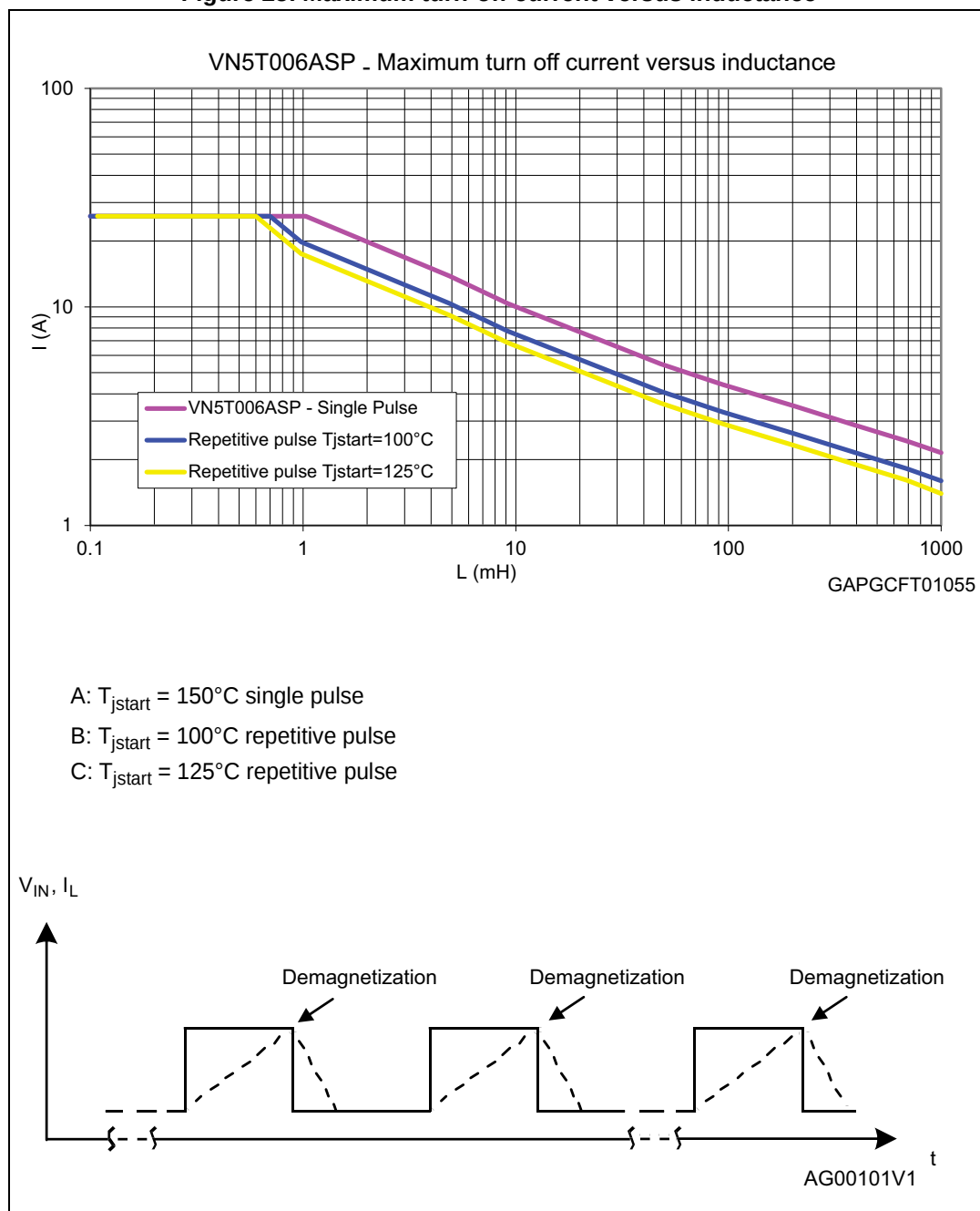
For  $V_{CCpeak} = -600$  V and  $I_{latchup} \geq 20$  mA;  $V_{OH\mu C} \geq 4.5$  V

$$30 \text{ K}\Omega \leq R_{\text{prot}} \leq 190 \text{ k}\Omega.$$

Recommended value:  $R_{\text{prot}} = 56 \text{ k}\Omega$

### 3.3 Maximum demagnetization energy ( $V_{CC} = 24\text{ V}$ )

Figure 25. Maximum turn-off current versus inductance



Note:

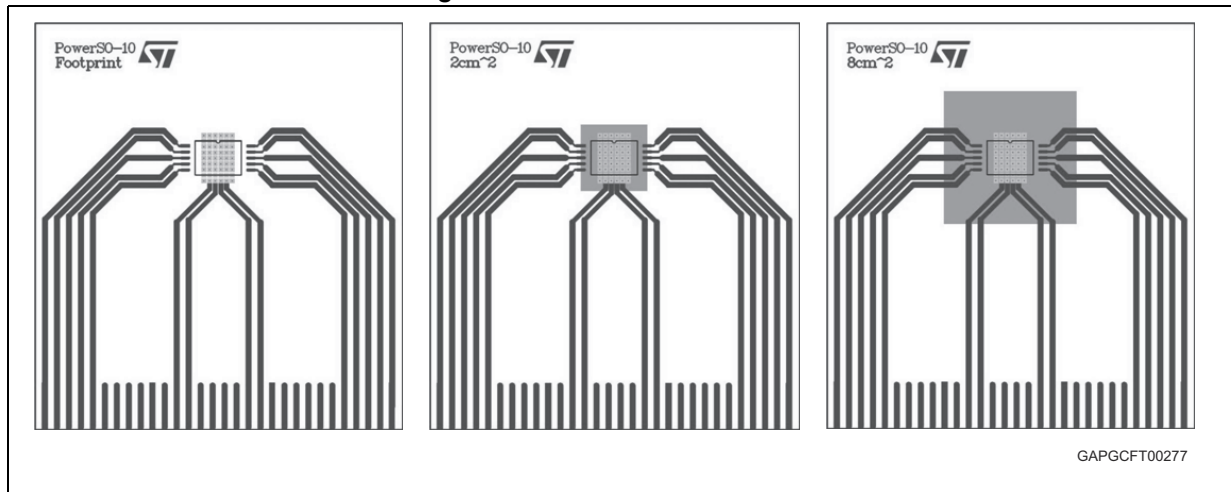
Values are generated with  $R_L = 0\ \Omega$

In case of repetitive pulses,  $T_{jstart}$  (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

## 4 Package and PCB thermal data

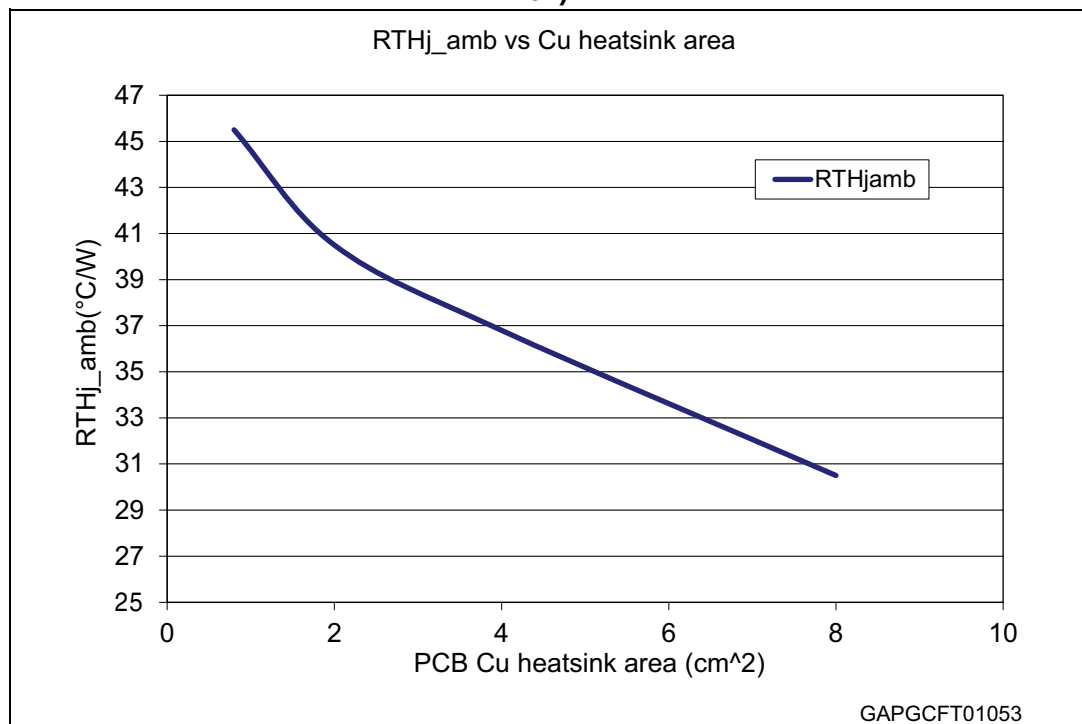
### 4.1 PowerSO-10 thermal data

Figure 26. PowerSO-10 PC board

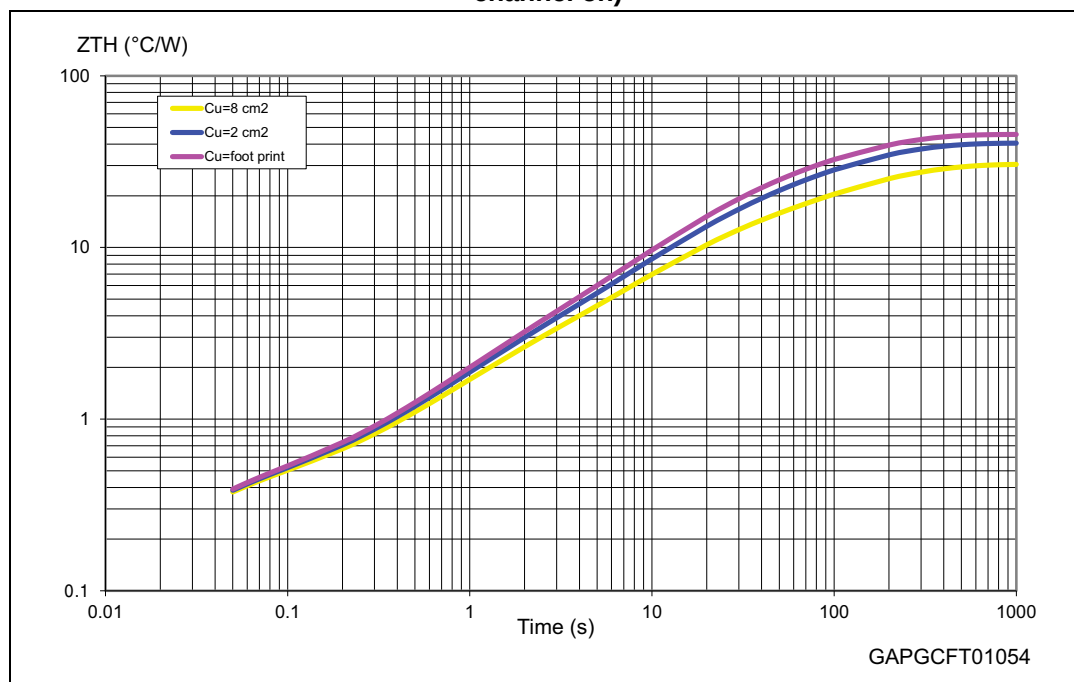


1. Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (Board finish thickness 1.6 mm  $\pm$  10%; Board double layer; Board dimension 77 x 86; Board Material FR4; Cu thickness 0.070 mm (front and back side); Thermal vias separation 1.2 mm; Thermal via diameter 0.3 mm  $\pm$  0.08 mm; Cu thickness on vias 0.025 mm).

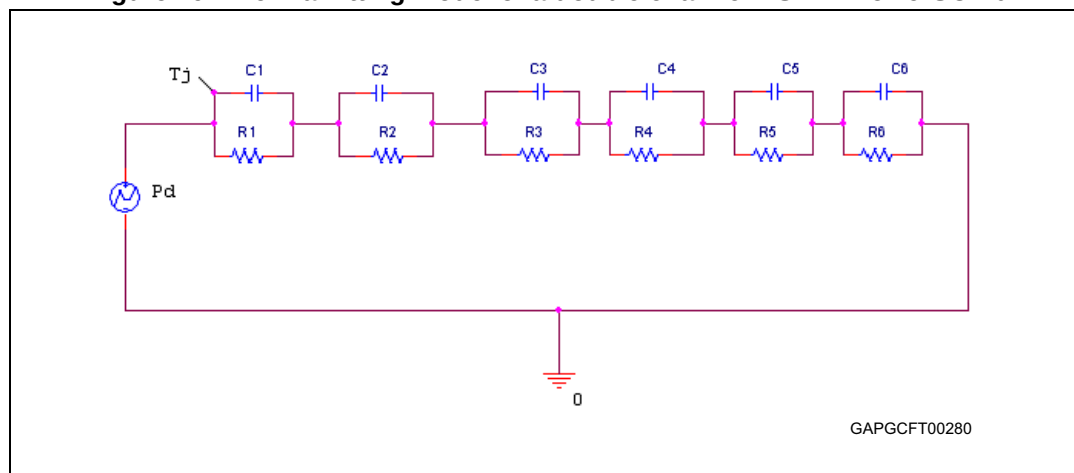
Figure 27.  $R_{thj-amb}$  vs PCB copper area in open box free air condition (one channel on)



**Figure 28. PowerSO-10 thermal impedance junction ambient single pulse (one channel on)**



**Figure 29. Thermal fitting model of a double channel HSD in PowerSO-10**



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

#### Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Table 15. Thermal parameters

| Area/island (cm <sup>2</sup> ) | Footprint | 2  | 8  |
|--------------------------------|-----------|----|----|
| R1 (°C/W)                      | 0.05      |    |    |
| R2 (°C/W)                      | 0.3       |    |    |
| R3 (°C/W)                      | 1.2       |    |    |
| R4 (°C/W)                      | 7         |    |    |
| R5 (°C/W)                      | 13        | 12 | 8  |
| R6 (°C/W)                      | 24        | 20 | 14 |
| C1 (W.s/°C)                    | 0.05      |    |    |
| C2 (W.s/°C)                    | 0.1       |    |    |
| C3 (W.s/°C)                    | 1         |    |    |
| C4 (W.s/°C)                    | 2         |    |    |
| C5 (W.s/°C)                    | 3         | 4  | 8  |
| C6 (W.s/°C)                    | 6         | 8  | 14 |

## 5 Package information

### 5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 5.2 PowerSO-10 mechanical data

Figure 30. PowerSO-10 package dimensions

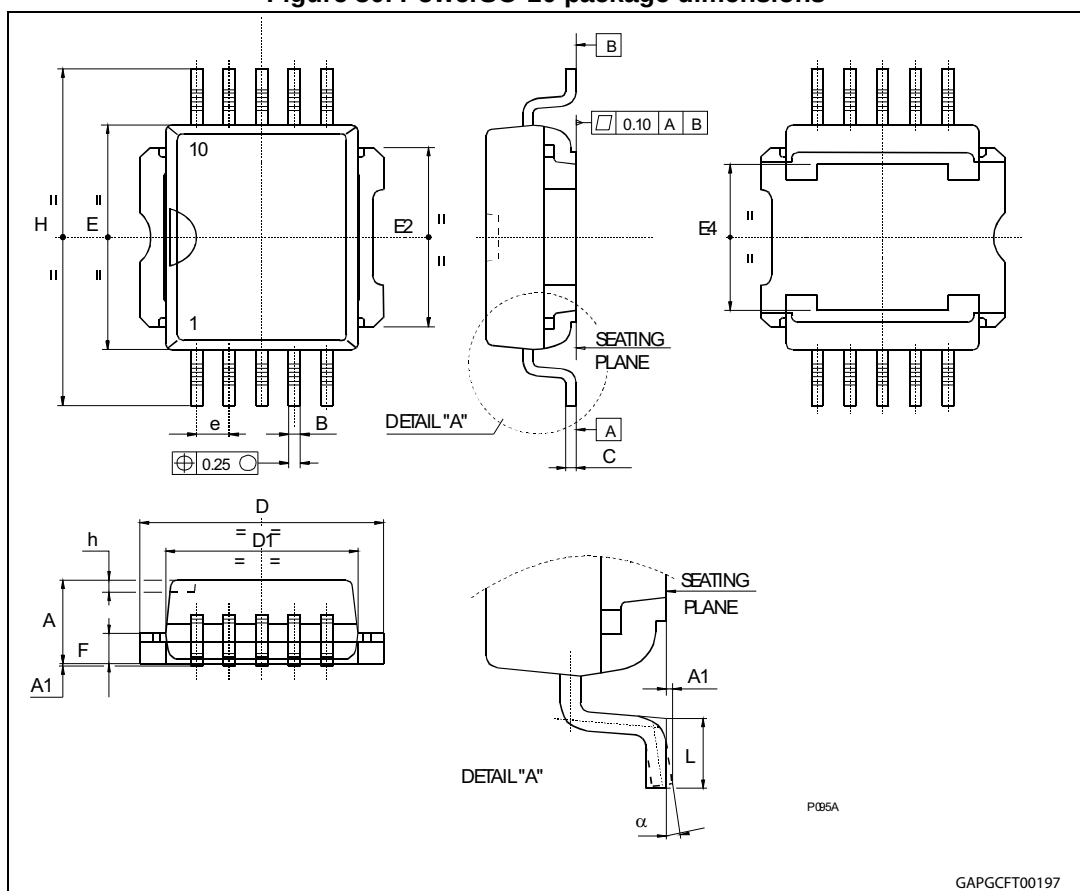


Table 16. PowerSO-10 mechanical data

| Symbol            | Millimeters |      |       |
|-------------------|-------------|------|-------|
|                   | Min.        | Typ. | Max.  |
| A                 | 3.35        |      | 3.65  |
| A <sup>(1)</sup>  | 3.4         |      | 3.6   |
| A1                | 0.00        |      | 0.10  |
| B                 | 0.40        |      | 0.60  |
| B <sup>(1)</sup>  | 0.37        |      | 0.53  |
| C                 | 0.35        |      | 0.55  |
| C <sup>(1)</sup>  | 0.23        |      | 0.32  |
| D                 | 9.40        |      | 9.60  |
| D1                | 7.40        |      | 7.60  |
| E                 | 9.30        |      | 9.50  |
| E2                | 7.20        |      | 7.60  |
| E2 <sup>(1)</sup> | 7.30        |      | 7.50  |
| E4                | 5.90        |      | 6.10  |
| E4 <sup>(1)</sup> | 5.90        |      | 6.30  |
| e                 |             | 1.27 |       |
| F                 | 1.25        |      | 1.35  |
| F <sup>(1)</sup>  | 1.20        |      | 1.40  |
| H                 | 13.80       |      | 14.40 |
| H <sup>(1)</sup>  | 13.85       |      | 14.35 |
| h                 |             | 0.50 |       |
| L                 | 1.20        |      | 1.80  |
| L <sup>(1)</sup>  | 0.80        |      | 1.10  |
| α                 | 0°          |      | 8°    |
| α <sup>(1)</sup>  | 2°          |      | 8°    |

1. Muar only POA P013P.

## 5.3 Packing information

Figure 31. PowerSO-10 suggested pad layout and tube shipment (no suffix)

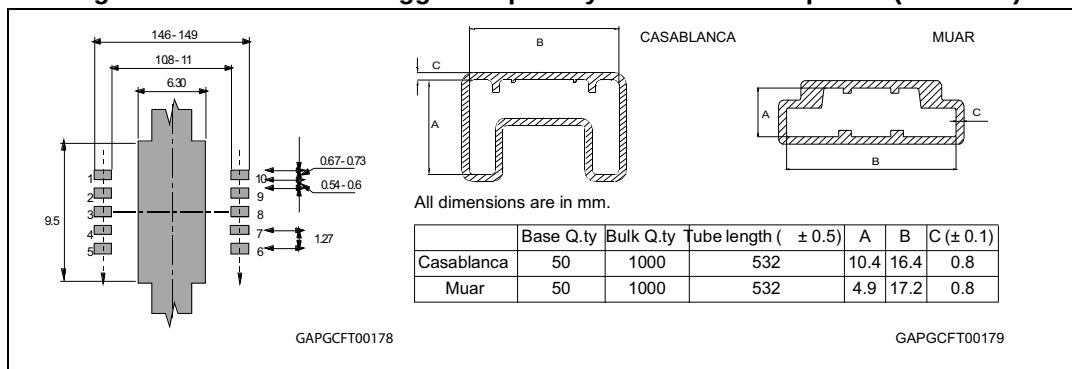
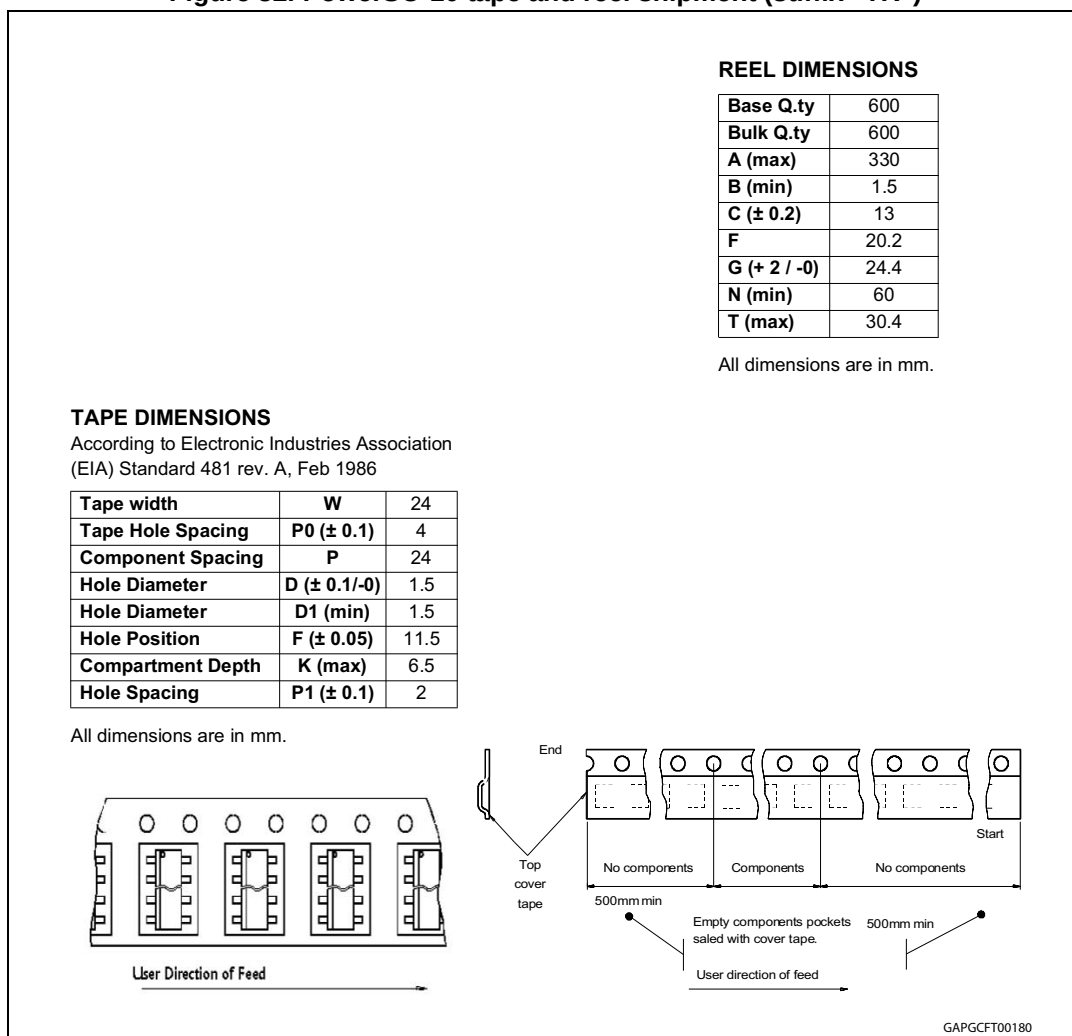


Figure 32. PowerSO-10 tape and reel shipment (suffix "TR")



## 6 Order codes

**Table 17. Device summary**

| Package    | Order codes  |                |
|------------|--------------|----------------|
|            | Tube         | Tape and reel  |
| PowerSO-10 | VN5T006ASP-E | VN5T006ASPTR-E |

## 7 Revision history

**Table 18. Document revision history**

| Date        | Revision | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19-Dec-2012 | 1        | Initial release.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 16-Jan-2013 | 2        | Updated <a href="#">Figure 3: Current and voltage conventions</a><br><a href="#">Table 6: Switching (<math>V_{CC} = 24\text{ V}</math>; <math>T_j = 25^\circ\text{C}</math>)</a> :<br>– $dV_{OUT}/dt_{(on)}$ : updated values<br><a href="#">Table 9: Current sense (<math>8\text{ V} &lt; V_{CC} &lt; 36\text{ V}</math>)</a> :<br>– $I_{OL}$ : removed row<br>– $dK/K_{BULB2}$ , $dK/K_{BULB2}$ : updated test conditions<br>Updated <a href="#">Table 22: Turn-On voltage slope</a> and <a href="#">Table 23: Turn-Off voltage slope</a> |
| 16-Jun-2013 | 3        | Changed document status from “preliminary data” to “production data”                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 17-Sep-2013 | 4        | Updated disclaimer.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 11-Apr-2016 | 5        | Added AEC-Q101 qualified in <a href="#">Features</a> section<br><a href="#">Table 9: Current sense (<math>8\text{ V} &lt; V_{CC} &lt; 36\text{ V}</math>)</a> :<br>– $dK_6/K_6$ : updated test conditions                                                                                                                                                                                                                                                                                                                                   |

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