TPS27S100x 40-V, 4-A, 80-mΩ Single-Channel High-Side Switch

1 Features

- 80-mΩ Single-channel High-side switch with full diagnostics
  - TPS27S100A: Open-drain status output
  - TPS27S100B: Current monitor analog output
- Wide operating voltage 3.5 V to 40 V
- Very-low standby current, <0.5 µA
- Operating junction temperature, –40 to 150°C
- Input control, 3.3-V and 5-V logic compatible
- High-accuracy current monitor, ±30 mA at 1 A
- Adjustable current limit (0.5-A to 6-A) with external resistor, ±20% at 0.5 A
- Diagnostic enable function for multiplexing of MCU, analog or digital interface
- Excellent ESD protection on IN and OUT pins
  - ±16 kV IEC 61000-4-2 ESD contact discharge
  - ±4 kV IEC 61000-4-4 Electrical fast transient
  - ±1.0 kV/42 Ω IEC 61000-4-5 Surge
- Protection
  - Overload and short-circuit-to-GND protection
  - Inductive load negative voltage clamp
  - Undervoltage lockout (UVLO) protection
  - Thermal shutdown and swing with self recovery
  - Loss of GND protection
- Diagnostic
  - On- and Off-State output Open-Load / short to supply detection
  - Overload and short to ground detection
  - Thermal shutdown and swing detection
- Thermally-Enhanced 14-Pin PWP or 16-Pin QFN package

2 Applications

- Programmable logic controller
- Building automation
- Telecom/networks

3 Description

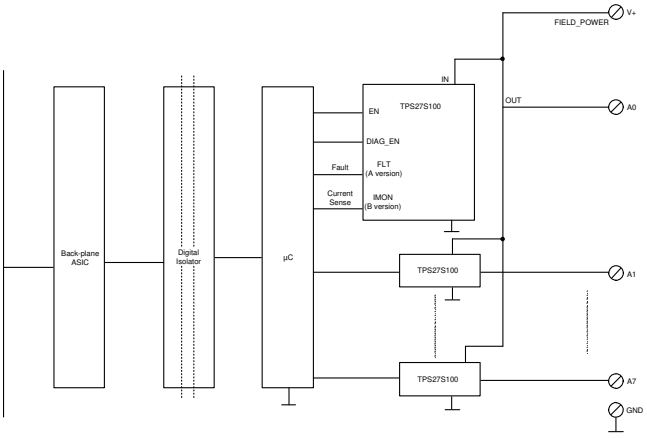
The TPS27S100x is a single-channel, fully-protected, high-side switch with an integrated NMOS and charge pump. Full diagnostics and high-accuracy current-monitor features enable intelligent control of the load. An adjustable current-limit function greatly improves the reliability of the whole system. The device diagnostic reporting has two versions to support both digital fault status and analog current monitor output. Accurate current monitor and adjustable current limit features differentiate it from the market.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS27S100x	HTSSOP (14)	4.40 mm × 5.00 mm
	QFN (16)	4.00 mm × 3.5 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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4 Revision History

Changes from Revision A (February 2018) to Revision B **Page**

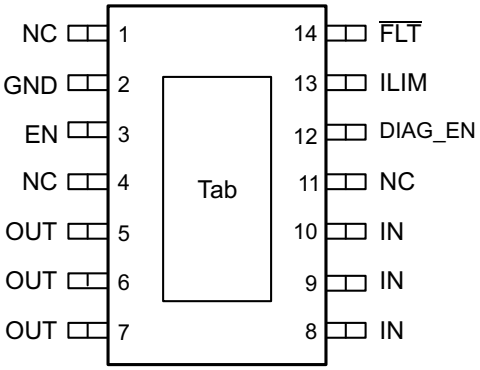
- Added the QFN Package to the *Features* section ... 1
- Added Package QFN (16) and Body Size 4.00 mm × 3.5 mm to the *Device Information* table ... 1
- Updated the *Typical Application Schematic* ... 1
- Added RRK Package to the *Pin Out Drawing* and *Pin Functions* table ... 3
- Updated the *Specifications Absolute Maximum Ratings* table ... 4
- Changed the Operation junction temperature range MAX from 150°C to 125°C in the *Specifications Recommended Operating Conditions* table ... 4
- Added RRK package to the *Specifications Thermal Information* table ... 4
- Updated the Operating Current section in the *Specifications Electrical Characteristics* table ... 4

Changes from Original (October 2017) to Revision A **Page**

- Added footnote 2 and 3 to the *Electrical Characteristics* table ... 4
- Added reverse current protection information to the *Reverse Current Protection* section ... 22

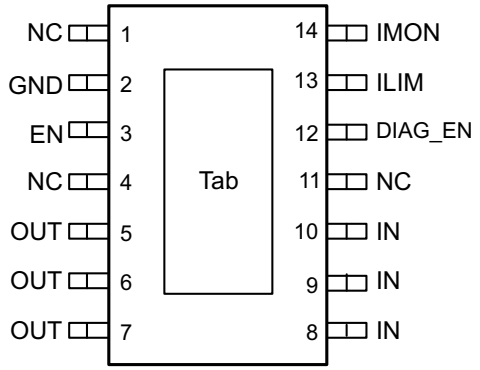
5 Pin Configuration and Functions

TPS27S100A PWP Package
14-Pin HTSSOP With Exposed Thermal Pad
Top View



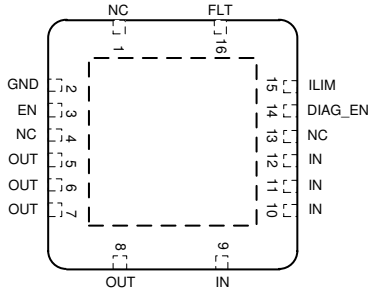
NC – No internal connection

TPS27S100B PWP Package
14-Pin HTSSOP With Exposed Thermal Pad
Top View



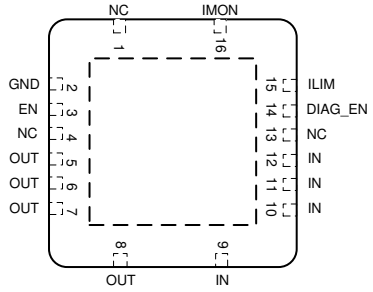
NC – No internal connection

TPS27S100A RRK Package
16-Pin QFN With Exposed Thermal Pad
Top View



NC – No internal connection

TPS27S100B RRK Package
16-Pin QFN With Exposed Thermal Pad
Top View



NC – No internal connection

Pin Functions

PIN					I/O	DESCRIPTION
NAME	TPS27S100 A PWP	TPS27S100 B PWP	TPS27S100 A RRK	TPS27S100B RRK		
DIAG_EN	12	12	14	14	I	Enable and disable pin for diagnostic functions. Connect to device GND if not used.
EN	3	3	3	3	I	Enable control for channel activation.
$\overline{\text{FLT}}$	14	—	16	—	O	Open-drain diagnostic status output. Leave floating if not used.
GND	2	2	2	2	—	Ground pin.
ILIM	13	13	15	15	O	adjustable current-limit pin. Connect to device GND if external current limit is not used.
IMON	—	14	—	16	O	Current-monitor output. Leave floating if not used.
IN	8, 9, 10	8, 9, 10	9, 10, 11, 12	9, 10, 11, 12	I	Power supply.
NC	1, 4, 11	1, 4, 11	1, 4, 13	1, 4, 13	—	No-connect pin; leave floating.
OUT	5, 6, 7	5, 6, 7	5, 6, 7, 8	5, 6, 7, 8	O	Output, connected to load.
Thermal pad	—	—	—	—	—	Thermal pad. Connect to device GND or leave floating.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)(2)

	MIN	MAX	UNIT
Supply voltage		40	V
Supply voltage (for transients less than 400 ms)		48	V
Current on GND pin, t < 2 minutes	–250	100	mA
Voltage on EN and DIAG_EN pins	–0.3	7	V
Current on EN and DIAG_EN pins	–10		mA
Voltage on $\overline{FLT}$ pin	–0.3	7	V
Current on $\overline{FLT}$ pin	–30	10	mA
Voltage on ILIM pin	–0.3	7	V
Voltage on IMON pin	–2.7	6.5	V
Inductive load switch-off energy dissipation, single pulse(3)		70	mJ
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Test condition: V_{IN} = 13.5 V, L = 8 mH, R = 0 Ω, T_J = 150°C. FR4 2s2p board, 2- × 70-µm Cu, 2- × 35-µm Cu. 600-mm^2 board copper area.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) (1)	IN, OUT, GND	±5000	V
		Human body model (HBM) (1)	Other pins	±4000	
		Charged device model (CDM)		±750	
$V_{(ESD)}$	Electrostatic discharge	Contact/Air discharge, per IEC 61000-4-2 (2)	IN, OUT	±16000	V
$V_{(ESD)}$		Electrical fast transient, per IEC 61000-4-4 (2)	IN, OUT	±4000	V
$V_{(ESD)}$		Surge protection with 42 Ω, per IEC 61000-4-5; 1.2/50 µs (2)	IN, OUT	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Tested with application circuit shown in Figure 35 with C_{VIN1}= 47 µF, C_{VIN2}= 100 nF, C_{VOUT}= 22 nF and SM15T30A TVS input clamp. Supply voltage of 24 V DC is always ON, EN Inputs are High, so output is High (ON) and floating (no load).

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Operating voltage	5	40	V
V_{ENx}	Voltage on EN and DIAG_EN pins	0	5	V
V_{FLT}	Voltage on $\overline{FLT}$ pin	0	5	V
$I_{L,nom}$	Nominal dc load current	0	4	A
T_J	Operating junction temperature range	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS27S100x		UNIT
		PWP (HTSSOP)	RRK (QFN)	
		14 PINS	16 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	41	42.7	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	29.7	31.3	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	25.1	16.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

Thermal Information (continued)

THERMAL METRIC[1]		TPS27S100x		UNIT
		PWP (HTSSOP)	RRK (QFN)	
		14 PINS	16 PINS	
ψ_{JT}	Junction-to-top characterization parameter	0.9	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24.8	16.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.7	4.6	°C/W

6.5 Electrical Characteristics

5 V < V_{IN} < 40 V; –40°C < T_J < 150°C unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING VOLTAGE						
$V_{IN(nom)}$	Nominal operating voltage		4		40	V
$V_{IN(uvr)}$	Undervoltage restart	V_{IN} rises up	3.5	3.7	4	V
$V_{IN(uvf)}$	Undervoltage shutdown	V_{IN} falls down	3	3.2	3.5	V
$V_{(uv,hys)}$				0.5		V
OPERATING CURRENT						
$I_{(op)}$	Nominal operating current	V_{EN} = 5 V, V_{DIAG_EN} = 0 V, 5 V < V_{IN} < 30 V, no load; –40°C T_J < 125°C		2.5	3.2	mA
$I_{(op)}$	Nominal operating current	V_{EN} = 5 V, V_{DIAG_EN} = 0 V, 5 V < V_{IN} < 40 V, no load; –40°C T_J < 150°C		2.5	5	mA
$I_{(op)}$	Nominal operating current	V_{EN} = 5 V, V_{DIAG_EN} = 0 V, 24-Ω load			10	mA
$I_{(off)}$	Standby mode current	V_{IN} = 24 V, V_{EN} = V_{DIAG_EN} = V_{IMON} = V_{ILIM} = V_{OUT} = 0 V, T_J = 25°C			2	µA
$I_{(off,diag)}$	Standby current with diagnostic enabled	V_{IN} = 24 V, V_{EN} = 0 V, V_{DIAG_EN} = 5 V			1.2	mA
$t_{(off,deg)}$	Standby mode deglitch time(1)	EN from high to low, if deglitch time > $t_{(off,deg)}$, the device enters into standby mode.		2		ms
$I_{lkg(out)}$	Off-state output leakage current	V_{IN} = 24 V, V_{EN} = V_{OUT} = 0, T_J = 25°C			0.5	µA
POWER STAGE						
$r_{DS(on)}$	On-state resistance	V_{IN} > 5 V, T_J = 25°C		80	100	mΩ
		V_{IN} > 5 V, T_J = 150°C			166	mΩ
		V_{IN} = 3.5 V, T_J = 25°C			120	mΩ
$I_{ILIM(int)}$	Internal current limit	Internal current limit value, ILIM pin connected to GND	7		13	A
$I_{ILIM(TSD)}$	Current limit during thermal shutdown	Internal current limit value under thermal shutdown		5		A
		External current limit value under thermal shutdown as a percentage of the external current limit setting value		50		%
$V_{DS(clamp)}$	Drain-to-source internal clamp voltage		50		70	V
OUTPUT DIODE CHARACTERISTICS						
V_F	Drain-to-source diode voltage	V_{EN} = 0, I_{OUT} = −0.2 A		0.7		V
$I_{(R1)}$	Continuous reverse current from source to drain	t < 60 s, V_{EN} = 0, T_J = 25°C. Short-to-supply condition.		2		A
$I_{(R2)}$	Continuous reverse current from source to drain	t < 60 s, V_{EN} = 0, T_J = 25°C. With GND network, 1-kΩ resistor in parallel with A diode. Reverse-polarity condition.		3		A
LOGIC INPUT (EN AND DIAG_EN)						
V_{IH}	Logic high-level voltage		2			V
V_{IL}	Logic low-level voltage				0.8	V
$R_{(EN,pd)}$	EN pulldown resistor			500		kΩ
$R_{(DIAG,pd)}$	DIAG_EN pulldown resistor			150		kΩ

(1) Value is specified by design, not subject to production test.

Electrical Characteristics (continued)

5 V < V_{IN} < 40 V; –40°C < T_J < 150°C unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIAGNOSTICS						
$V_{(ol,off)}$	Open-load detection threshold in off-state	V_{EN} = 0 V, When V_{IN} – V_{OUT} < $V_{(ol,off)}$, duration longer than $t_{d(ol,off)}$. Open load detected.	1.4	1.8	2.6	V
$I_{(ol,off)}$	Off-state output sink current with open load	V_{EN} = 0 V, V_{IN} = V_{OUT} = 24 V, T_J = 125°C.	–150			µA
$t_{d(ol,off)}$	Open-load detection-threshold deglitch time in off state	V_{EN} = 0 V, When V_{IN} – V_{OUT} < $V_{ol,off}$, duration longer than $t_{ol,off}$. Open load detected.		600		µs
$I_{(ol,on)}$	Open-load detection threshold in on state	V_{EN} = 5 V, when I_{OUT} < $I_{(ol,on)}$, duration longer than $t_{d(ol,on)}$. Open load detected. Version A only	2	6	10	mA
$t_{d(ol,on)}$	Open-load detection-threshold deglitch time in on-state	V_{EN} = 5 V, when I_{OUT} < $I_{(ol,on)}$, duration longer than $t_{d(ol,on)}$. Open load detected.		700		µs
$V_{(FLT)}$	Fault low output voltage	I_{FLT} = 2 mA			0.4	V
$T_{(SD)}$	Thermal shutdown threshold			175		°C
$T_{(SD,rst)}$	Thermal shutdown status reset			155		°C
$T_{(SW)}$	Thermal swing shutdown threshold			60		°C
$T_{(hys)}$	Hysteresis for resetting the thermal shutdown and swing			10		°C
CURRENT MONITOR AND CURRENT LIMIT						
$K_{(IMON)}$	Current sense current ratio			500		
$K_{(ILIM)}$	Current limit current ratio			2000		
$dK_{(IMON)}/K_{(IMON)}$	Current-monitor accuracy	I_{load} ≥ 5 mA	–80		80	%
		I_{load} ≥ 25 mA	–12		12	
		I_{load} ≥ 50 mA	–8		8	
		I_{load} ≥ 0.1 A	–5		5	
		I_{load} ≥ 1 A	–3		3	
$dK_{(ILIM)}/K_{(ILIM)}$	External current-limit accuracy(2), (3)	I_{limit} ≥ 0.5 A, 25°C < T_J < 150°C	–20		20	%
		I_{limit} ≥ 0.5 A, -40°C < T_J < 25°C	–28		28	%
$dK_{(ILIM)}/K_{(ILIM)}$	External current-limit accuracy(2), (3)	I_{limit} ≥ 1.6 A, 25°C < T_J < 150°C	–15		15	%
		I_{limit} ≥ 1.6 A, -40°C < T_J < 25°C	–18		18	
$V_{IMON(lin)}$	Current-monitor voltage linear voltage range(1)	V_{IN} ≥ 5 V	0		4	V
$I_{OUT(lin)}$	Current-monitor voltage linear current range(1)	V_{IN} ≥ 5 V, $V_{IMON(lin)}$ ≤ 4 V	0		4	A
$V_{IMON(H)}$	IMON pin voltage in Fault mode	V_{IN} ≥ 7 V, fault mode	4.3	4.75	4.9	V
		V_{IN} ≥ 5 V, fault mode	Min(V_{IN} – 0.8, 4.3)		4.9	
$I_{IMON(H)}$	IMON pin current in Fault mode	V_{IMON} = 4.3 V, V_{IN} > 7 V, fault mode	10			mA
$V_{IMON(th)}$	Current limit internal threshold voltage(1)			1.233		V

(2) External current limit set is recommended to be higher than 500 mA.
(3) External current limit accuracy is only applicable to overload conditions greater than 1.5 x the current limit setting.

6.6 Timing Requirements – Current Monitor Characteristics(1)

			MIN	NOM	MAX	UNIT
$t_{IMON(off1)}$	IMON settling time from DIAG_EN disabled	V_{EN} = 5 V, I_{load} ≥ 5 mA. V_{DIAG_EN} from 5 to 0 V. IMON to 10% of sense value.			10	µs
$t_{IMON(on1)}$	IMON settling time from DIAG_EN enabled	V_{EN} = 5 V, I_{load} ≥ 5 mA. V_{DIAG_EN} from 0 to 5 V. IMON to 90% of sense value.			10	µs
$t_{IMON(off2)}$	IMON settling time from EN falling edge	V_{DIAG_EN} = 5 V, I_{load} ≥ 5 mA. EN from 5 to 0 V. IMON to 10% of sense value.			10	µs
		V_{DIAG_EN} = 5 V, I_{load} ≥ 5 mA. EN from 5 to 0 V. Current limit triggered.			180	µs
$t_{IMON(on2)}$	IMON settling time from EN rising edge	V_{IN} = 24 V, V_{DIAG_EN} = 5 V, I_{load} ≥ 100 mA. V_{EN} from 0 to 5 V. IMON to 90% of sense value.			150	µs

(1) Value specified by design, not subject to production test.

6.7 Switching Characteristics

V_{IN} = 24 V, R_{load} = 24 Ω, over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	EN rising edge to V_{OUT} = 10%, DIAG_EN high	20		50	µs
$t_{d(off)}$	Turn-off delay time	EN falling edge to V_{OUT} = 90%, DIAG_EN high	40		80	µs
$dV/dt_{(on)}$	Slew rate on	V_{OUT} = 10% to 90%, DIAG_EN high	0.1		0.5	V/µs
$dV/dt_{(off)}$	Slew rate off	V_{OUT} = 90% to 10%, DIAG_EN high	0.1		0.5	V/µs

(1) Value specified by design, not subject to production test.

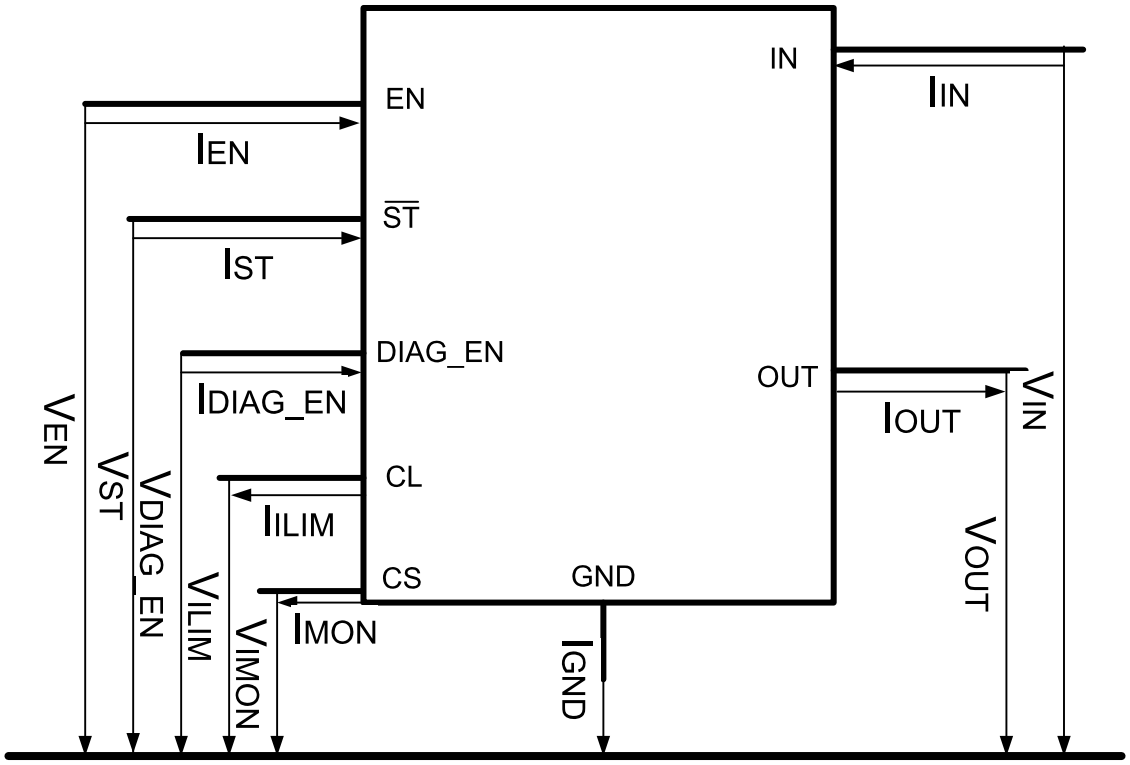


Figure 1. Pin Current and Voltage Conventions

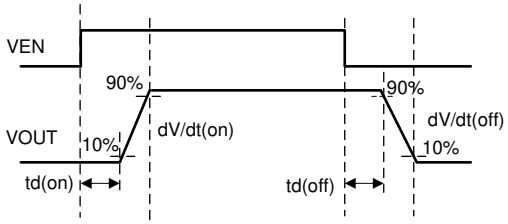


Figure 2. Output Delay Characteristics

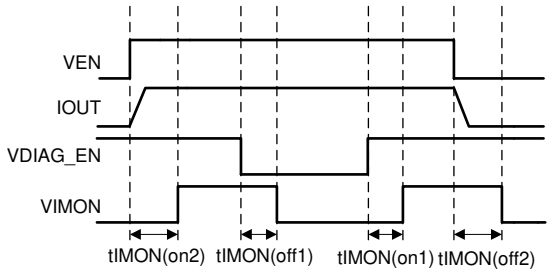


Figure 3. Current sense Delay Characteristics

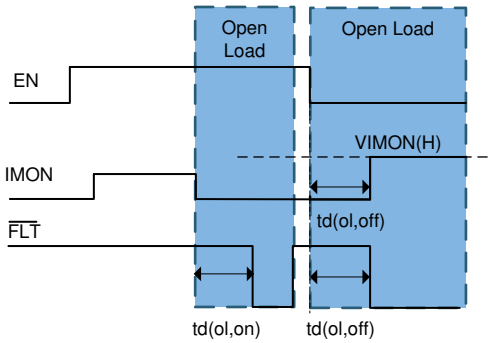


Figure 4. Open Load Blanking Time Characteristics

6.8 Typical Characteristics

All the below data are based on the mean value of the three lots samples, V_{IN} = 24 V if not specified.

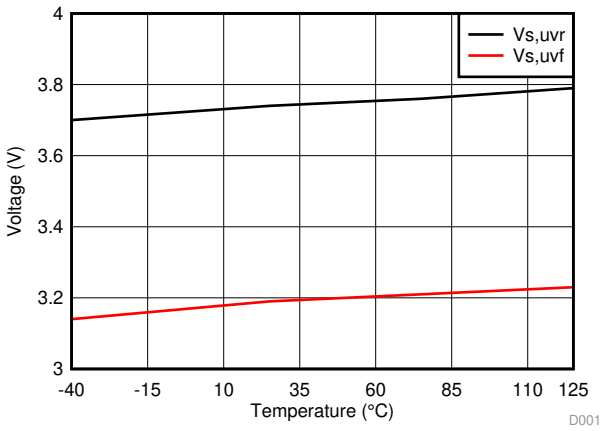


Figure 5. IN Pin Undervoltage Rising and Falling Thresholds $V_{IN,UVR}$ and $V_{IN,UVF}$

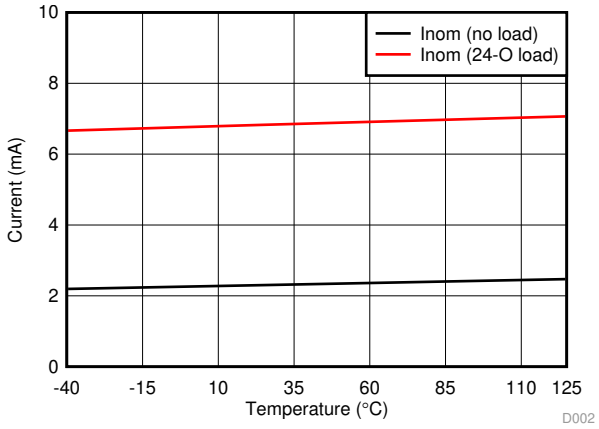


Figure 6. I_{nom} With No Load and 24-Ω Load

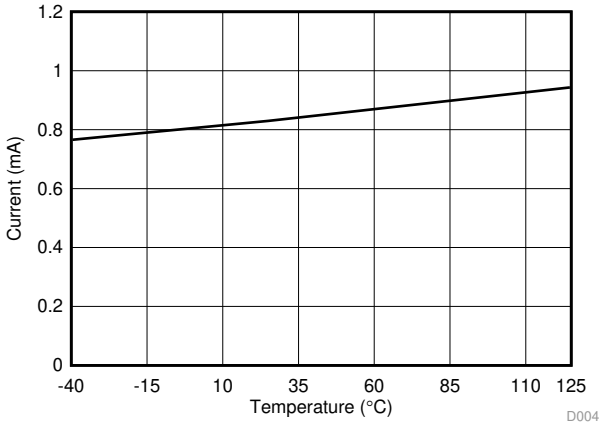


Figure 7. $I_{off,diag}$ as a Function of Temperature

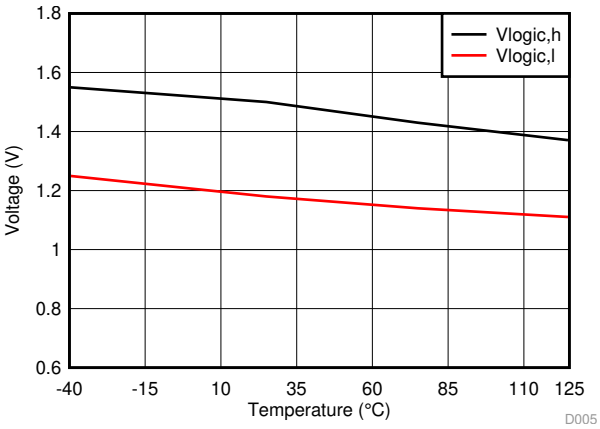


Figure 8. $V_{logic,h}$ and $V_{logic,l}$

Typical Characteristics (continued)

All the below data are based on the mean value of the three lots samples, V_{IN} = 24 V if not specified.

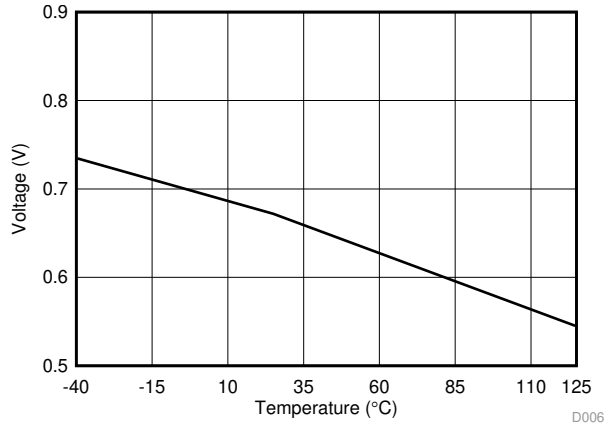


Figure 9. Drain-to-source Diode Voltage VF

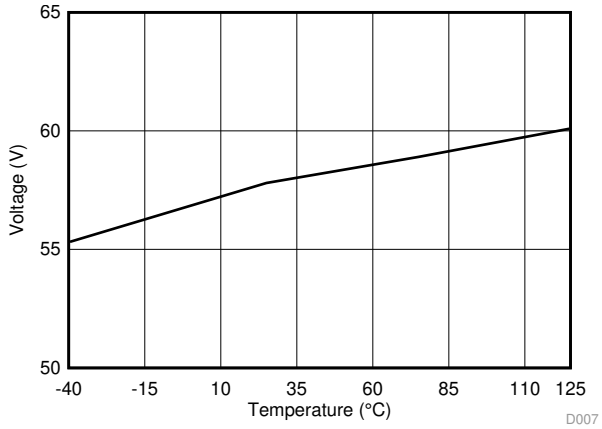


Figure 10. $V_{DS,\ Clamp}$

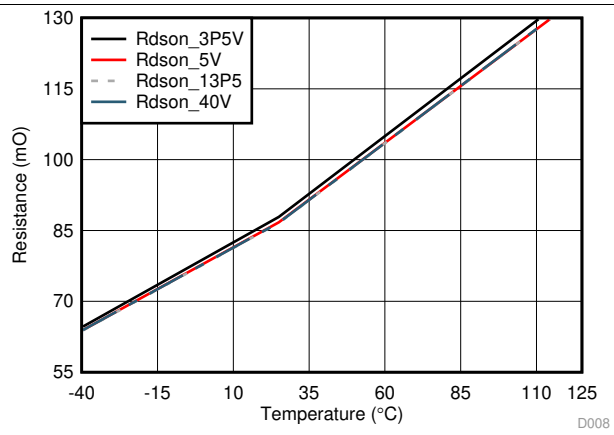


Figure 11. FET R_{DSON}

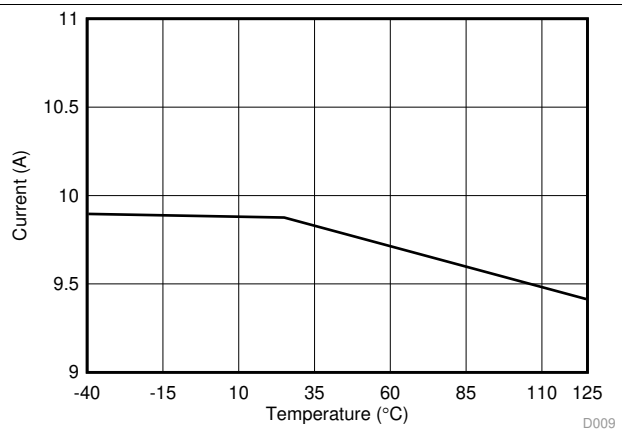


Figure 12. Current Limit $I_{lim,nom}$

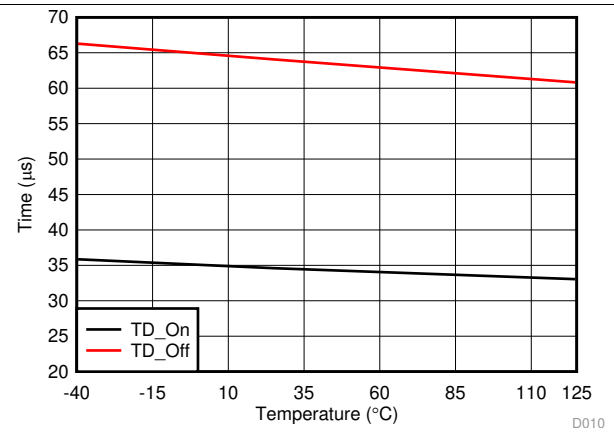


Figure 13. TDon and TDoff

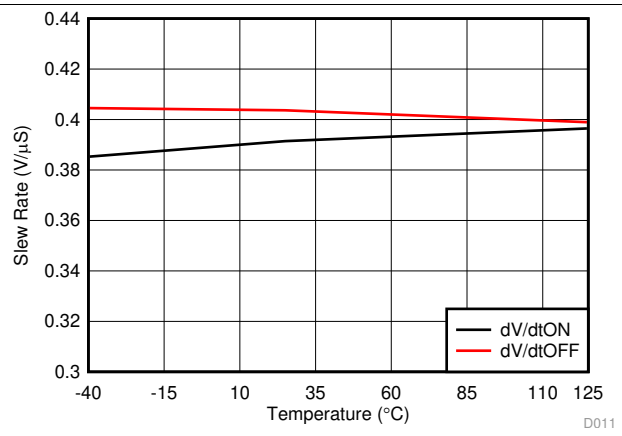


Figure 14. dV/dtON and dV/dtOFF

Typical Characteristics (continued)

All the below data are based on the mean value of the three lots samples, V_{IN} = 24 V if not specified.

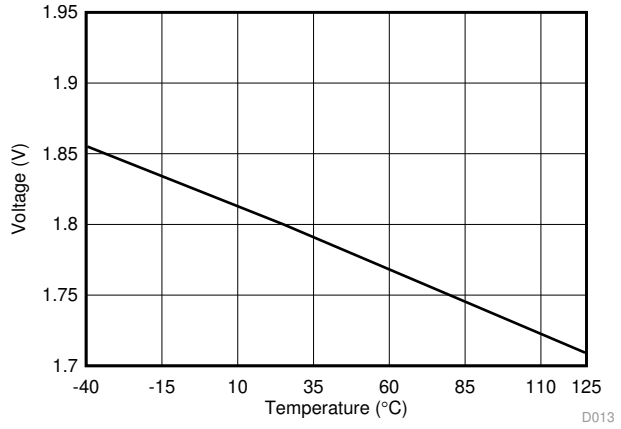


Figure 15. $V_{ol,off}$

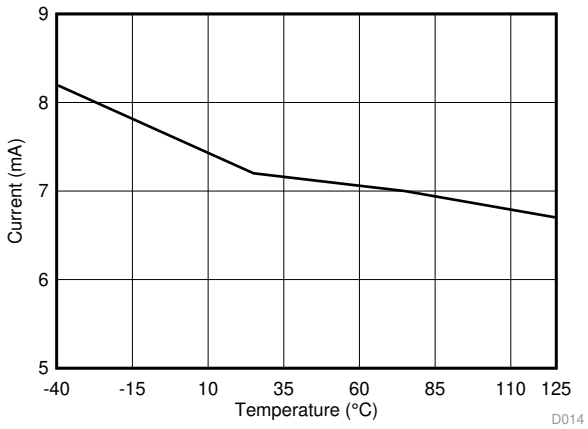


Figure 16. $I_{ol,on}$

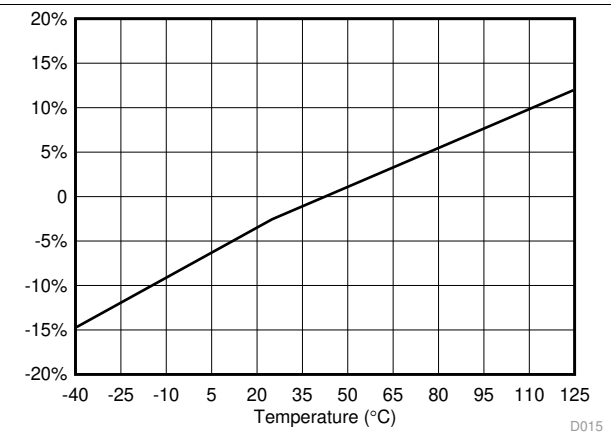


Figure 17. $K_{(IMON)}$ at I_{OUT} = 5 mA, V_{IN} = 24 V

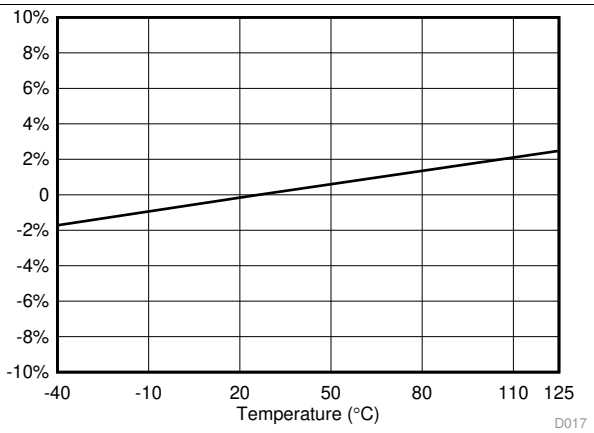


Figure 18. $K_{(IMON)}$ at I_{OUT} = 25 mA, V_{IN} = 24 V

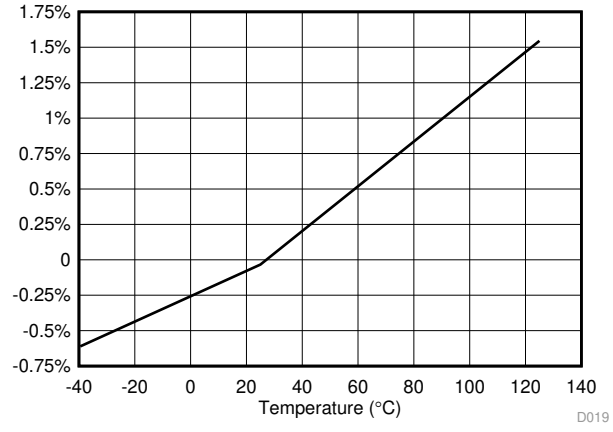


Figure 19. $K_{(IMON)}$ at I_{OUT} = 50 mA, V_{IN} = 24 V

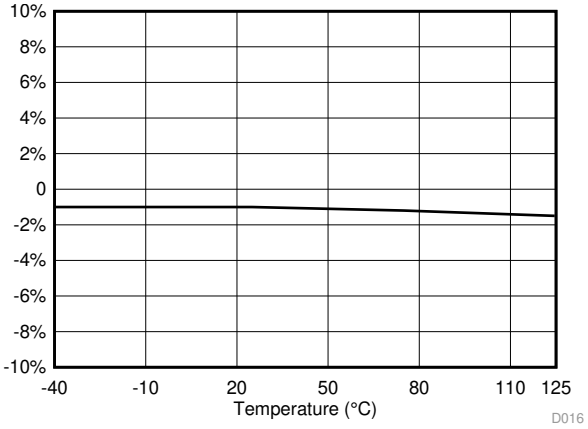


Figure 20. $K_{(IMON)}$ at I_{OUT} = 100 mA, V_{IN} = 24 V

Typical Characteristics (continued)

All the below data are based on the mean value of the three lots samples, V_{IN} = 24 V if not specified.

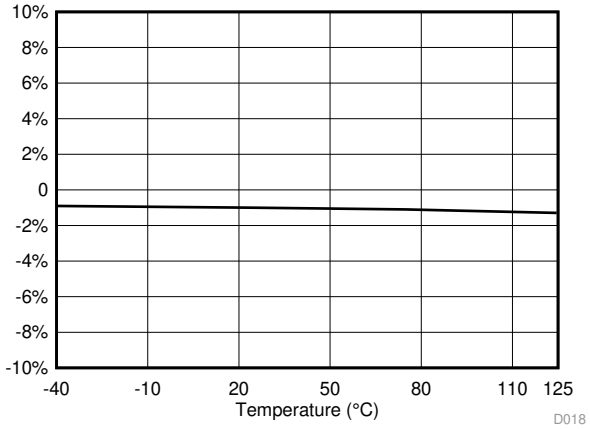


Figure 21. $K_{(IMON)}$ at I_{OUT} = 1 A, V_{IN} = 24 V

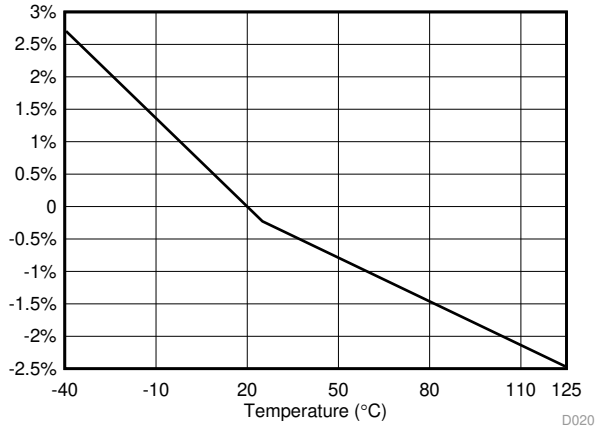


Figure 22. $K_{(ILIM)}$ at I_{ILIM} = 0.5 A, V_{IN} = 24 V

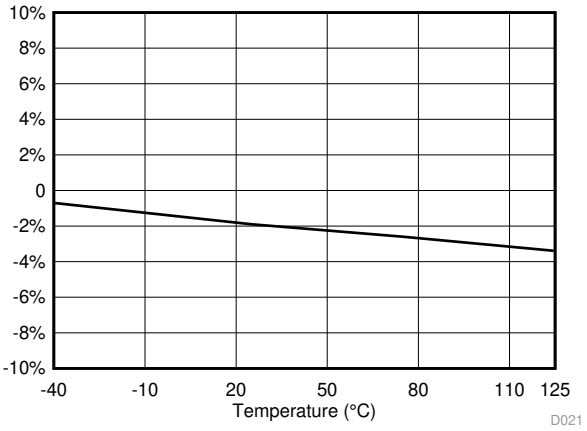


Figure 23. $K_{(ILIM)}$ at I_{ILIM} = 1.6 A, V_{IN} = 24 V

7 Detailed Description

7.1 Overview

The TPS27S100x is a single-channel, fully-protected, high-side switch with an integrated NMOS and charge pump. Full diagnostics and high-accuracy current-monitor features enable intelligent control of the load. An adjustable current-limit function greatly improves the reliability of the whole system. The device diagnostic reporting has two versions to support both digital fault status and analog current monitor output.

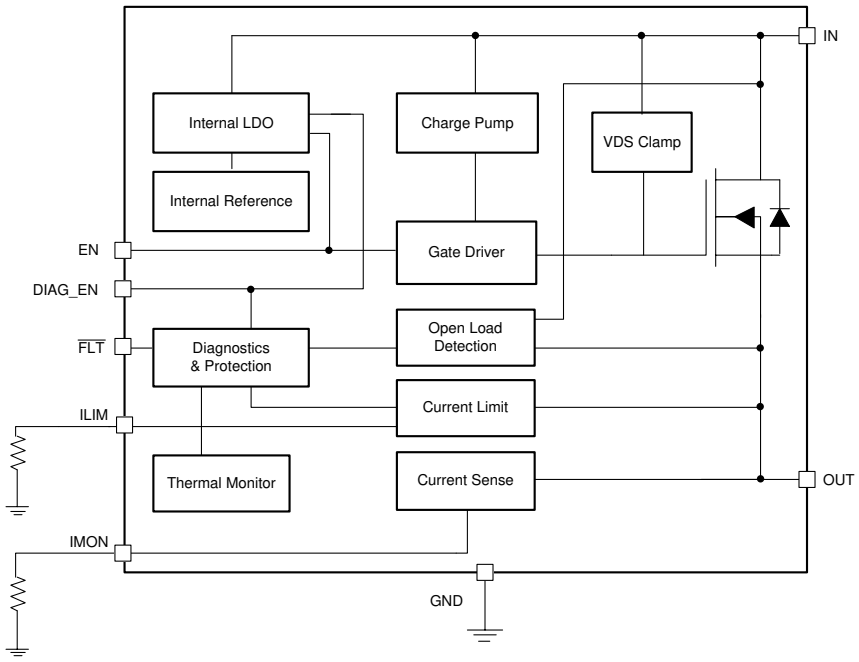
For TPS27S100A, the digital fault status report is implemented with an open-drain structure. For TPS27S100B, high-accuracy current-monitor allows a better real-time monitoring effect and more-accurate diagnostics without further calibration. A current mirror is used to source a fraction (1 / $K_{(IMON)}$) of the load current. $K_{(IMON)}$ is a nearly constant value across the temperature and supply voltage.

The external high-accuracy current limit allows setting the current limit value by application. Under start-up or short-circuit conditions, it improves the reliability of the system significantly by clamping the inrush current effectively. It can also save system costs by reducing PCB trace, connector size, and the preceding power-stage capacity. An internal current limit is also implemented in this device. The lower value of the external or internal current-limit value is applied.

An active drain to source voltage clamp is built in to address switching off the energy of inductive loads, such as relays, solenoids, motors, and so forth. During switching-off cycle, both the energy of the power supply and the inductive load are dissipated on the device itself. See *Inductive-Load Switching-Off Clamp* for more details.

The TPS27S100x device can be used as a high-side switch to drive a wide variety of resistive, inductive, and capacitive loads.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Accurate Current Monitor

For TPS27S100B, the high-accuracy current-monitor function is internally implemented, which allows a better real-time monitoring effect. A current mirror is used to source 1 / K_{IMON} of the load current, flowing out to the external resistor between the IMON and GND.

Feature Description (continued)

K_{IMON} is the ratio of the output current and the sense current. It is a constant value across the temperature and supply voltage range. Each part is factory calibrated during production test, so user-calibration is not required in most cases.

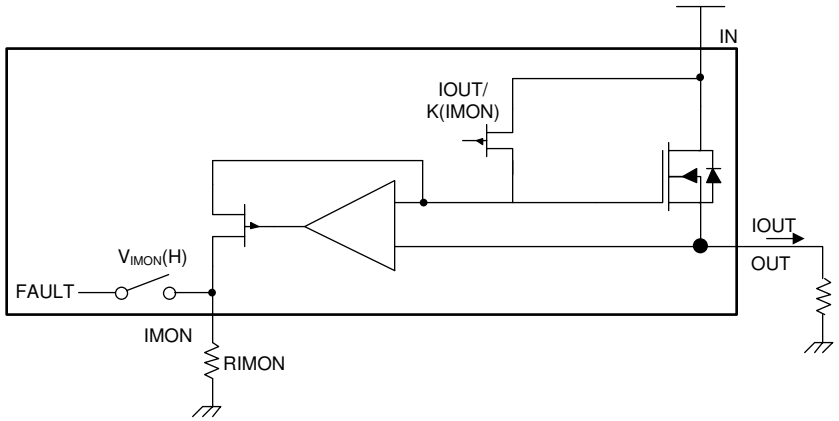


Figure 24. Current-monitor Block Diagram

When a fault occurs, the IMON pin also works as a fault report with a pullup voltage, $V_{IMON(H)}$.

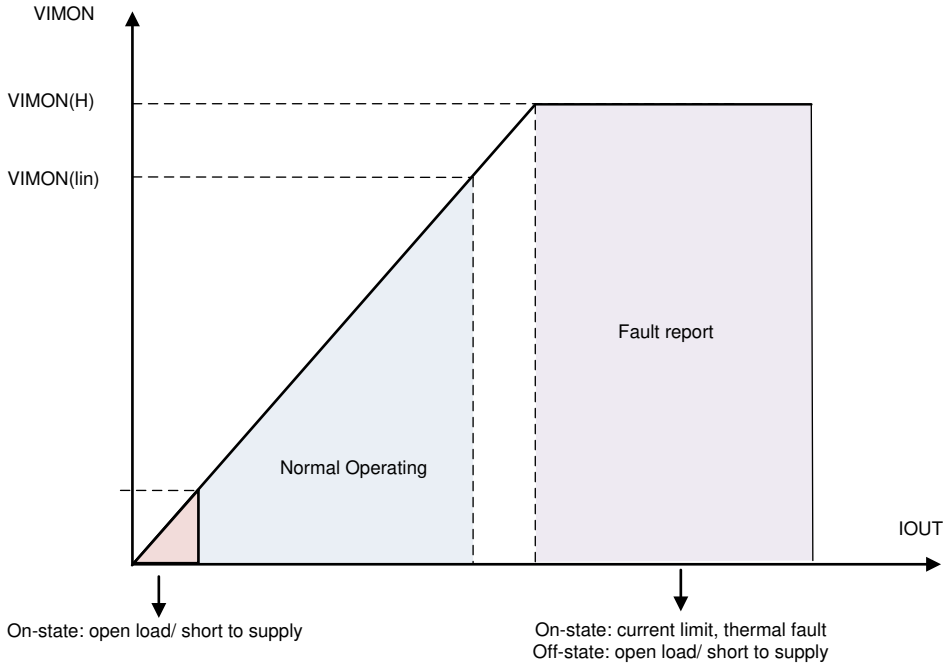


Figure 25. IMON Output-Voltage Curve

Use Equation 1 to calculate R_{IMON}. Also, please ensure V_{IMON} is within the current-sense linear region $V_{IMON(lin)}$ across the full range of the load current.

$$R_{IMON} = \frac{V_{IMON}}{I_{IMON}} = \frac{V_{IMON} \times K_{(IMON)}}{I_{OUT}} \quad (1)$$

Feature Description (continued)

7.3.2 Adjustable Current Limit

A high-accuracy current limit allows high reliability of the design. It protects the load and the power supply from over-stressing during short-circuit-to-GND or power-up conditions. The current limit can also save system cost by reducing the size of PCB traces and connectors, and the capacity of the preceding power stage.

When the current-limit threshold is hit, a closed loop activates immediately. The output current is clamped at the set value, and a fault is reported out. The device heats up due to the high power dissipation on the power FET. If thermal shutdown occurs, the current limit is set to $I_{ILIM(TSD)}$ to reduce the power dissipation on the power FET.

The device has two current-limit thresholds.

Internal current limit – The internal current limit is fixed at $I_{ILM(int)}$. Tie the ILIM pin directly to the device GND for large-transient-current applications.

External adjustable current limit – An external resistor is used to set the current-limit threshold. Use Equation 2 below to calculate the R_{ILIM}. $V_{ILIM(th)}$ is the internal band-gap voltage. $K_{(ILIM)}$ is the ratio of the output current and the current-limit set value. It is constant across the temperature and supply voltage. The external adjustable current limit allows the flexibility to set the current limit value by applications.

$$R_{ILIM} = \frac{V_{IILM(th)} \cdot K_{(ILIM)}}{I_{OUT}} \quad (2)$$

Note that if a GND network is used (which leads to the level shift between the device GND and board GND), the ILIM pin must be connected with device GND.

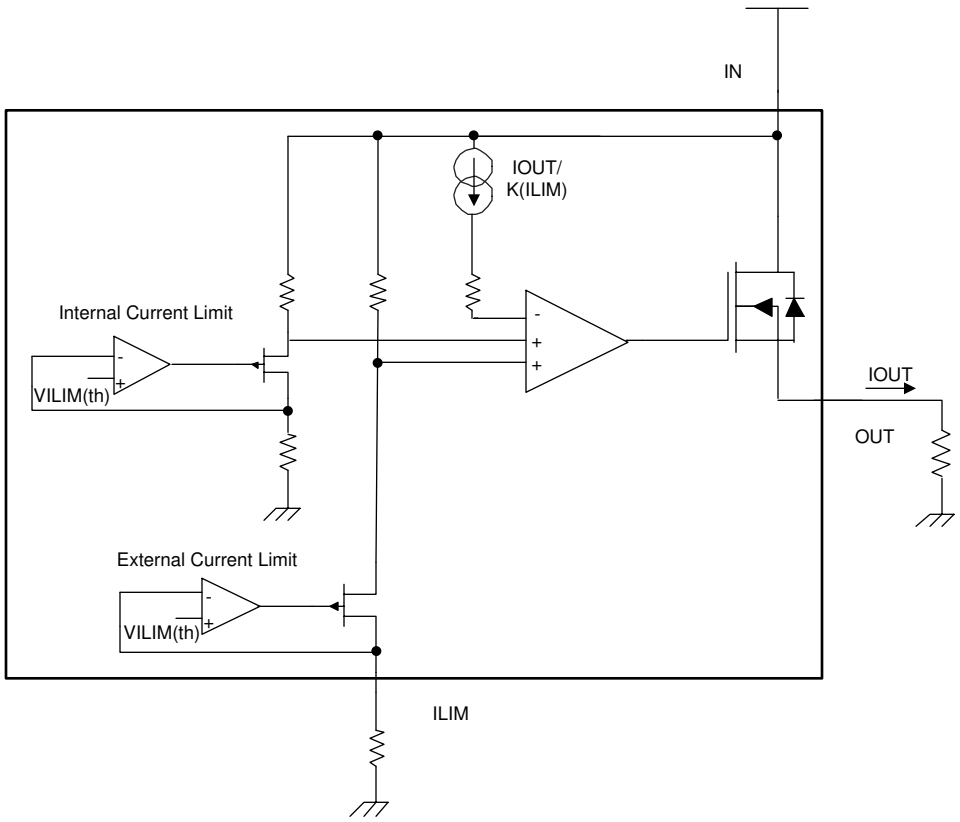


Figure 26. Current-Limit Block Diagram

For better protection from a hard short-to-GND condition (when the EN pin is enabled, a short to GND occurs suddenly), the device implements a fast-trip protection to turn off the channel before the current-limit closed loop is set up. The fast-trip response time is less than 1 μs, typically. With this fast response, the device can achieve better inrush current-suppression performance.

Feature Description (continued)

7.3.3 Inductive-Load Switching-Off Clamp

When switching an inductive load off, the inductive reactance tends to pull the output voltage negative. Excessive negative voltage could cause the power FET to break down. To protect the power FET, an internal clamp between drain and source is implemented, namely $V_{DS(clamp)}$.

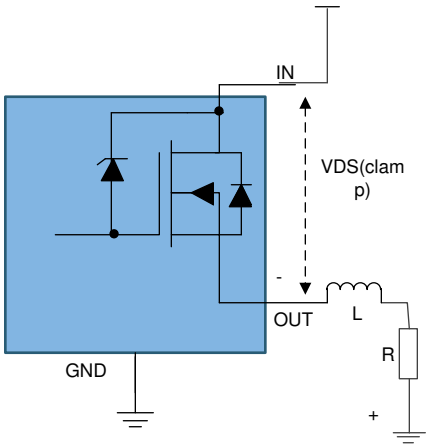


Figure 27. Drain-to-Source Clamping Structure

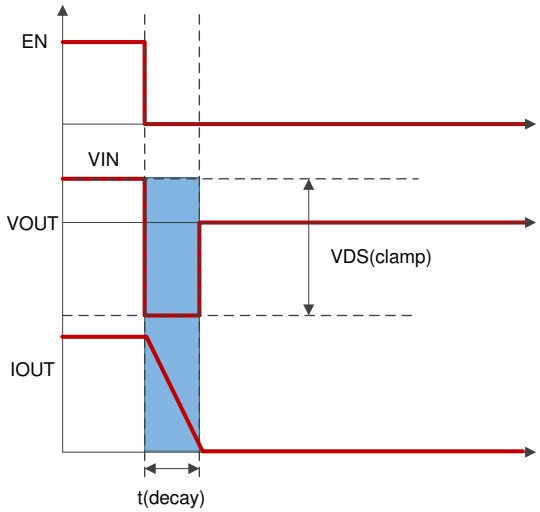


Figure 28. Inductive-Load Switching-Off Diagram

7.3.4 Full Protections and Diagnostics

Table 1 is when DIAG_EN enabled. When DIAG_EN is low, all the diagnostics is disabled accordingly. The output is in high-impedance mode. Refer to Table 2 for details.

Table 1. Fault Table

CONDITIONS	IN	OUT	CRITERION	$\overline{\text{FLT}}$ (TPS27S100A)	IMON (TPS27S100B)	FAULT RECOVERY
Normal	L	L		H	0	
	H	H		H	In linear region	
Short to GND	H	L	Current limit triggered.	L	$V_{IMON(H)}$	AUTO

Feature Description (continued)

Table 1. Fault Table (continued)

CONDITIONS	IN	OUT	CRITERION	$\overline{FLT}$ (TPS27S100A)	IMON (TPS27S100B)	FAULT RECOVERY
Open load(1) Short to supply	H	H	TPS27S100A: $I_{OUT} < I_{(ol,on)}$ TPS27S100B: Judged by users	L	Almost 0	AUTO
	L	H	$V_{IN} - V_{OUT} < V_{(ol,off)}$	L	$V_{IMON(H)}$	AUTO
Thermal shutdown	H		T_{SD} triggered	L	$V_{IMON(H)}$	Recovery when $T_J < T_{(SD,rst)}$ or when EN toggles.
Thermal swing	H		T_{SW} triggered	L	$V_{IMON(H)}$	AUTO

(1) Need external pull-up resistor during off-state

Table 2. DIAG_EN Logic Table

DIAG_EN	EN	PROTECTIONS AND DIAGNOSTICS
HIGH	ON	See Table 1
	OFF	See Table 1
LOW	ON	Diagnostics disabled, protection normal IMON or $\overline{FLT}$ is high Impedance
	OFF	Diagnostics disabled, no protections IMON or $\overline{FLT}$ is high impedance

7.3.4.1 Short-to-GND and Overload Detection

When the switch is on, a short to GND or overload condition causes overcurrent. If the overcurrent triggers either the internal or external current-limit threshold, the fault condition is reported out. The microcontroller can handle the overcurrent by turning off the switch. The device heats up if no actions are taken. If a thermal shutdown occurs, the current limit is $I_{ILIM(TSD)}$ to keep the power stressing on the power FET to a minimum. The device automatically recovers when the fault condition is removed.

7.3.4.2 Open-Load Detection

When the channel is on, for TPS27S100A, if the current flowing through the output is less than $I_{(ol,on)}$, the device recognizes an open-load fault. For TPS27S100B, if an open-load event occurs, it can be detected as an ultra-low V_{IMON} and handled by the microcontroller.

When the channel is off, if a load is connected, the output is pulled down to GND. But if an open load occurs, the output voltage is close to the supply voltage ($V_{IN} - V_{OUT} < V_{(ol,off)}$), and the fault is reported out.

There is always a leakage current $I_{(ol,off)}$ present on the output due to internal logic control path or external humidity, corrosion, and so forth. Thus, TI recommends an external pullup resistor to offset the leakage current when an open load is detected. The recommended pullup resistance is 15 kΩ.

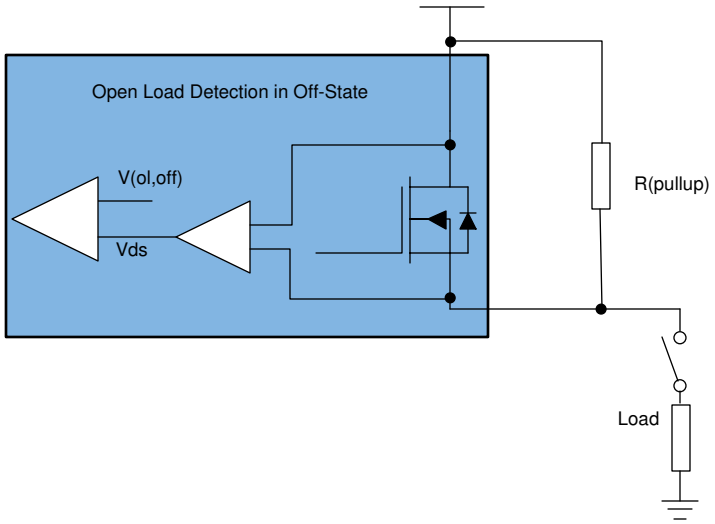


Figure 29. Open-Load Detection Circuit in Off-State

7.3.4.3 Short-to-Supply Detection

Short-to-Supply has the same detection mechanism and behavior as open-load detection, in both the on-state and off-state. See Table 1 for more details.

7.3.4.4 Thermal Fault Detection

To protect the device in severe power stressing cases, the device implements two types of thermal fault detection, absolute temperature protection (thermal shutdown) and dynamic temperature protection (thermal swing). Respective temperature sensors are integrated close to each power FET, so the thermal fault is reported by each channel. This arrangement can help the device keep the cross-channel effect to a minimum when some channels are in a thermal fault condition.

Thermal shutdown is active when the absolute temperature $T_J > T_{(SD)}$. When thermal shutdown occurs, the respective output turns off.

Thermal swing activates when the power FET temperature is increasing sharply, that is, when $\Delta T = T_{(FET)} - T_{(Logic)} > T_{(sw)}$, then the output turns off. The output automatically recovers and the fault signal clears when $\Delta T = T_{(FET)} - T_{(Logic)} < T_{(sw)} - T_{(hys)}$. Thermal swing function improves the device reliability when subjected to repetitive fast thermal variation.

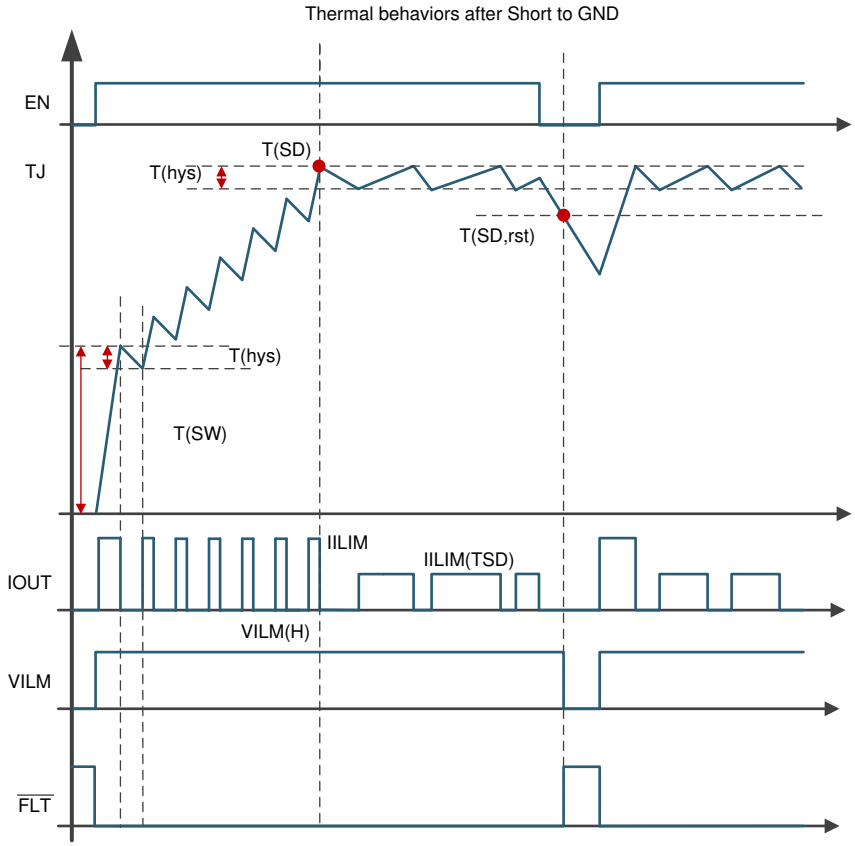


Figure 30. Thermal Behavior Diagram

7.3.4.5 UVLO Protection

The device monitors the supply voltage V_{IN}, to prevent unpredicted behaviors when V_{IN} is too low. When V_{IN} falls down to $V_{IN(uvf)}$, the device shuts down. When V_{IN} rises up to $V_{IN(uvr)}$, the device turns on.

7.3.4.6 Loss of GND Protection

When loss of GND occurs, output is shut down regardless of whether the EN pin is high or low. The device can protect against two ground-loss conditions, loss of device GND and loss of module GND.

7.3.4.7 Reverse Current Protection

Reverse current occurs in two conditions: short to supply and reverse polarity.

- When a short to the supply occurs, there is only reverse current through the body diode. $I_{R(1)}$ specifies the limit of the reverse current.
- In a reverse-polarity condition, there are reverse currents through the body diode and the device GND pin. $I_{R(2)}$ specifies the limit of the reverse current.

To protect the device, TI recommends two types of external circuitry.

- Adding a blocking diode. Both the IC and load are protected when in reverse polarity.

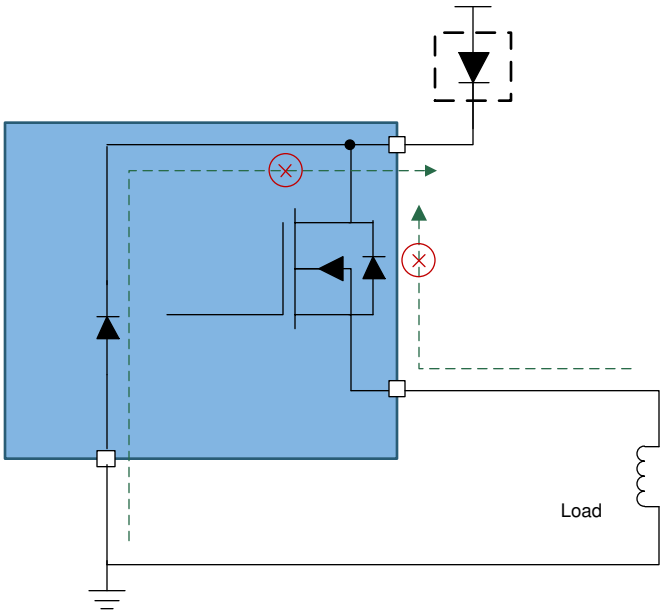


Figure 31. Reverse-Current External Protection, Method 1

- Adding a GND network. The reverse current through the device GND is blocked. The reverse current through the FET is limited by the load itself. TI recommends a resistor in parallel with the diode as a GND network. The recommended selection are 1-kΩ resistor in parallel with an >100-mA diode. The reverse current protection diode in the GND network forward voltage should be less than 0.6 V in any circumstances. In addition a minimum resistance of 4.7 K is recommended on the I/O pins.

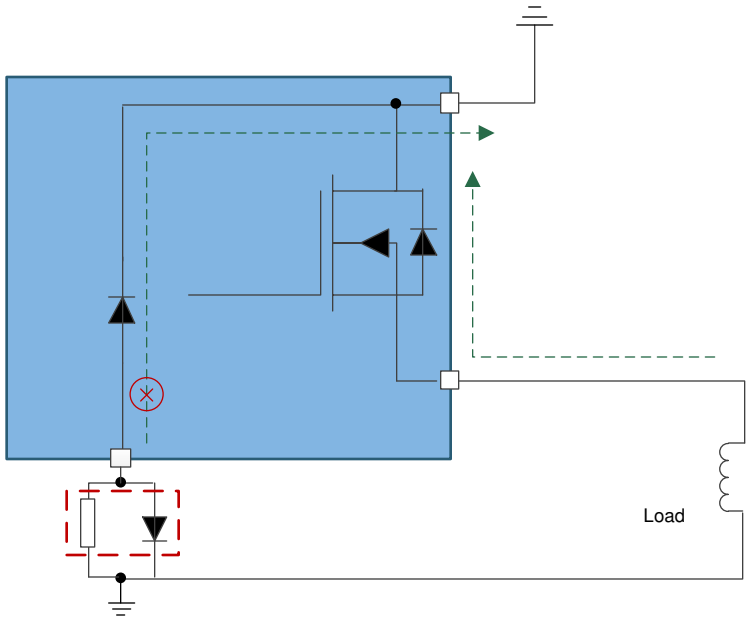


Figure 32. Reverse-Current External Protection, Method 2

7.3.4.8 Protection for MCU I/Os

TI recommends serial resistors to protect the microcontroller, for example, 4.7-kΩ when using a 3.3-V microcontroller and 10-kΩ for a 5-V microcontroller.

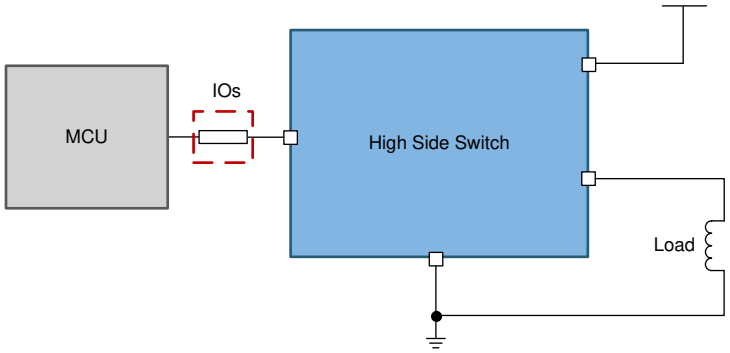


Figure 33. MCU I/O External Protection

7.4 Device Functional Modes

7.4.1 Working Mode

The device has three working modes: the normal mode, the standby mode, and the standby mode with diagnostics.

Device Functional Modes (continued)

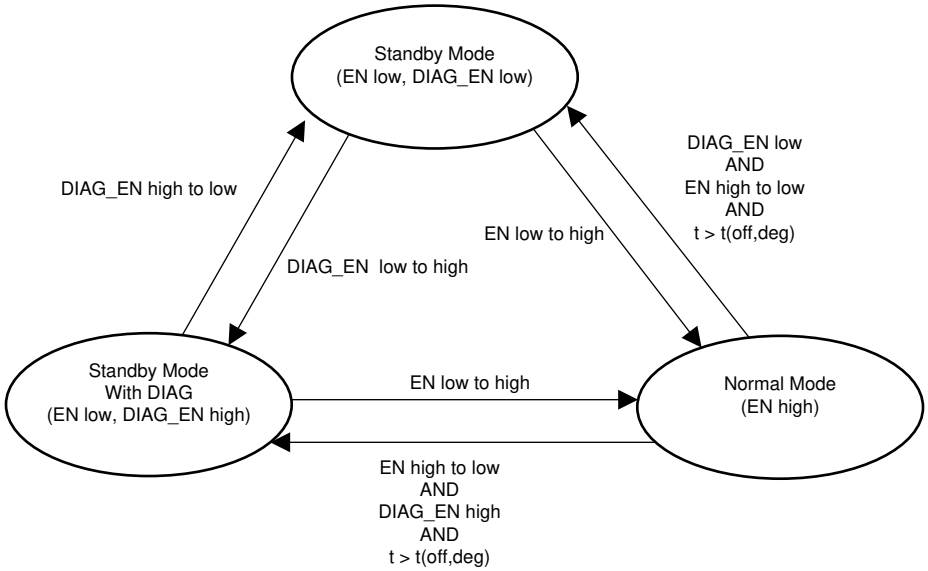


Figure 34. Working Modes

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The device is capable of driving a wide variety of resistive, inductive, and capacitive loads. Full diagnostics and high accuracy current-monitor features enable intelligent control of the load. An external adjustable current limit improves the reliability of the whole system by clamping the inrush or overload current.

8.2 Typical Application

Figure 35 shows an example of how to design the external circuitry parameters.

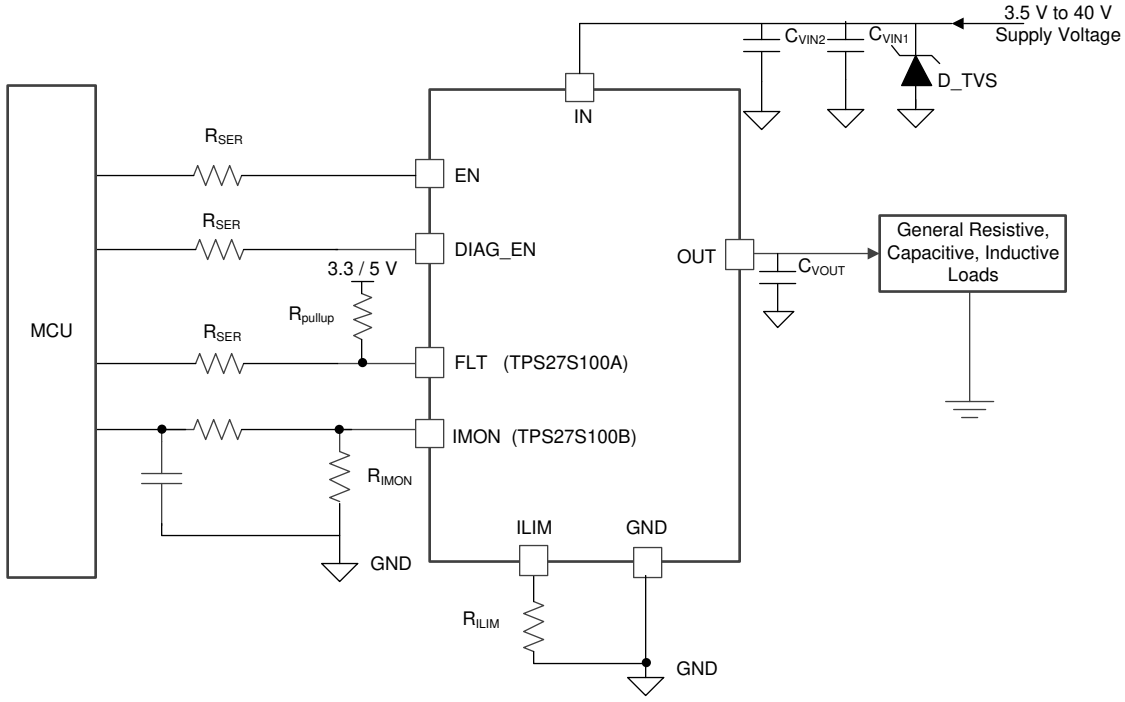


Figure 35. Typical Application Circuitry

Table 3. Recommended External Components

COMPONENT	TYPICAL VALUE	PURPOSE
R_{SER}	15 kΩ	Protect microcontroller and device I/O pins
R_{IMON}	1 kΩ	Translate the sense current into sense voltage
C_{SNS}	100 pF - 10 nF	Low-pass filter for the ADC input
R_{ILIM}	0.82 kΩ	Set current limit threshold
$C_{VIN1/2}$	4.7 nF to Device GND	Filtering of high frequency noise
	220 nF to Module GND	Stabilize the input supply and voltage spike suppression for surge transient immunity.
C_{OUT}	22 nF	Immunity to ESD
D_{TVS}	36V TVS diode	Transient voltage clamp for surge transient immunity

8.2.1 Design Requirements

- V_{IN} range from 9 V to 30 V
- Nominal current of 2 A
- Current Monitor for fault monitoring
- Expected current limit value of 5 A
- Full diagnostics with 5-V MCU

8.2.2 Detailed Design Procedure

To keep the 2-A nominal current in the 0 to 4-V current-sense range, calculate the R_{IMON} resistor using Equation 3. To achieve better current-sense accuracy, a 1% tolerance or better resistor is preferred.

$$R_{IMON} = \frac{V_{IMON} \times K_{(IMON)}}{I_{OUT}} = \frac{4 \times 500}{2} = 1000\ \Omega \quad (3)$$

To set the adjustable current limit value at 5-A, calculate R_{ILIM} using Equation 4.

$$R_{ILIM} = \frac{V_{LIM(th)} \cdot K_{(ILIM)}}{I_{OUT}} = \frac{1.233 \cdot 2000}{5} = 493.2\ \Omega \quad (4)$$

TI recommends R_{SER} = 10 kΩ for 5-V MCU, and R_{pullup} = 10 kΩ as the pull-up resistor.

8.2.3 Application Curves

Figure 36 shows a an example of initial inrush or short-circuit current limit. Test conditions: EN is from low to high, load is resistive short-to-GND or with a 470-µF capacitive load, external current limit is 2 A. CH1 is the output current. CH3 is the EN step.

Figure 37 shows an example of current limit during hard short-circuit. Test conditions: EN is high, load is (5 µH + 100 mΩ), external current limit is 1 A. A short to GND suddenly happens.

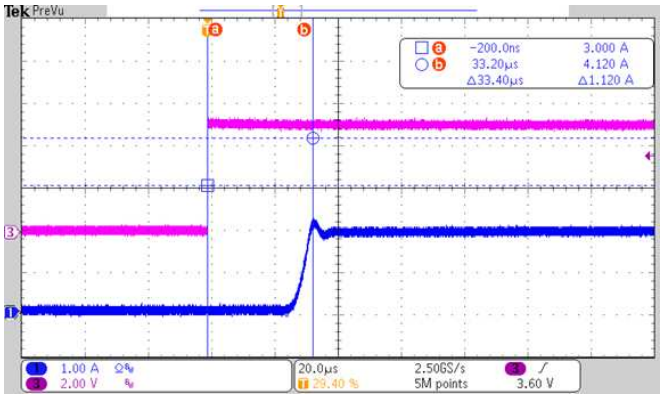


Figure 36. Initial Short-to-GND Waveform

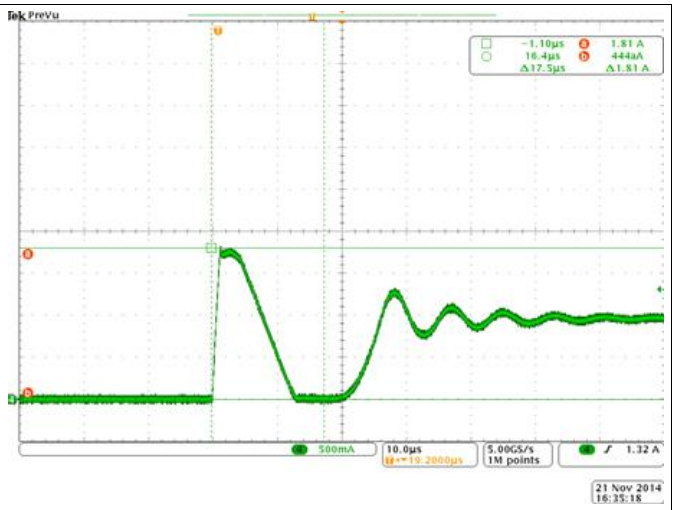


Figure 37. Hard Short-to-GND Waveform

9 Power Supply Recommendations

The device is qualified for both 12-V and 24-V applications. The typical power input is a 12-V or 24-V industrial power supply.

10 Layout

10.1 Layout Guidelines

To prevent thermal shutdown, T_J must be less than 150°C. If the output current is very high, the power dissipation may be large. The HTSSOP package has good thermal impedance. However, the PCB layout is very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat-flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the board opposite the package.
- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- All thermal vias should either be plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85%.

10.2 Layout Example

10.2.1 Without a GND Network

Without a GND network, tie the thermal pad directly to the board GND copper for better thermal performance.

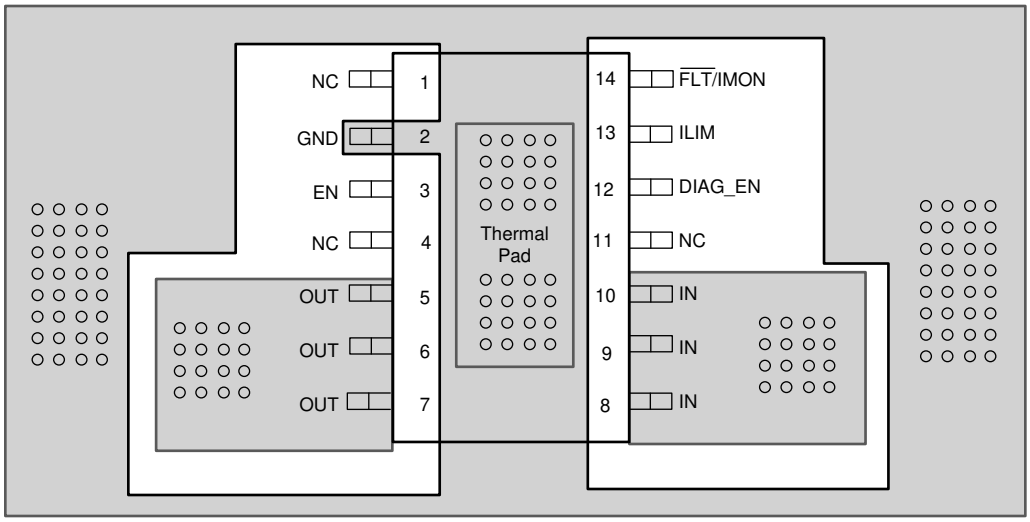


Figure 38. Layout Without a GND Network

Layout Example (continued)

10.2.2 With a GND Network

With a GND network, tie the thermal pad with a single trace through the GND network to the board GND copper.

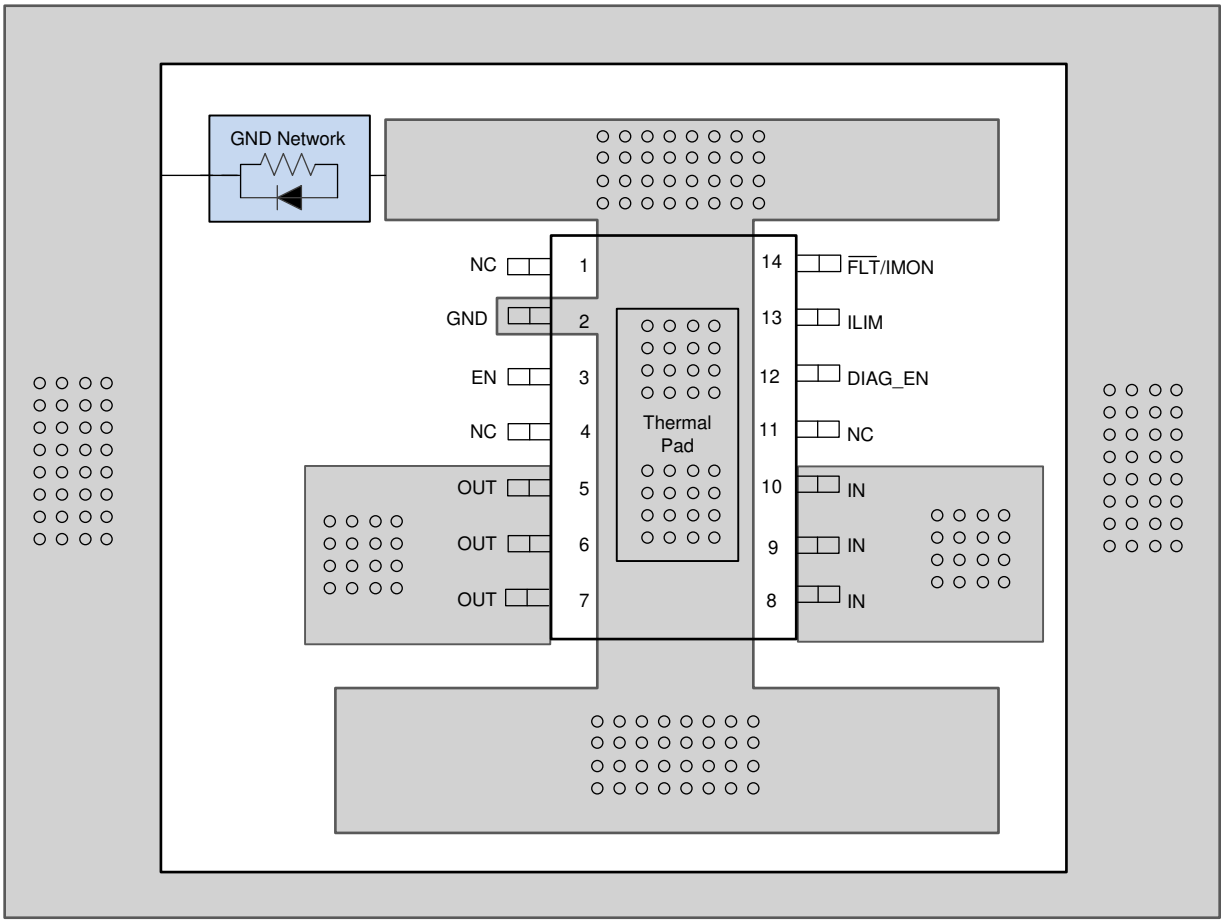


Figure 39. Layout With a GND Network

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS27S100APWPR	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	27S1A	Samples
TPS27S100APWPT	ACTIVE	HTSSOP	PWP	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	27S1A	Samples
TPS27S100ARRKR	ACTIVE	WQFN	RRK	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	27S100A	Samples
TPS27S100ARRKT	ACTIVE	WQFN	RRK	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	27S100A	Samples
TPS27S100BPWPR	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	27S1B	Samples
TPS27S100BPWPT	ACTIVE	HTSSOP	PWP	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	27S1B	Samples
TPS27S100BRRKR	ACTIVE	WQFN	RRK	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	27S100B	Samples
TPS27S100BRRKT	ACTIVE	WQFN	RRK	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	27S100B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

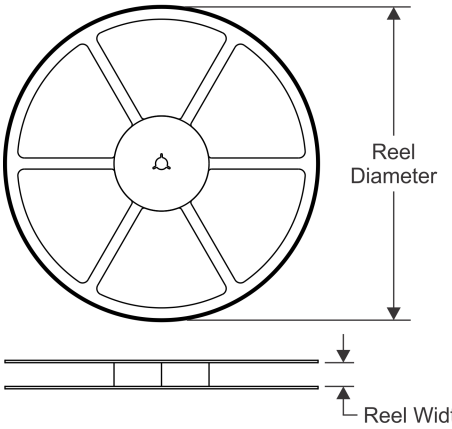
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

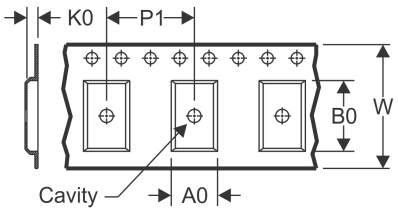
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

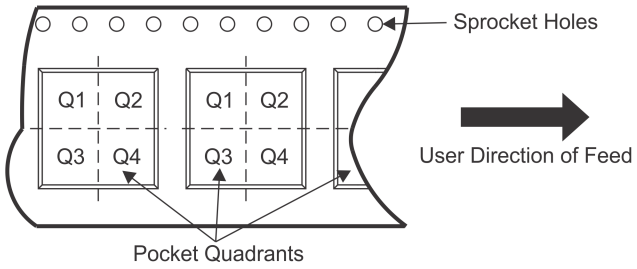


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

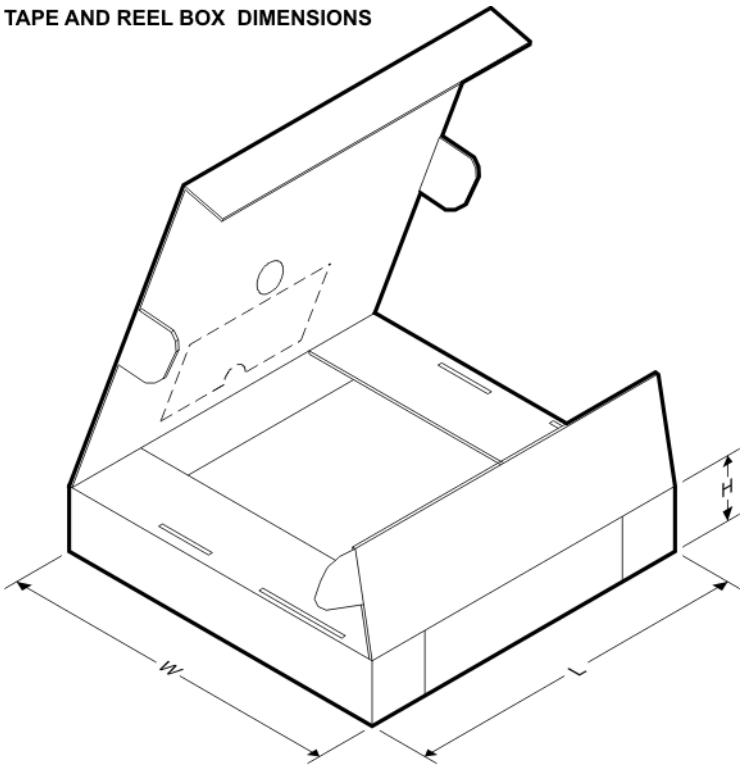
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS27S100APWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS27S100APWPT	HTSSOP	PWP	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS27S100ARRKR	WQFN	RRK	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
TPS27S100ARRKT	WQFN	RRK	16	250	180.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
TPS27S100BPWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS27S100BPWPT	HTSSOP	PWP	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS27S100BRRKR	WQFN	RRK	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
TPS27S100BRRKT	WQFN	RRK	16	250	180.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

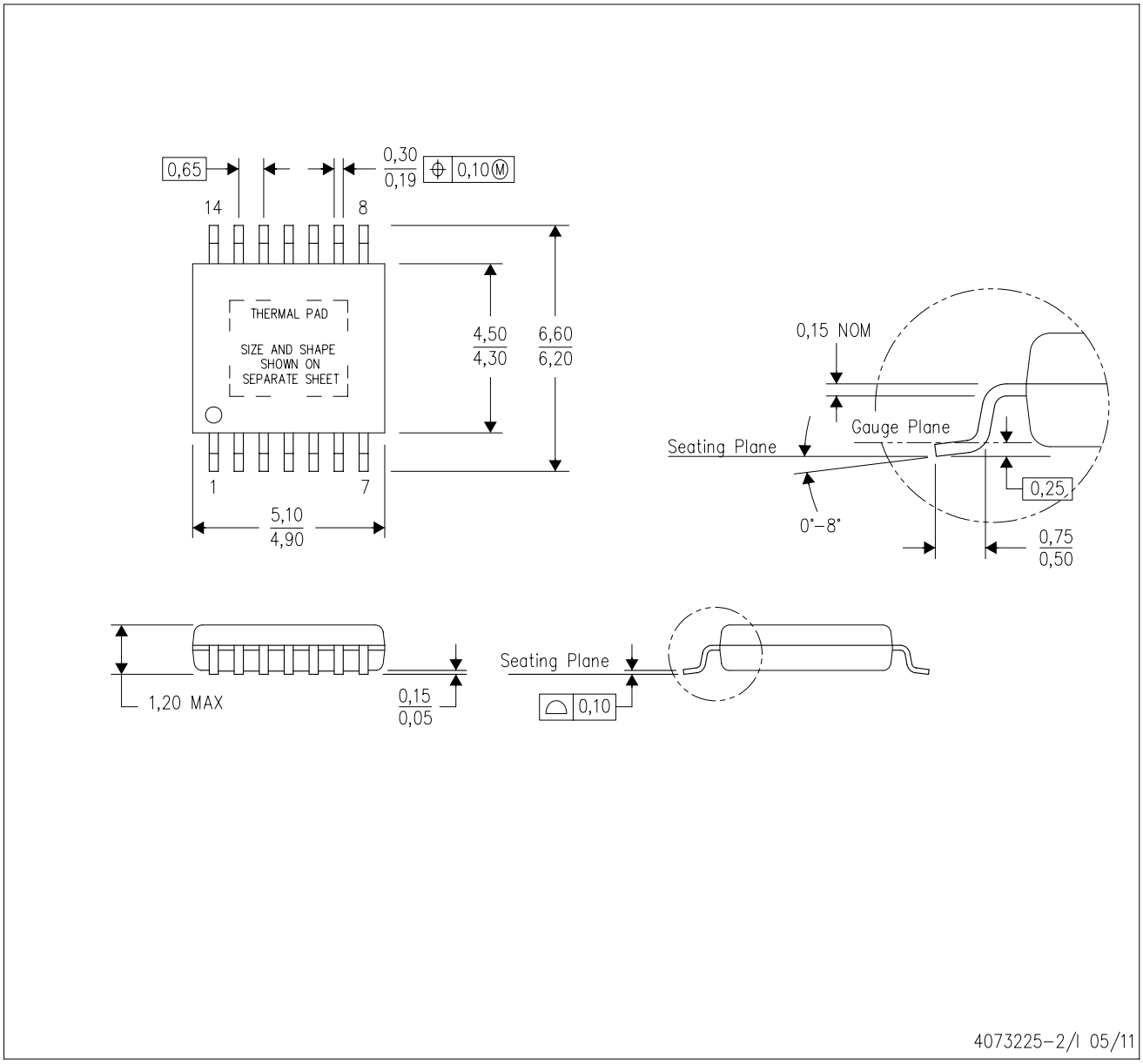
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS27S100APWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0
TPS27S100APWPT	HTSSOP	PWP	14	250	210.0	185.0	35.0
TPS27S100ARRKR	WQFN	RRK	16	3000	367.0	367.0	35.0
TPS27S100ARRKT	WQFN	RRK	16	250	210.0	185.0	35.0
TPS27S100BPWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0
TPS27S100BPWPT	HTSSOP	PWP	14	250	210.0	185.0	35.0
TPS27S100BRRKR	WQFN	RRK	16	3000	367.0	367.0	35.0
TPS27S100BRRKT	WQFN	RRK	16	250	210.0	185.0	35.0

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

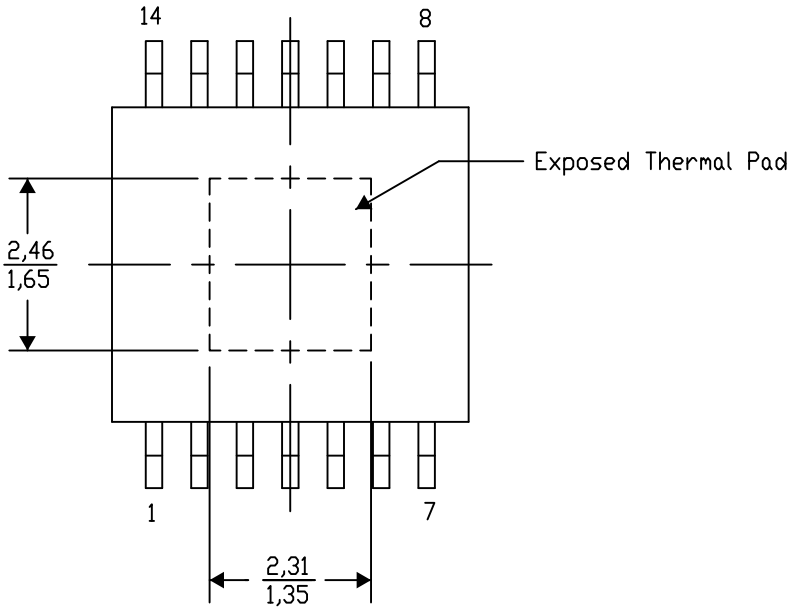
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

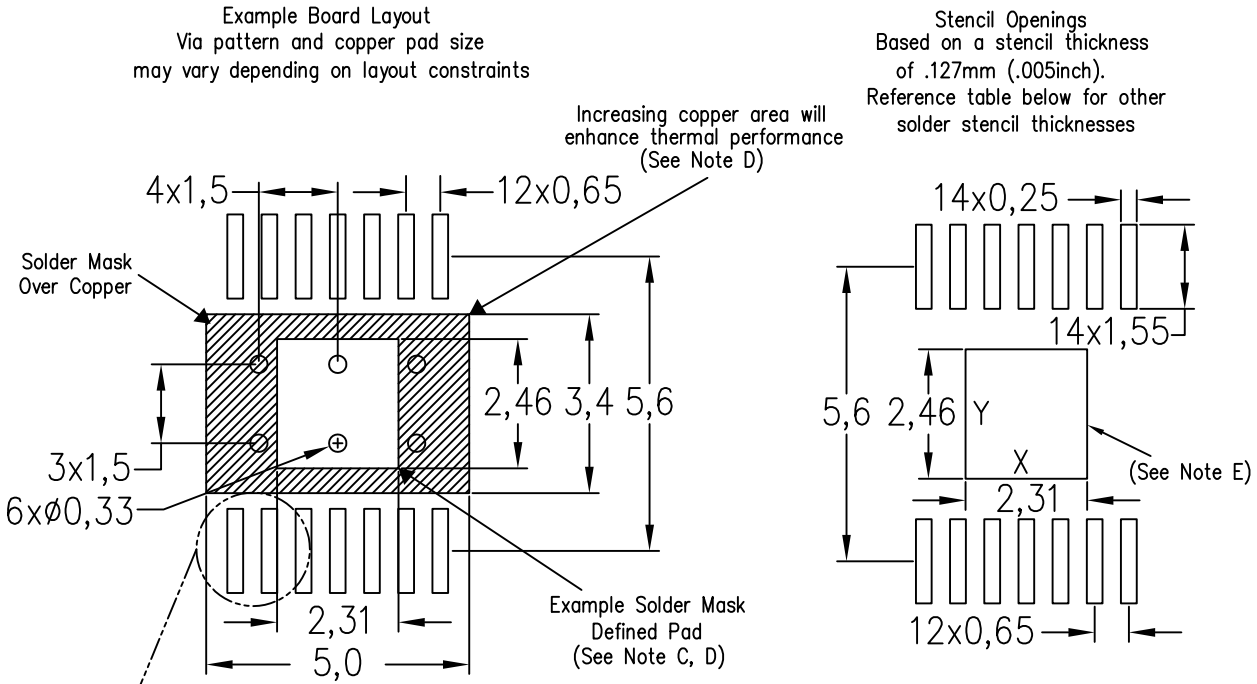
Exposed Thermal Pad Dimensions

4206332–2/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/W 09/15

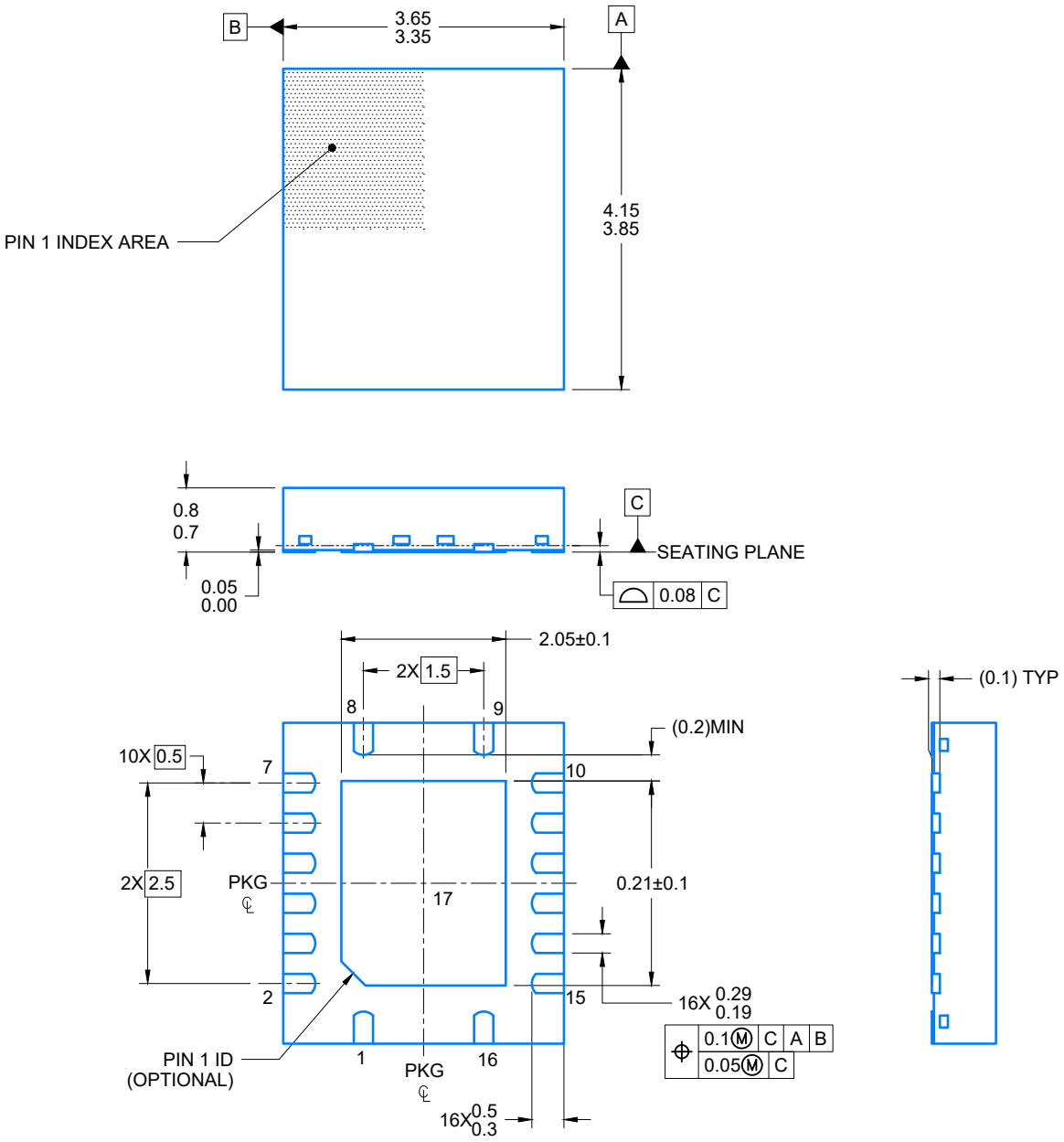
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

RRK0016A

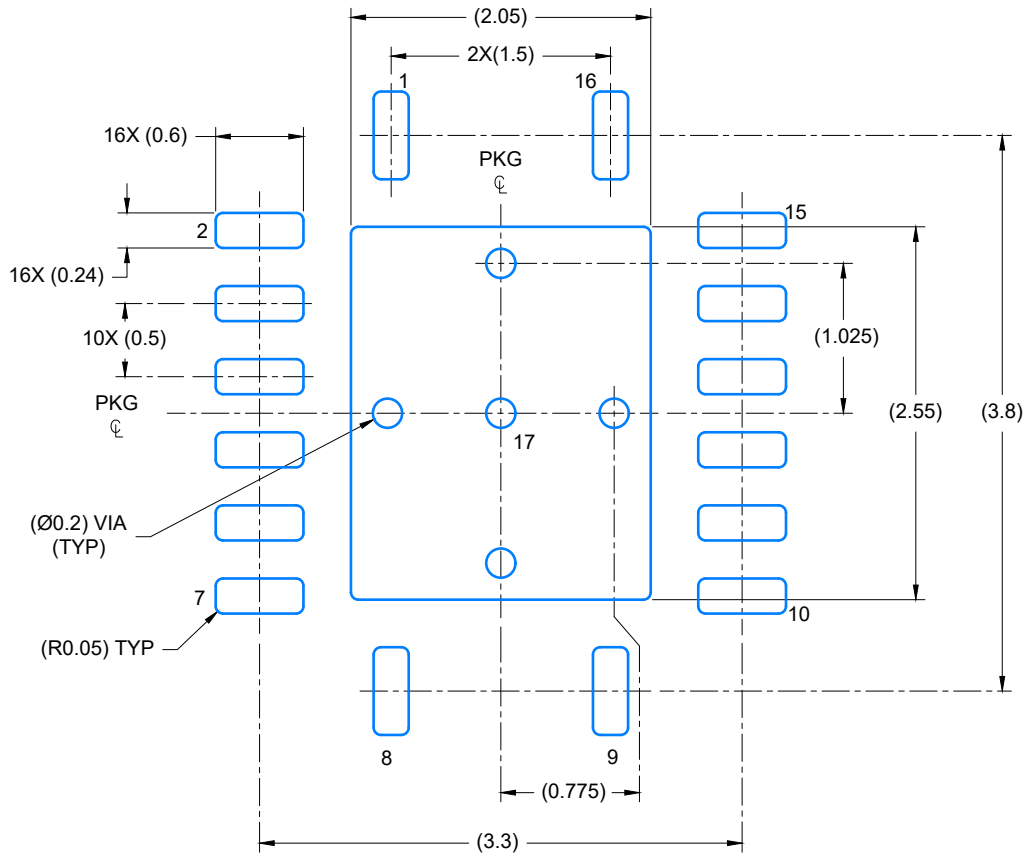
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD

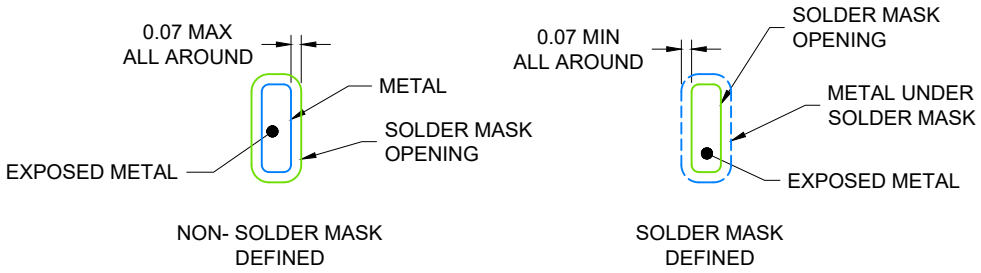


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

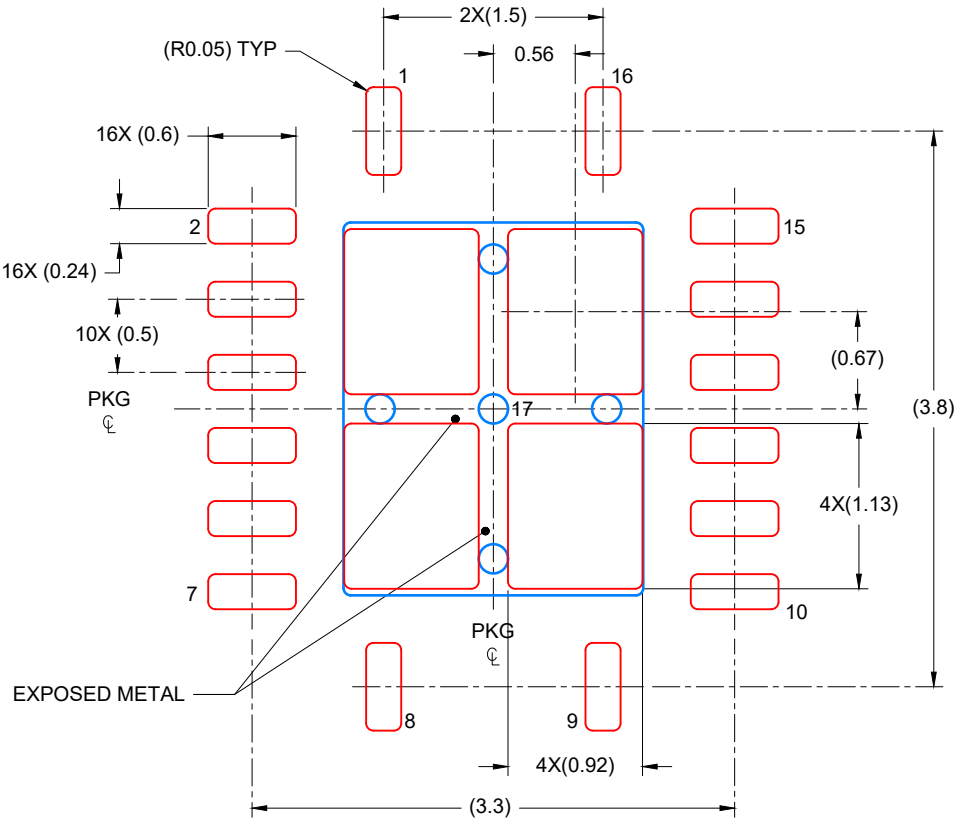


SOLDER MASK DETAILS

4424663 / A 11/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 17: 79%
SCALE: 20X

4424663 / A 11/2018

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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