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## MAX9140/MAX9141/ MAX9142/MAX9144

## 40ns, Low-Power, 3V/5V, Rail-to-Rail Single-Supply Comparators

### General Description

The MAX9140/MAX9141 are single and the MAX9142/MAX9144 are dual/quad high-speed comparators optimized for systems powered from a 3V or 5V supply. The MAX9141 features latch enable and device shutdown. These devices combine high speed, low power, and rail-to-rail inputs. Propagation delay is 40ns, while supply current is only 150 $\mu$ A per comparator.

The input common-mode range of the devices extends beyond both power-supply rails. The outputs pull to within 0.3V of either supply rail without external pullup circuitry, making these devices ideal for interface with both CMOS and TTL logic. All input and output pins can tolerate a continuous short-circuit fault condition to either rail. Internal hysteresis ensures clean output switching, even with slow-moving input signals.

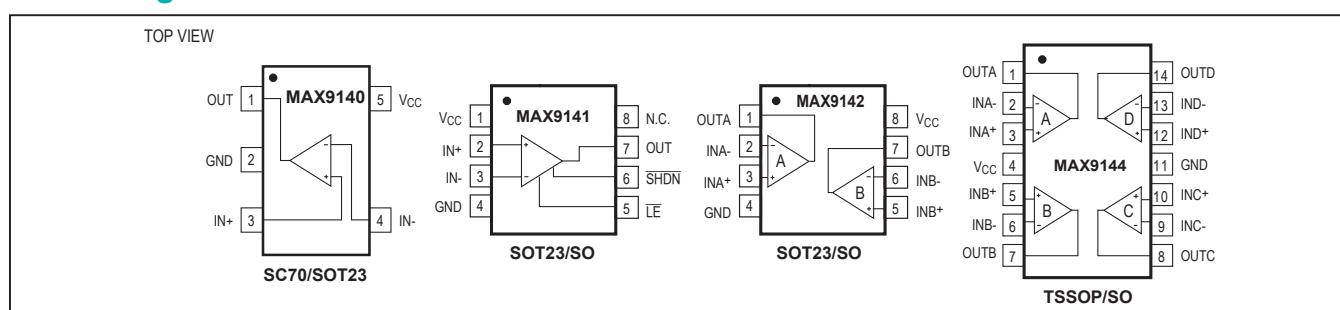
The devices are higher-speed, lower-power, and lower-cost upgrades to industry-standard comparators MAX941/MAX942/MAX944.

The MAX9140 are offered in tiny 5-pin SC70 and SOT23 packages. The MAX9141 and MAX9142 are available in 8-pin SOT23 and SO packages, while the MAX9144 is available in both 14-pin SO and TSSOP packages.

### Applications

- Line Receivers
- Battery-Powered Systems
- Threshold Detectors/Discriminators
- 3V/5V Systems
- Zero-Crossing Detectors
- Sampling Circuits

### Pin Configurations



## Absolute Maximum Ratings

### Power-Supply Ranges

Supply Voltage ( $V_{CC}$ to GND) .....	+6V
IN+, IN- to GND .....	-0.3V to ( $V_{CC}$ + 0.3V)
$\bar{LE}$ Input Voltage (MAX9141 only) .....	-0.3V to ( $V_{CC}$ + 0.3V)
SHDN Input Voltage (MAX9141 only) .....	-0.3V to ( $V_{CC}$ + 0.3V)
Current into Input Pins .....	$\pm 20\text{mA}$
Input/Output Short-Circuit Duration to $V_{CC}$ or GND .....	Continuous
Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )	
5-Pin SC70 (derate 3.1mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$ ) .....	247mW
5-Pin SOT23 (derate 7.1mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$ ) .....	571mW

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8-Pin SOT23 (derate 9.1mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$ ) .....	727mW
8-Pin SO (derate 5.9mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$ ) .....	470.6mW
14-Pin TSSOP (derate 9.1mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$ ) .....	727mW
14-Pin SO (derate 8.33mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$ ) .....	666.7mW

Operating Temperature Range	
E grade .....	-40 $^\circ\text{C}$ to +85 $^\circ\text{C}$
A grade .....	-40 $^\circ\text{C}$ to +125 $^\circ\text{C}$
Junction Temperature .....	+150 $^\circ\text{C}$
Storage Temperature Range .....	-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$
Lead Temperature (soldering, 10s) .....	+300 $^\circ\text{C}$

## Electrical Characteristics

( $V_{CC} = 5\text{V}$ ,  $V_{CM} = 0\text{V}$ ,  $\bar{SHDN} = \bar{LE} = V_{CC}$  (MAX9141 only),  $C_L = 15\text{pF}$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ\text{C}$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage	$V_{CC}$	(Note 2)		2.7	5.5		V
Input Voltage Range	$V_{CMR}$	(Note 3)		-0.2	$V_{CC} + 0.2$		V
Input Offset Voltage	$V_{OS}$	(Note 4)	$T_A = +25^\circ\text{C}$	0.5	2.0		mV
			$T_A = -40^\circ\text{C}$ to +85 $^\circ\text{C}$	4.5			
			MAX9140AA__	6.0			
Input Hysteresis	$V_{HYST}$	(Note 5)		1.5			mV
Input Bias Current	$I_B$	(Note 6)	$T_A = -40^\circ\text{C}$ to +85 $^\circ\text{C}$	90	320		nA
			MAX9140AA__	350			
Input Offset Current	$I_{OS}$		$T_A = -40^\circ\text{C}$ to +85 $^\circ\text{C}$	8	120		nA
			MAX9140AA__	140			
Common-Mode Rejection Ratio	CMRR	$V_{CC} = 5.5\text{V}$ (Note 7)	$T_A = -40^\circ\text{C}$ to +85 $^\circ\text{C}$	80	800		$\mu\text{V/V}$
			MAX9140AA__	850			
Power-Supply Rejection Ratio	PSRR	$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	$T_A = -40^\circ\text{C}$ to +85 $^\circ\text{C}$	80	750		$\mu\text{V/V}$
			MAX9140AA__	800			
Output High Voltage	$V_{OH}$	$I_{SOURCE} = 4\text{mA}$	$T_A = -40^\circ\text{C}$ to +85 $^\circ\text{C}$	$V_{CC} - 0.425$	$V_{CC} - 0.3$		V
			MAX9140AA__	$V_{CC} - 0.47$			
Output Low Voltage	$V_{OL}$	$I_{SINK} = 4\text{mA}$	$T_A = -40^\circ\text{C}$ to +85 $^\circ\text{C}$	0.3	0.425		V
			MAX9140AA__	0.45			
Output Leakage Current	$I_{LEAK}$	$\bar{SHDN} = \text{GND}$ , MAX9141 only (Note 8)		0.04	1		$\mu\text{A}$

**Electrical Characteristics (continued)**

( $V_{CC} = 5V$ ,  $V_{CM} = 0V$ ,  $\overline{SHDN} = \overline{LE} = V_{CC}$  (MAX9141 only),  $C_L = 15pF$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (Per Comparator)	I <sub>CC</sub>	$V_{CM} = V_{CC} = 3V$	MAX9141	165	275	$\mu A$
			MAX9140, $T_A = -40^\circ C$ to $85^\circ C$	150	250	
			MAX9140AA_	360		
			MAX9142/MAX9144	150	250	
		$V_{CM} = V_{CC} = 5V$	MAX9141	200	320	
			MAX9140, $T_A = -40^\circ C$ to $85^\circ C$	165	300	
			MAX9140AA_	400		
			MAX9142/MAX9144	165	300	
		MAX9141 only, $\overline{SHDN} = GND$ ; $V_{CC} = V_{CM} = 3V$		12	30	
Propagation Delay	$t_{PD+}$ , $t_{PD-}$	$V_{CC} = 3V$ , $V_{OD} = 10mV$		40		ns
Differential Propagation Delay	$t_{DPD}$	$V_{OD} = 10mV$ (Note 9)		2		ns
Propagation Delay Skew		$V_{OD} = 10mV$ (Note 10)		2		ns
Logic Input-Voltage High	$V_{IH}$	(Note 11)	$(V_{CC}/2)$ +0.4	$V_{CC}/2$		V
Logic Input-Voltage Low	$V_{IL}$	(Note 11)	$V_{CC}/2$	$(V_{CC}/2)$ -0.4		V
Logic Input Current	$I_{IL}$ , $I_{IH}$	$V_{LOGIC} = 0$ to $V_{CC}$ (Note 11)	2	10		$\mu A$
Data-to-Latch Setup Time	$t_S$	(Note 12)		16		ns
Latch-to-Data Hold Time	$t_H$	(Note 12)		16		ns
Latch Pulse Width	$t_{LPW}$	(Note 12)		45		ns
Latch Propagation Delay	$t_{LPD}$	(Note 12)		60		ns
Shutdown Enable Time		(Note 13)		1		$\mu s$
Shutdown Disable Time		(Note 13)		5		$\mu s$

**Note 1:** All devices are 100% production tested at  $T_A = +25^\circ C$ . Specifications over temperature are guaranteed by design.

**Note 2:** Inferred from PSRR test.

**Note 3:** Inferred from CMRR test. Note also that either or both inputs can be driven to the absolute maximum limit (0.3V beyond either supply rail) without damage or false output inversion.

**Note 4:**  $V_{OS}$  is defined as the center of the input-referred hysteresis zone. See Figure 1.

**Note 5:** The input-referred trip points are the extremities of the differential input voltage required to make the comparator output change state. The difference between the upper and lower trip points is equal to the width of the input-referred hysteresis zone. See Figure 1.

**Note 6:** The polarity of  $I_B$  reverses direction as  $V_{CM}$  approaches either supply rail.

**Note 7:** Specified over the full common-mode voltage range ( $V_{CMR}$ ).

**Note 8:** Specification is for current flowing into or out of the output pin for  $V_{OUT}$  driven to any voltage from  $V_{CC}$  to GND while the part is in shutdown.

**Note 9:** Specified between any two channels in the MAX9142/MAX9144.

**Note 10:** Specified as the difference between  $t_{PD+}$  and  $t_{PD-}$  for any one comparator.

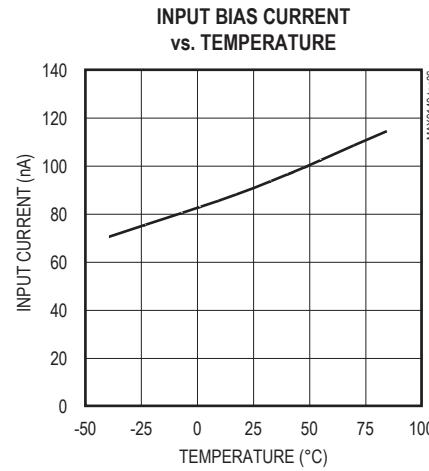
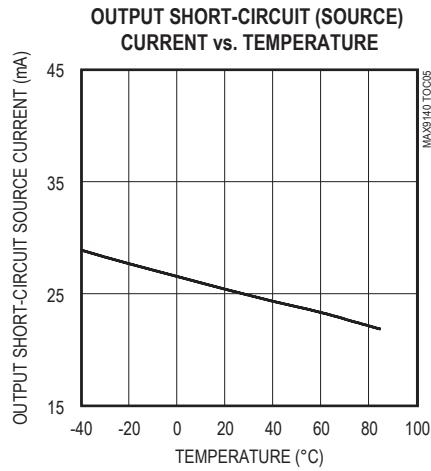
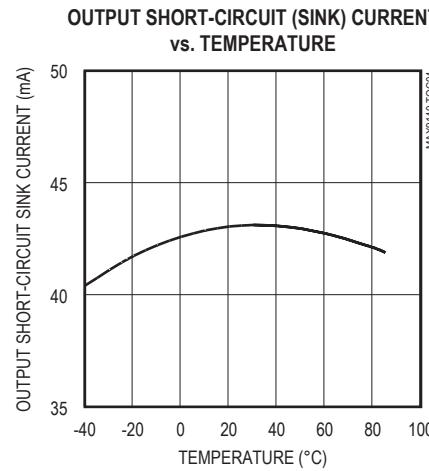
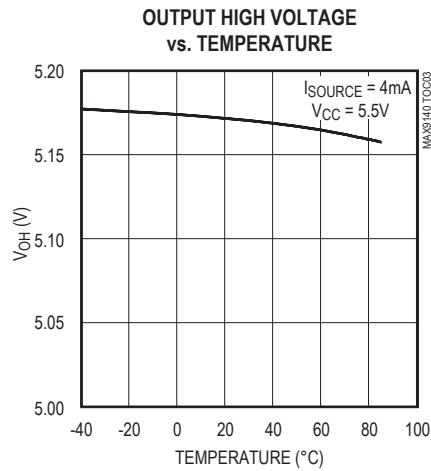
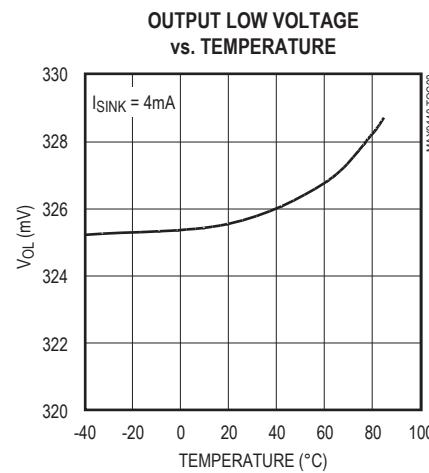
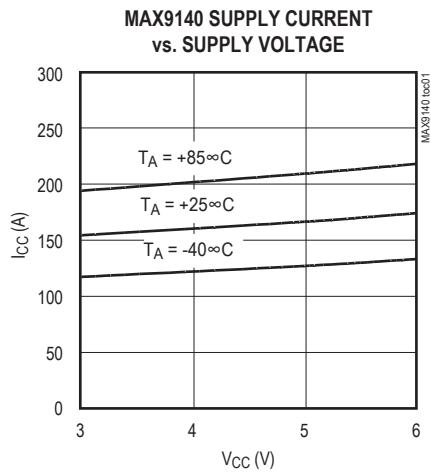
**Note 11:** Applies to the MAX9141 only for both  $\overline{SHDN}$  and  $\overline{LE}$ .

**Note 12:** Applies to the MAX9141 only. Comparator is active with  $\overline{LE}$  driven high and is latched with  $\overline{LE}$  driven low ( $V_{OD} = 10mV$ ). See Figure 2.

**Note 13:** Applicable to the MAX9141 only. Comparator is active with the  $\overline{SHDN}$  driven high and is shutdown with  $\overline{SHDN}$  driven low. Shutdown enable time is the delay when the  $\overline{SHDN}$  is driven high to the time the output is valid. Shutdown disable time is the delay when the  $\overline{SHDN}$  is driven low to the time the comparator shuts down.

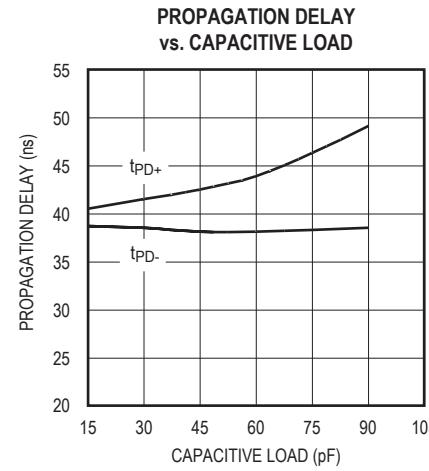
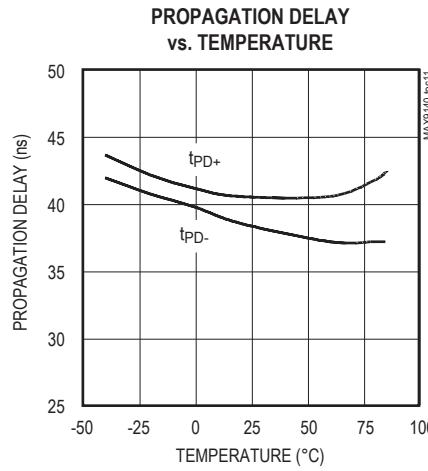
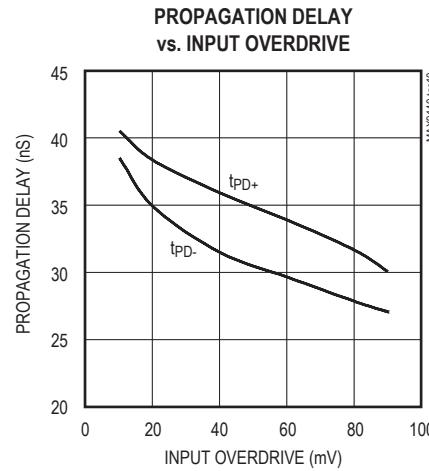
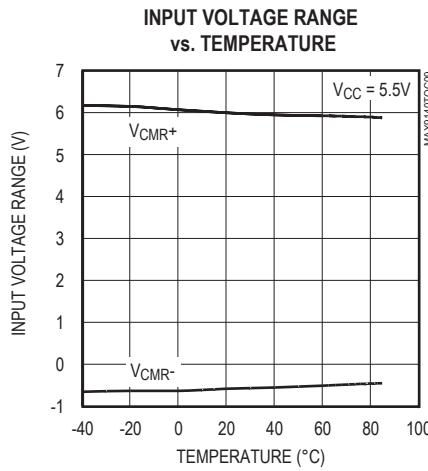
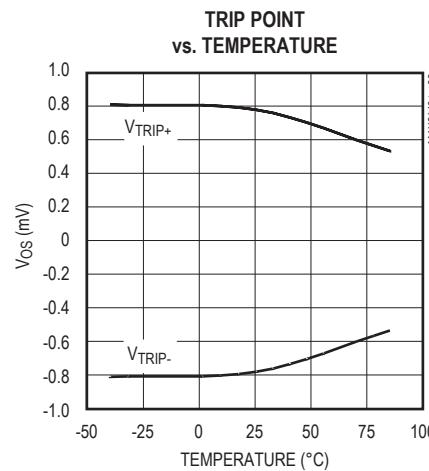
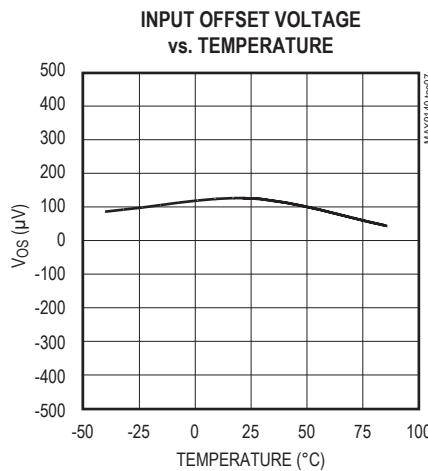
## Typical Operating Characteristics

( $V_{CC} = 3.0\text{V}$ ,  $V_{CM} = 0\text{V}$ ,  $C_L = 15\text{pF}$ ,  $V_{OD} = 10\text{mV}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



### Typical Operating Characteristics (continued)

( $V_{CC} = 3.0\text{V}$ ,  $V_{CM} = 0\text{V}$ ,  $C_L = 15\text{pF}$ ,  $V_{OD} = 10\text{mV}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

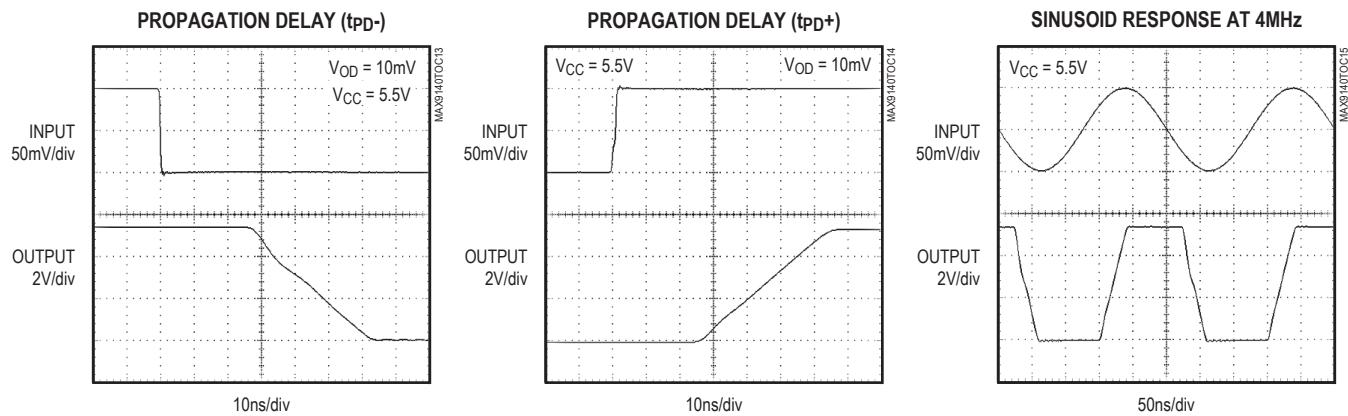


MAX9140/MAX9141/  
MAX9142/MAX9144

# 40ns, Low-Power, 3V/5V, Rail-to-Rail Single-Supply Comparators

## Typical Operating Characteristics (continued)

( $V_{CC} = 3.0\text{V}$ ,  $V_{CM} = 0\text{V}$ ,  $C_L = 15\text{pF}$ ,  $V_{OD} = 10\text{mV}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



## Pin Description

PIN				NAME	FUNCTION
MAX9140	MAX9141	MAX9142	MAX9144		
—	—	1	1	OUTA	Comparator A Output
—	—	2	2	INA-	Comparator A Inverting Input
—	—	3	3	INA+	Comparator A Noninverting Input
5	1	8	4	V <sub>CC</sub>	Positive Supply
—	—	5	5	INB+	Comparator B Noninverting Input
—	—	6	6	INB-	Comparator B Inverting Input
—	—	7	7	OUTB	Comparator B Output
—	—	—	8	OUTC	Comparator C Output
—	—	—	9	INC-	Comparator C Inverting Input
—	—	—	10	INC+	Comparator C Noninverting Input
2	4	4	11	GND	Ground
—	—	—	12	IND+	Comparator D Noninverting Input
—	—	—	13	IND-	Comparator D Inverting Input
—	—	—	14	OUTD	Comparator D Output
3	2	—	—	IN+	Noninverting Input
4	3	—	—	IN-	Inverting Input
—	6	—	—	SHDN	Shutdown: MAX9141 is active when SHDN is driven high; MAX9141 is in shutdown when SHDN is driven low.
—	5	—	—	LE	The output is latched when LE is low. The latch is transparent when LE is high.
1	7	—	—	OUT	Comparator Output
—	8	—	—	N.C.	No Connection. Not internally connected.

## Detailed Description

The MAX9140/MAX9141/MAX9142/MAX9144 single-supply comparators feature internal hysteresis, high speed, and low power. Their outputs are pulled to within 300mV of either supply rail without external pullup or pulldown circuitry. Rail-to-rail input voltage range and low-voltage single-supply operation make these devices ideal for portable equipment. The devices interface directly to CMOS and TTL logic.

Most high-speed comparators oscillate in the linear region because of noise or undesired parasitic feedback. This tends to occur when the voltage on one input is at or equal to the voltage on the other input. To counter the parasitic effects and noise, the devices have an internal hysteresis of 1.5mV.

The hysteresis in a comparator creates two trip points: one for the rising input voltage and one for the falling input voltage (Figure 1). The difference between the trip points is the hysteresis. The average of the trip points is the offset voltage. When the comparator's input voltages are equal, the hysteresis effectively causes one comparator input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. Standard comparators require hysteresis to be added with external resistors. The devices' fixed internal hysteresis eliminates these resistors. To increase hysteresis and noise margin even more, add positive feedback with two resistors as a voltage divider from the output to the noninverting input.

Figure 1 illustrates the case where IN- is fixed and IN+ is varied. If the inputs were reversed, the figure would look the same, except the output would be inverted.

The MAX9141 includes an internal latch that allows storage of comparison results. The LE pin has a high input impedance. If LE is high, the latch is transparent (i.e., the comparator operates as though the latch is not present). The comparator's output state is latched when LE is pulled low (Figure 2).

## Shutdown Mode (MAX9141 Only)

The MAX9141 shuts down when the SHDN pin is low. When shut down, the supply current drops to less than 12 $\mu$ A, and the three-state output becomes high impedance. The SHDN pin has a high-input impedance. Connect SHDN to V<sub>CC</sub> for normal operation. Exit shutdown with LE high (transparent state); otherwise, the output will be indeterminate.

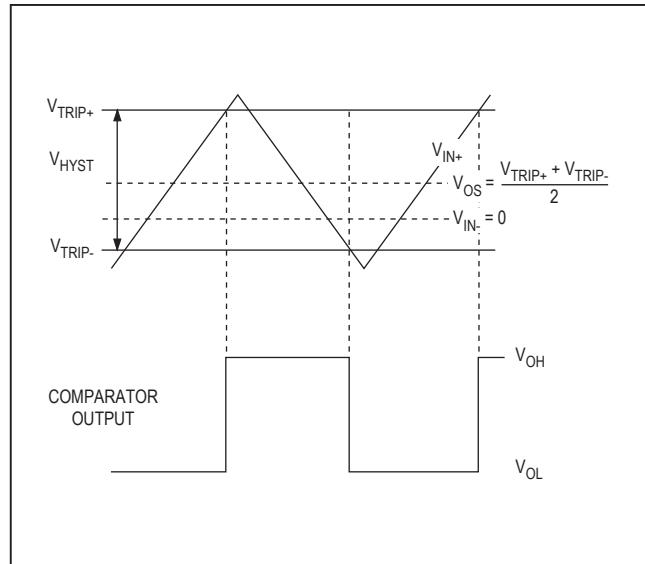


Figure 1. Input and Output Waveform, Noninverting Input Varied

## Input Stage Circuitry

The devices include internal protection circuitry that prevents damage to the precision input stage from large differential input voltages. This protection circuitry consists of two back-to-back diodes between IN+ and IN- as well as two series 4.1k $\Omega$  resistors (Figure 3). The diodes limit the differential voltage applied to the internal circuitry of the comparators to be no more than 2V<sub>F</sub>, where V<sub>F</sub> is the forward voltage drop of the diode (about 0.7V at +25°C).

For a large differential input voltage (exceeding 2V<sub>F</sub>), this protection circuitry increases the input bias current at IN+ (source) and IN- (sink).

$$\text{Input Current} = \frac{(\text{IN}+ - \text{IN}-) - 2V_F}{2 \times 4.1k\Omega}$$

Input current with large differential input voltages should not be confused with input bias current (I<sub>B</sub>). As long as the differential input voltage is less than 2V<sub>F</sub>, this input current is equal to I<sub>B</sub>. The output is in the correct logic state if one or both inputs are within the common-mode range.

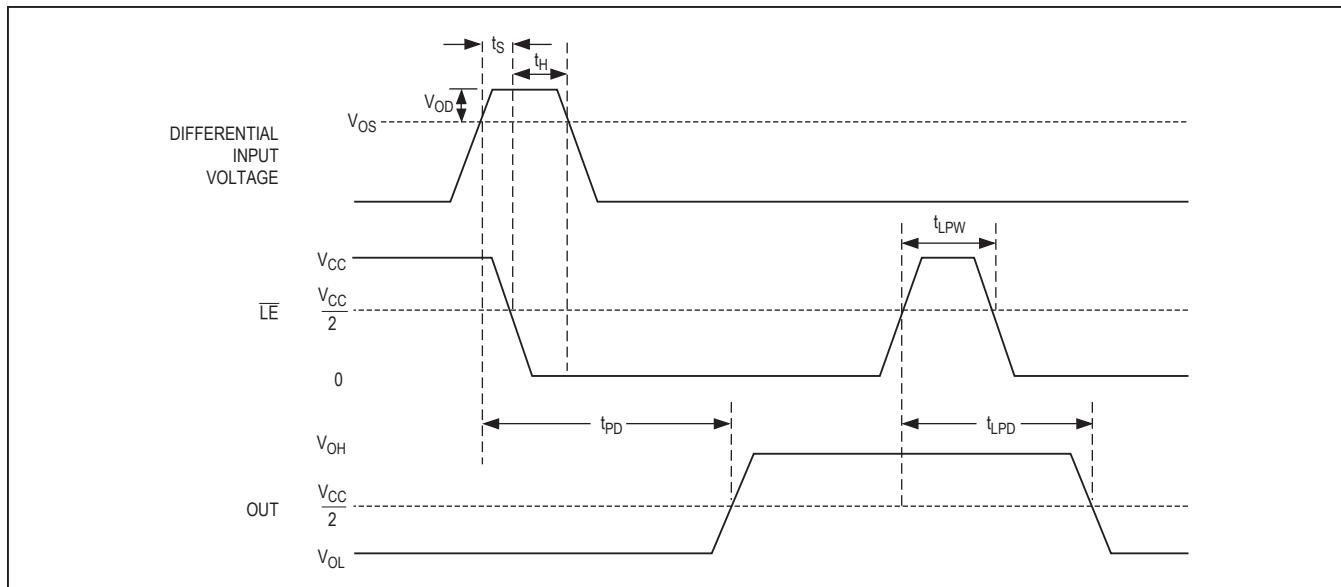


Figure 2. MAX9141 Timing Diagram with Latch Operator

### Output Stage Circuitry

The MAX9140/MAX9141/MAX9142/MAX9144 contain a current-driven output stage as shown in Figure 4. During an output transition,  $I_{SOURCE}$  or  $I_{SINK}$  is pushed or pulled to the output pin. The output source or sink current is high during the transition, creating a rapid slew rate. Once the output voltage reaches  $V_{OH}$  or  $V_{OL}$ , the source or sink current decreases to a small value, capable of maintaining the  $V_{OH}$  or  $V_{OL}$  static condition. This significant decrease in current conserves power after an output transition has occurred.

One consequence of a current-driven output stage is a linear dependence between the slew rate and the load capacitance. A heavy capacitive load will slow down a voltage output transition. This can be useful in noisesensitive applications where fast edges may cause interference.

### Applications Information

#### Circuit Layout and Bypassing

The high-gain bandwidth of the MAX9140/MAX9141/MAX9142/MAX9144 requires design precautions to realize the full high-speed capabilities of these comparators. The recommended precautions are:

- 1) Use a PCB with a good, unbroken, low-inductance ground plane.
- 2) Place a decoupling capacitor (a  $0.1\mu F$  ceramic capacitor is a good choice) as close to  $V_{CC}$  as possible.

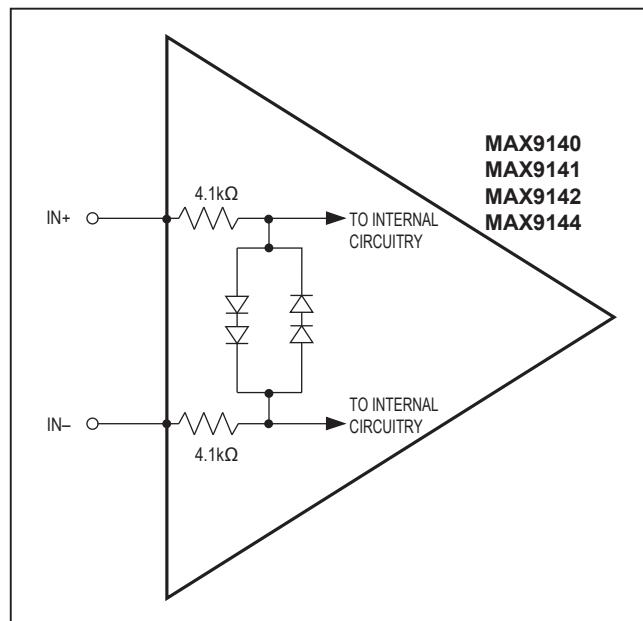


Figure 3. Input Stage Circuitry

- 3) Pay close attention to the decoupling capacitor's bandwidth, keeping leads short.
- 4) On the inputs and outputs, keep lead lengths short to avoid unwanted parasitic feedback around the comparators.
- 5) Solder the device directly to the PCB instead of using a socket.

## MAX9140/MAX9141/ MAX9142/MAX9144

40ns, Low-Power, 3V/5V, Rail-to-Rail  
Single-Supply Comparators

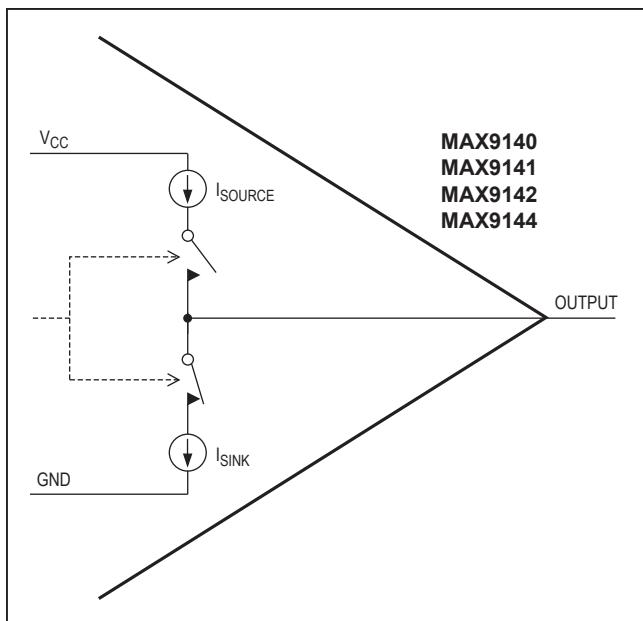


Figure 4. Output Stage Circuitry

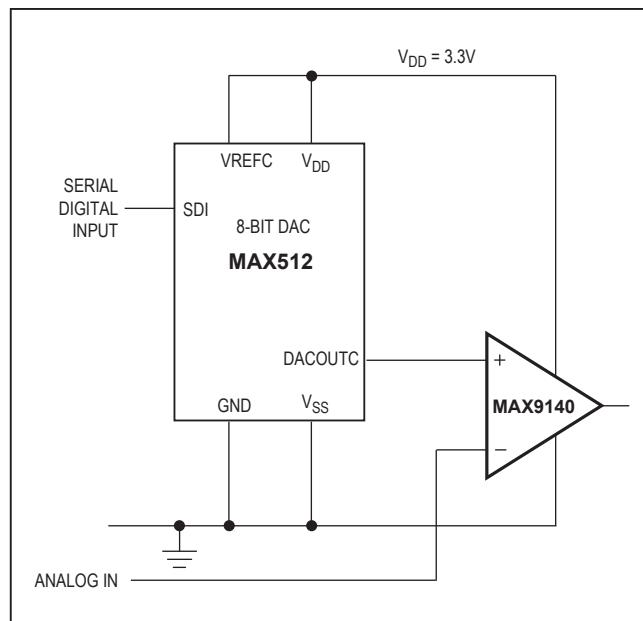


Figure 5. 3.3V Digitally Controlled Threshold Detector

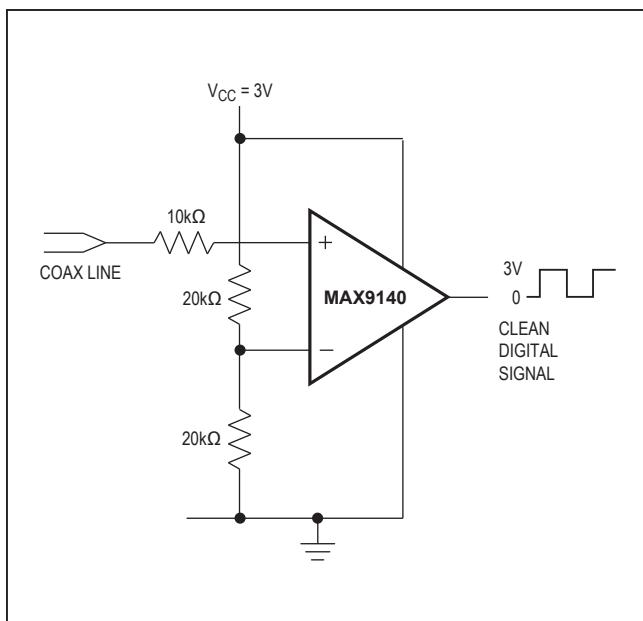


Figure 6. Line Receiver Application

## Chip Information

PROCESS: Bipolar

## Ordering Information

PART*	PIN-PACKAGE	TOP MARK
<b>MAX9140AAUK+T</b>	5 SOT23	+AFEJ
MAX9140AAXK+T	5 SC70	+ASW
MAX9140AAXK/V+T	5 SC70	+AUG
MAX9140EXK-T	5 SC70	ACC
MAX9140EUK-T	5 SOT23	ADQP
<b>MAX9141EKA-T</b>	8 SOT23	AAFD
MAX9141ESA	8 SO	—
<b>MAX9142EKA+</b>	8 SOT23	+AAFE
MAX9142EKA+T	8 SOT23	+AAFE
MAX9142ESA+	8 SO	—
MAX9142ESA+T	8 SO	—
<b>MAX9142EKA-T</b>	8 SOT23	AAFE
MAX9142ESA	8 SO	—
<b>MAX9144EUD</b>	14 TSSOP	—
MAX9144ESD	14 SO	—

**Note:** All E-grade devices are specified over the  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  operating temperature range. All A-grade devices are specified over the  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  operating temperature range.

+Denotes a lead(Pb)-free/RoHS-compliant package.

-Denotes a package containing lead(Pb).

T = Tape and reel.

## Package Information

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.	LAND PATTERN NO.
8 SOT23	K8-5	<a href="#">21-0078</a>	<a href="#">90-0176</a>
5 SOT23	U5-1	<a href="#">21-0057</a>	<a href="#">90-0174</a>
5 SC70	X5+1	<a href="#">21-0076</a>	<a href="#">90-0188</a>
14 TSSOP	U14-1	<a href="#">21-0066</a>	<a href="#">90-0113</a>
8 SO	S8-2	<a href="#">21-0041</a>	<a href="#">90-0096</a>
14 SO	S14-1	<a href="#">21-0041</a>	<a href="#">90-0112</a>

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/01	Initial release	—
1	1/07	Updated <i>Absolute Maximum Ratings</i> with $\pm 20\text{mA}$ current into input pin.	2
2	12/07	Added two new automotive grade products.	1, 2
3	1/10	Added automotive qualified part	1
4	6/14	Added Junction Temperature to <i>Absolute Maximum Ratings</i>	2
5	9/15	Removed MAX9140AAXK/V from <i>Ordering Information</i> and edited the <i>Absolute Maximum Ratings</i>	1, 2
6	10/15	Updated TOC7 and TOC8 in the <i>Typical Operating Characteristics</i> section	6
7	11/17	Added AEC statement to <i>Features</i> section and updated <i>Ordering Information</i> table	1, 9
8	1/19	Removed embedded package outline drawings	10–13
9	10/19	Updated <i>Ordering Information</i>	9

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