4.5V to 42V Input Voltage Range 3.5A Output Current Integrated FET

1ch Buck Converter

BD9G401EFJ-M　BD9G401UEFJ-M

General Description

BD9G401EFJ-M and BD9G401UEFJ-M are buck converters with built-in high side MOSFET. It has an input voltage range of 4.5V to 42V. Current mode architecture provides fast transient response and a simple phase compensation setup.
The IC is mainly used as a secondary side power supply: for example, a step-down output of 3.3V/5V can be produced from voltage power supply such as 12V or 24V. In addition, it has a synchronization function with an external CLK that provides noise management.

Features

- AEC-Q100 Qualified(Note 1)
- Integrated Nch MOSFET
- Synchronizes to external clock 250kHz to 500kHz
- ON/OFF Control through EN Terminal
  (Standby current of 0μA)
- Small package(HTSOP-J8ES)
- LowDrop Out operation

(Note1: Grade 2)

Applications

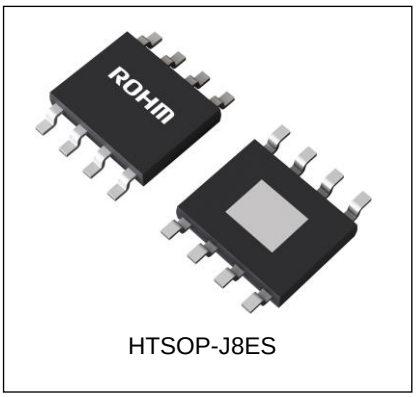
- Consumer devices in general that has 12V / 24V lines
- Automotive applications
  (Audio system, Navigation system, etc)
- Industrial distributed-power applications
- Entertainment equipment

Key Specifications

- Input Voltage：　4.5V to 42V
- Precision Reference voltage　(Ta= 25°C) ±1.5%
  (Ta= -40 to +105°C) ±2.0%
- Max Output Current：　3.5A(Max)
- Operating Temperature：　-40°C to +105°C

Package W (Typ) x D (Typ) x H (Max)

HTSOP-J8ES　4.90mm x 6.00mm x 1.00mm



HTSOP-J8ES

Typical Application Circuit

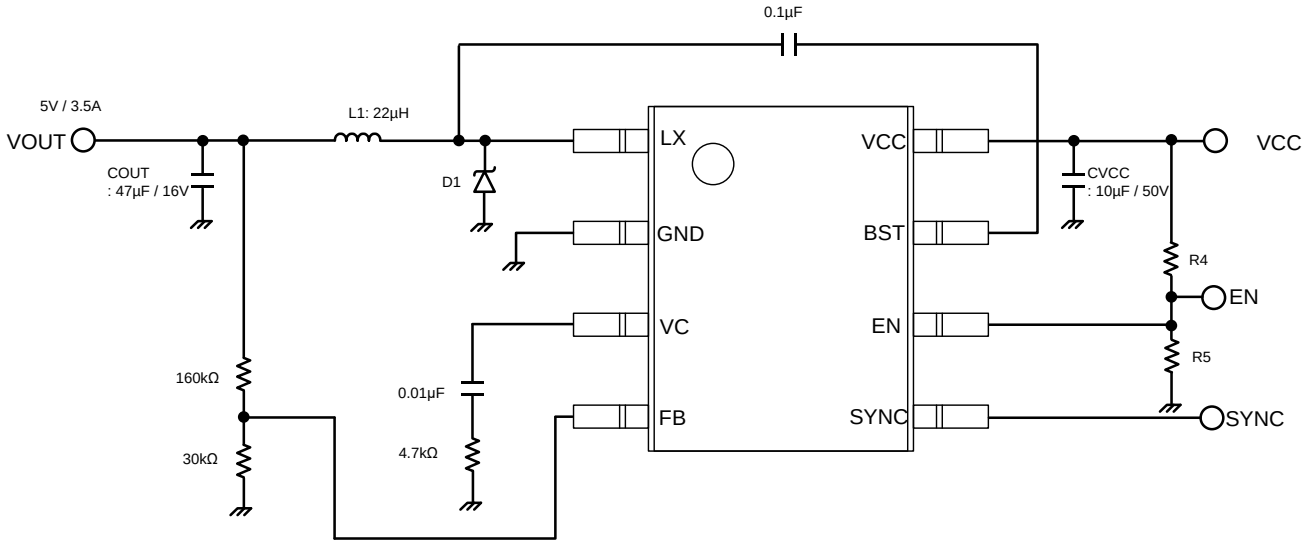


Figure 1. Typical Application Circuit

Pin Configuration

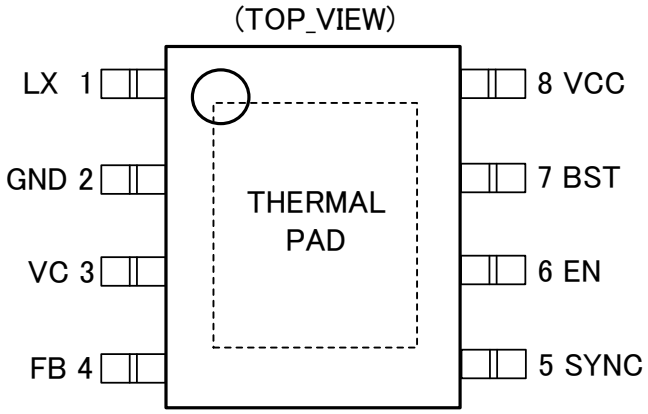


Figure 2. Pin Configuration

Pin Description

Pin No.	Pin Name	Description
1	LX	Switching terminal
2	GND	Ground terminal
3	VC	Error amplifier output terminal
4	FB	Feedback input terminal
5	SYNC	External clock input terminal
6	EN	Enable terminal
7	BST	Terminal for boot-strap capacitor
8	VCC	Input voltage terminal
-	THERMAL PAD	PAD for heat dissipation. Always connect to GND.

Block Diagram

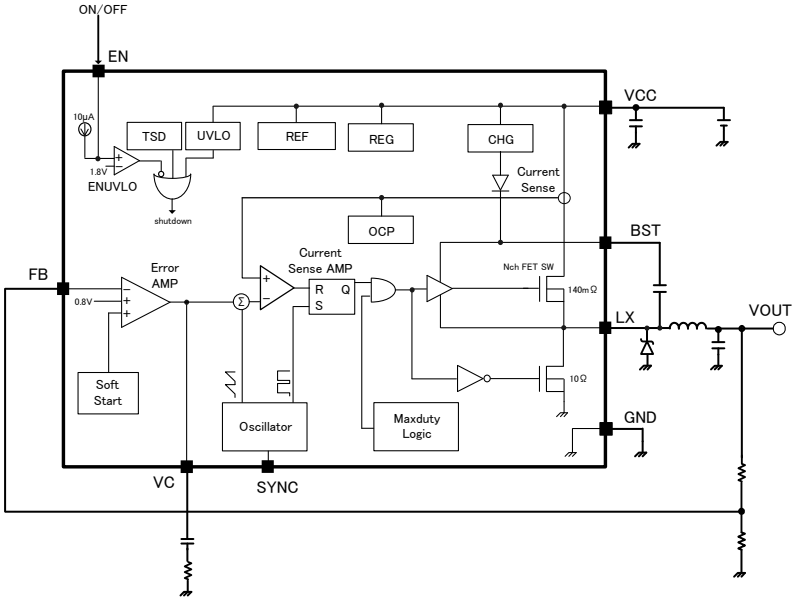


Figure 3. Block Diagram

Description of Blocks

1. REF
   This block generates the reference voltage.

2. REG
   Regulator for internal circuit power supply.

3. CHG
   Regulator for bootstrap capacitor charging.

4. TSD
   Thermal Shutdown Protection Circuit
   When it detects the temperature exceeding Maximum Junction Temperature (Tj= 150°C), it turns off the output FET, and resets SoftStart circuit. It has a hysteresis function. When the temperature is decreased, the chip automatically returns to normal operation.

5. UVLO
   Under Voltage Lock-Out Circuit
   This prevents internal circuit error during increase and decrease of power supply voltage.
   It monitors VCC terminal voltage. When VCC voltage becomes 4.0V (Typ) and below, it turns OFF output FET. SoftStart circuit also resets during this time. This circuit has a hysteresis of 200mV (Typ).

6. ENUVLO
   If the voltage from this terminal is below 0.3V, IC operation is OFF. If it is between 0.3V and 1.4V, internal REG circuit turns ON. If it is greater than 1.8V(Typ), the IC is operational and a hysteresis generation current of 10 μA (Typ) is sourced from the EN terminal. To turn off the IC, source current should be removed.
   When the situation without a signal to control EN terminal at the time of start up is assumed, pull down EN terminal by pull down resistor to prevent becoming the high impedance.
   Arbitrary UVLO is possible by connecting EN terminal to a voltage divider from the input voltage.
   See Detailed Description below.

7. ErrorAMP
   This is an error amplifier circuit that detects the output signal, and outputs PWM control signal.
   Internal reference voltage is set to 0.8V(Typ).

8. SoftStart
   This is a circuit that gently raises the output voltage of the DC / DC converter to prevent in-rush current during start-up.
   SoftStart Time is 8ms (Typ) when the IC operates with the 300 kHz (Typ) internal clock.
   When the IC operates with an external clock, SoftStart Time is changed according to the oscillator frequency.
   See Detailed Description below.

9. Oscillator
   This is a oscillation circuit with an operating frequency fixed to 300 kHz(Typ).
   By inputting external CLK to the SYNC terminal, synchronous operation of 250 kHz to 500 kHz can be achieved.
   See Detailed Description below for synchronous operation.
   When used in self-running mode, please connect SYNC terminal to GND.

10. Current Sense AMP
    This is a voltage - pulse width converter.
    It compares the voltage depending on the current of FET SW through the sum of the error amplifier output voltage and the slope ripple. The output then controls the width of the output pulse and outputs it to the driver.

11. Nch FET SW
    This is a Power Nch MOSFET.
    It should be used within OCP threshold 4.0A(Min) including the DC current and ripple current of the inductor.
    See the Application Components Selection Method below for the calculation of FET maximum current.

12. OCP
    The IC has a pulse-by-pulse over current protection function to protect the FET from over current. When OCP is detected twice sequentially, the device will turn off and restart.
    See the Detailed Description below for OCP function.

13. MaxDuty logic
    When Nch FET SW continues being turned ON in eight successive cycles, the high side FET will be turned off forcibly.
    See the later Detailed Description for LowDrop Out operation.

Absolute Maximum Ratings (Ta= 25°C)

Parameter	Symbol	Limit Rating	Unit
VCC-GND Voltage	VCC	45	V
BST-GND Voltage	VBST	50	V
BST-LX Voltage	VBST-LX	7	V
EN-GND Voltage	VEN	45	V
LX-GND Voltage	VLX	45	V
FB-GND Voltage	VFB	7	V
VC-GND Voltage	VVC	7	V
SYNC-GND Voltage	VSYNC	7	V
Operating Temperature	Topr	-40 to +105	°C
Storage Temperature	Tstg	-55 to +150	°C
Junction Temperature	Tjmax	150	°C

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings

Thermal Resistance(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 3)	2s2p(Note 4)	
HTSOP-J8ES				
Junction to Ambient	θ_{JA}	206.4	45.2	°C/W
Junction to Top Characterization Parameter(Note 2)	Ψ_{JT}	21	13	°C/W

(Note 1)Based on JESD51-2A(Still-Air)
(Note 2)The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3)Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 4)Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 5)	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 5) This thermal via connects with the copper pattern of all layers..

Recommended Operating Ratings (Ta= -40°C to +105°C)

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Power Supply Voltage	VCC	4.5(Note 6)	-	42	V
Output Voltage	VOUT	0.8 (Note 7)	-	VCC (Note 8)	V
Output Current	IOUT	-	-	3.5	A
SYNC Terminal Input Frequency	f_{SYNC}	250	-	500	kHz
Input Capacitance	C_{IN}(Note 9)	2.2	-	-	µF
Inductance	L(Note 10)	11	-	-	µH

(Note 6) Voltage more than 4.65V is necessary for IC start. The IC can work to 4.5V after start.
(Note 7) Restricted by Min On Time 200ns(Max).
(Note 8)Upper limit restricted by MaxDuty.
(Note 9) The capacitance is selected in the range including temperature characteristics and bias voltage effect. Refer to P18.
(Note10)Restricted by output voltage setting. Refer to P17.

Electrical Characteristics (Unless otherwise specified: Ta= 25°C, VCC= 12V, EN= 3V)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Circuit Current						
VCC Standby Current	I_{st}	−	0	10	μA	V_{EN}= 0V
VCC Circuit Current	I_{cc}	−	1.2	2.4	mA	V_{FB}= 1.2V
Under Voltage Lock Out (UVLO)						
Detect Voltage	V_{uv}	3.65	4.00	4.35	V	VCC down sweep
Hysteresis Width	V_{uvhy}	50	200	300	mV	
Oscillator						
Oscillator Frequency	f_{osc}	270	300	330	kHz	
MaxDuty Cycle	D_{max}	95.0	97.0	99.9	%	V_{SYNC}= 0V
Error Amp						
FB Threshold Voltage	V_{FB}	0.788	0.800	0.812	V	Ta= 25°C
	V_{FBT}	0.784	0.800	0.816	V	Ta= -40 to +105°C
Input Bias Current	I_{FB}	-1.0	0	+1.0	μA	V_{FB}= 3.0V
FB Leak Current	I_{leak}	-1.0	0	+1.0	μA	V_{FB}= 0V
SoftStart Time	t_{soft}	5.6	8.0	10.4	ms	V_{SYNC}= 0V
Output						
LX NMOS ON Resistance	R_{onH}	−	140	−	mΩ	
LX Precharge NMOS ON Resistance	R_{onL}	−	10	−	Ω	
Over Current Detect	I_{ocp}	4	6	−	A	
CTL						
EN Terminal Internal REG ON-Voltage	V_{ENON}	0.3	−	1.4	V	
EN Terminal IC Output on Threshold	V_{ENUV}	1.65	1.80	1.95	V	IC on or off threshold
EN Terminal Source Current	I_{EN}	9.0	10.0	11.0	μA	V_{EN}= 3V
SYNC						
SYNC Terminal Control Voltage High	V_{SYNCH}	2.0	−	5.5	V	
SYNC Terminal Control Voltage Low	V_{SYNCL}	-0.3	−	+0.8	V	
SYNC Terminal Input Current	I_{SYNC}	6	12	24	μA	V_{SYNC}= 3V

Detailed Description

External CLK for SYNC Function

The SYNC terminal can be used to synchronize the regulator to an external system clock(250kHz to 500kHz). To implement the synchronization feature, connect a square wave to SYNC terminal. The square wave amplitude must have transition lower than 0.8V and higher than 2.0V on the SYNC terminal and have an ON and OFF time greater than 100ns. The synchronization frequency range is 250 kHz to 500 kHz. The rising edge of the LX will be synchronized to the falling edge of SYNC terminal signal after 3 SYNC input pulse count. During synchronization and the external clock is removed, the device transitions to self-running mode after 7 µs.

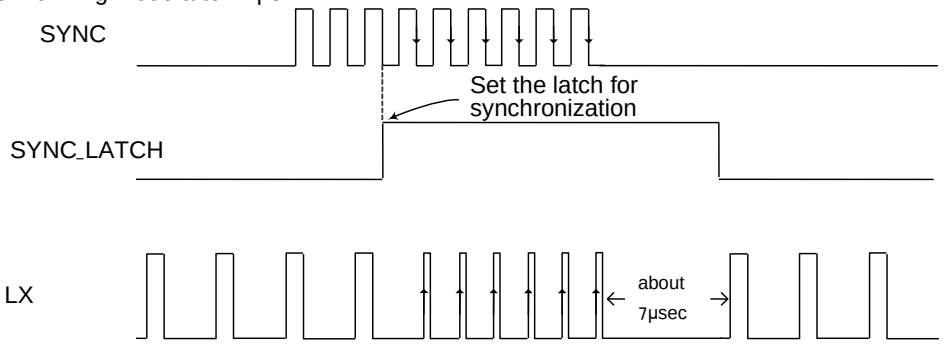


Figure 4. Frequency Synchronization Function Timing Chart

In the Case of not Using the Synchronization Function

Although the SYNC terminal is internally pulled down by a resistor, it is recommended to connect SYNC terminal to ground if the synchronization function is not in use.

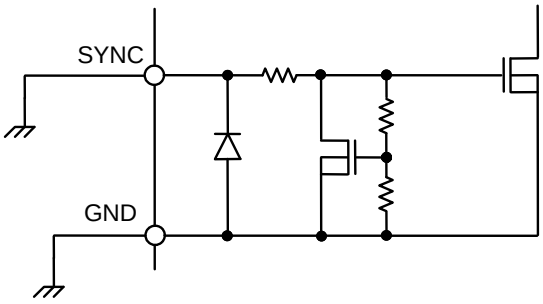


Figure 5. Circuit Diagram of SYNC Terminal Not in Use

SoftStart

The SoftStart Time is determined by the DC / DC operating frequency.
If synchronization is used at the time EN=ON, SoftStart Time is restricted by SYNC terminal input pulse frequency.
SYNC terminal input pulse frequency is fosc_ex . The SoftStart Time is expressed by the equation below.

$$t_{Soft} = \frac{300}{fosc\_ex} \times 8\,[\mathrm{msec}]$$

Where:
t_{soft} is the SoftStart time [msec],
fosc_ex is the external clock [khz]

Detailed Description - Continued

OCP Operation

IC has built-in over current protection (OCP) for protecting the FET.
When OCP is detected twice sequentially, the IC is turned off and after 4000 counts of running CLK frequency, the IC turns ON.
In the case that the synchronization function is not used, it becomes 13ms at operating frequency 300 kHz.

When using synchronization function, latch stop time is determined by the external CLK frequency through the following expression.

$$T_{ocp} = \frac{1}{fosc\_ex} \times 4000 \quad [\mathrm{msec}]$$

Where:
T_{ocp} is the Latch stop time [msec]
fosc_ex is the external CLK frequency [kHz]

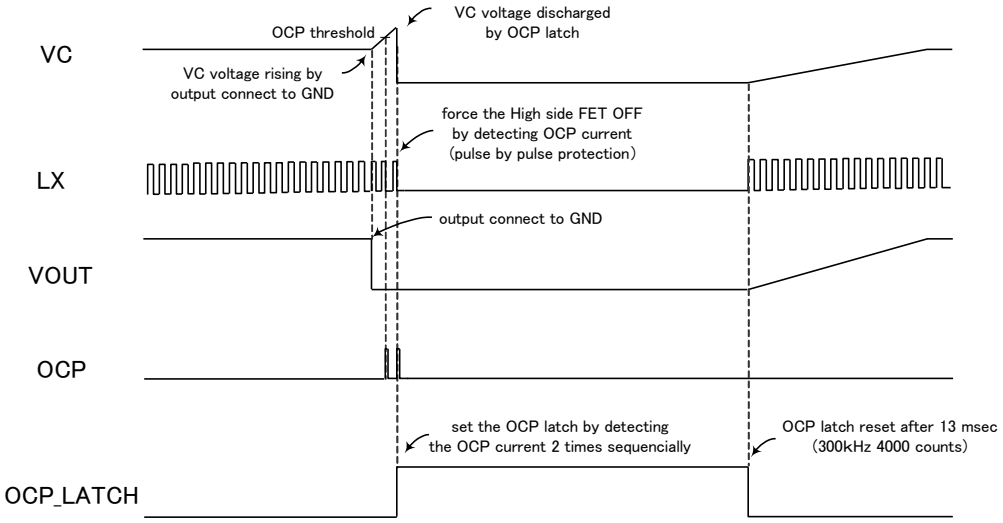


Figure 6. Timing Chart at OCP Operation

External UVLO Setting

The high precision reset function is built in at the EN terminal and arbitrary low-voltage malfunction prevention is possible by connecting EN terminal to a voltage divider from the input voltage.
If in use, please set R4 and R5 to arbitrary voltage of IC turned on (V_{start}) and turned off (V_{stop}) through the expression below.

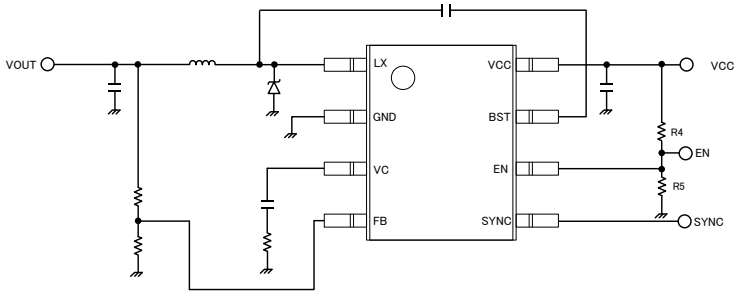


Figure 7. External UVLO Setup

$$R_4 = \frac{V_{start} - V_{stop}}{IEN} \quad [\Omega]$$

$$R_5 = \frac{VEN \times R_4}{V_{start} - VEN} \quad [\Omega]$$

IEN: EN terminal source current 10μA (Typ) VEN: EN terminal output on threshold 1.8V (Typ)
As for the example above, when VCC voltage at which the IC turns on is 15V and turns off at 14V, R4 would be 100 kΩ and R5 would be 13.6 kΩ for the voltage divider network in the diagram.

Detailed Description - Continued

The countermeasure of voltage generation over output voltage in less than 4.9 V output voltage application

IC produces at most 100μA to the output via LX from BST which is internal regulator at the following condition

Output of IC can generate at most 4.9V from BST voltage, so according to output voltage setting, output voltage is Greater than setting output voltage.
In order to prevent generation of output voltage that is over setting output voltage, fewer than 4.9 output voltage application need to attach over 100μA load in output.
Set a resistance level that feedback resister of output generate more than 100μA.
In addition, it is feasible to attach output over 100μA feedback resister.

[Conditions]
IC internal regulator is operating when switching is no operation.
For example, input voltage is less than internal UVLO threshold, EN terminal voltage is condition of internal REG ON.

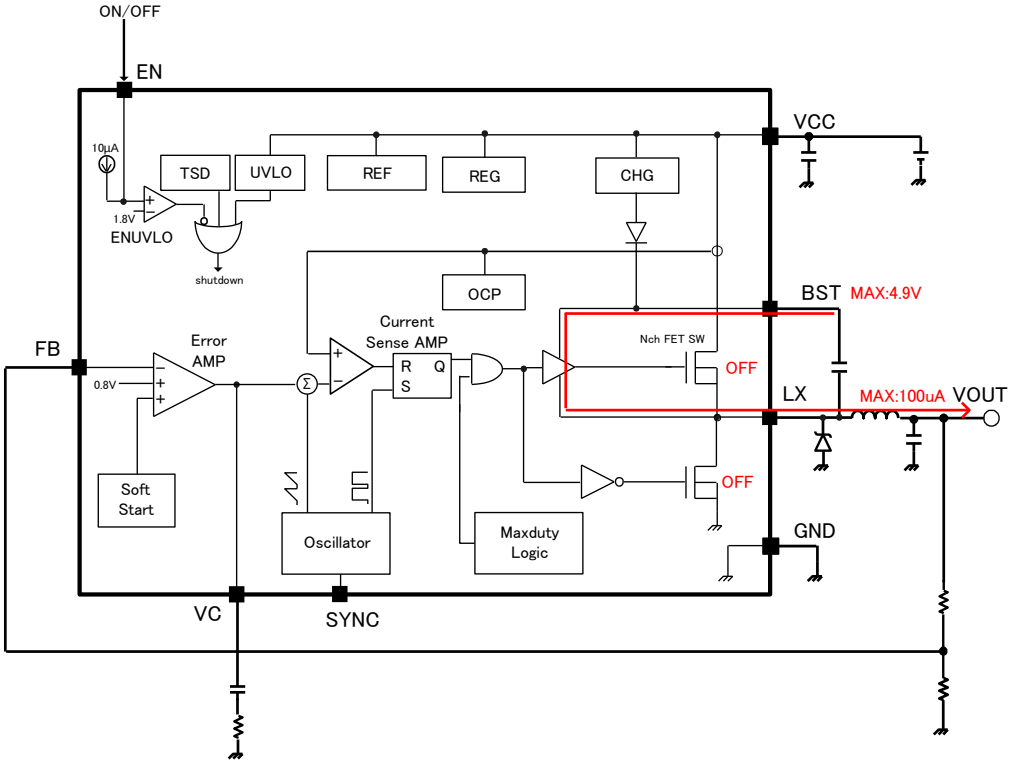


Figure 8. Current Path at the Time of the SW off and Internal REG ON

Detailed Description - Continued

LowDrop Out Operation

For the BST terminal charge that is the drive voltage of the High-side Nch FET, input and output limit is set by MaxDuty.
The IC has two operation modes: Steady operation mode and MaxDuty mode, to cope with wide duty output.
When the IC is in steady operation mode, FET is switching every period. When the IC is in MaxDuty mode, after ON pulse up to eight periods, FET is forced off in 700ns.

Operation Duty is calculated as follows by input and output voltage to use and a load.

$$Don = \frac{VOUT}{VCC - R_{onH} \times IOUT} \times 100 \quad [\%]$$

MaxDuty is calculated as follows by forced-off time (Typ: 300ns) and operating frequency.

$$Don\_\max = (1 - 300n \times f_{osc}) \times 100 \quad [\%]$$

In the case of 300 kHz operating frequency where the SYNC terminal is not used, MaxDuty for steady operation is 91%.
If duty requirement is beyond this level, then shift to MaxDuty mode.

During MaxDuty mode, the IC is enabled to output 100% duty for 8 periods of internal clock and a forced-off section of 700nsec exists.
MaxDuty in the MaxDuty mode is expressed by the following equation.

$$Don\_\max 2 = \left(1 - \frac{700n \times f_{osc}}{8}\right) \times 100 \quad [\%]$$

In MaxDuty mode, switching operation does not occur every period, so the inductor ripple current and output ripple voltage become bigger than steady operation.
Output voltage drops in the case of duty is higher than Don_max2.

MinDuty

There are output voltage restrictions by MinDuty.
The MinDuty required is as follows with worst min on time (200nsec).

$$Don\_\min = (200n \times f_{osc}) \times 100 \quad [\%]$$

Heat generation for the Light-Load

For the light-load, Nch FET of 10Ω in this IC pulls out charge into GND, and BST capacitor is charged.
When Nch FET pulls out charge, this IC has a loss by ON resistance 10Ω of Nch FET and the flowing current.
The loss and heat generation may be increased with the condition of high input voltage, high output voltage and low inductance value. Confirmation of efficiency and heat generation for the light-load is recommended.
When the heat generation for the light-load rises high, high inductance value is recommended.
The heat generation is decreased by dropping down the ripple current.

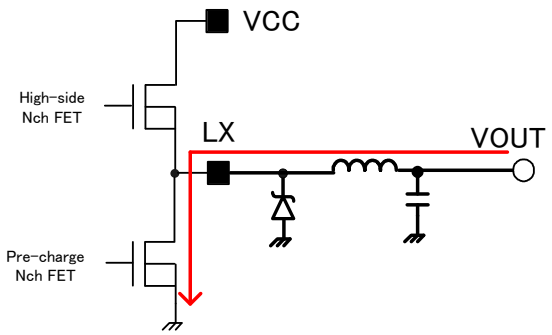


Figure 9. Current Passes at The Time of Light-Load

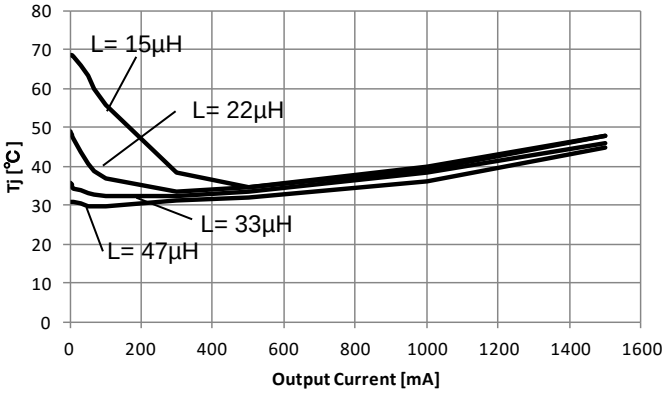


Figure 10. Junction Temperature vs Output Current
(VCC =24V, Vout= 12V)
(Rohm Board (4layers 40mm x 40mm))

Performance Curves (Reference data)
(Unless Otherwise Specified, Ta= 25°C, VCC= 12V)

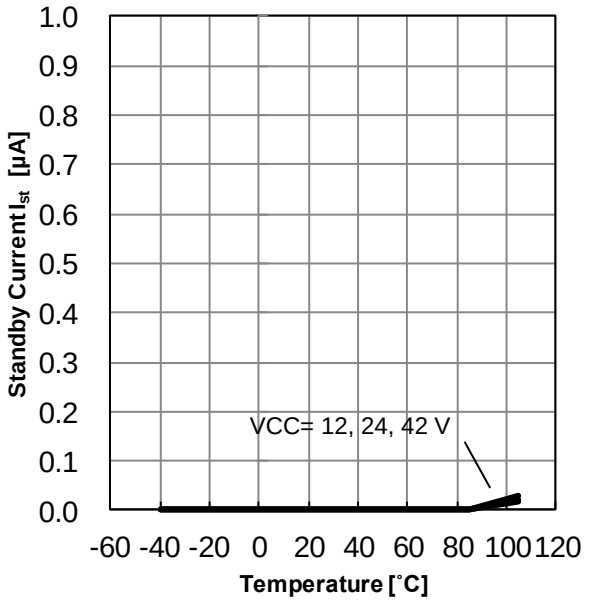


Figure 11. Standby Current vs Temperature

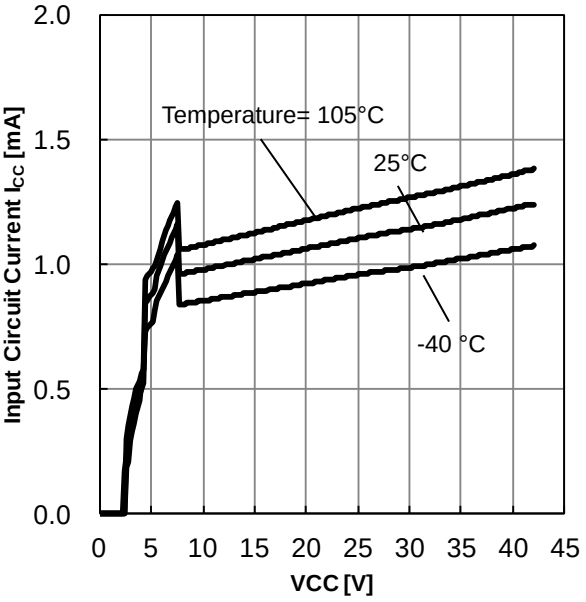


Figure 12. Input Circuit Current vs Input Voltage (V_{FB}= 1.2V)

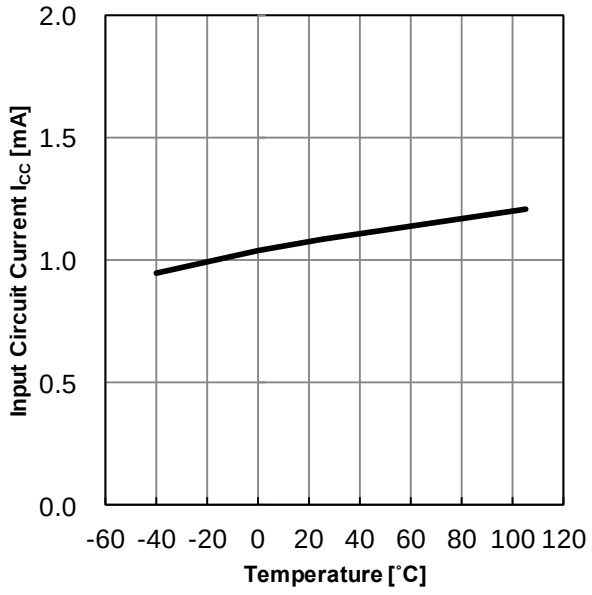


Figure 13. Input Circuit Current vs Temperature (V_{FB}= 1.2V)

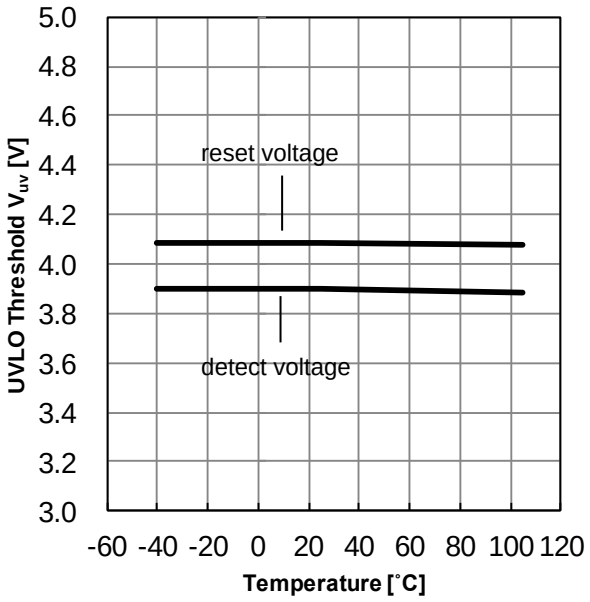


Figure 14. UVLO Threshold vs Temperature

Performance Curves (Reference data) - Continued

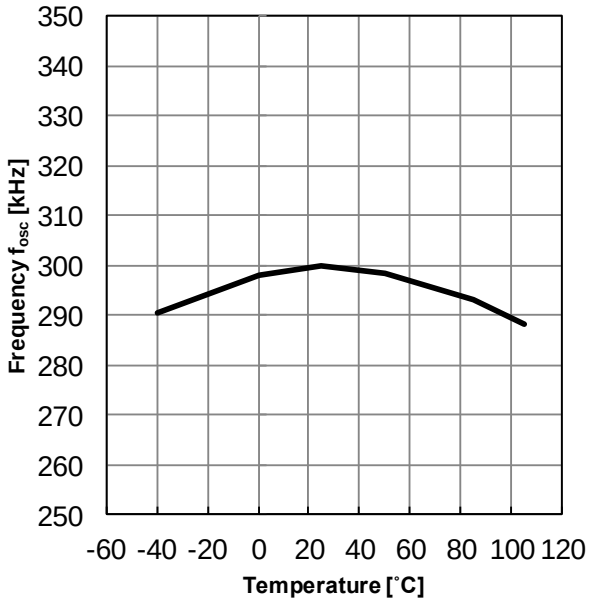


Figure 15. Frequency vs Temperature

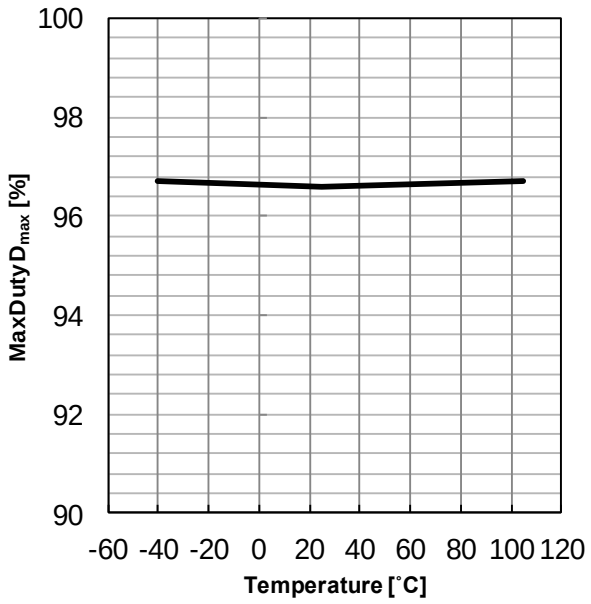


Figure 16. MaxDuty vs Temperature

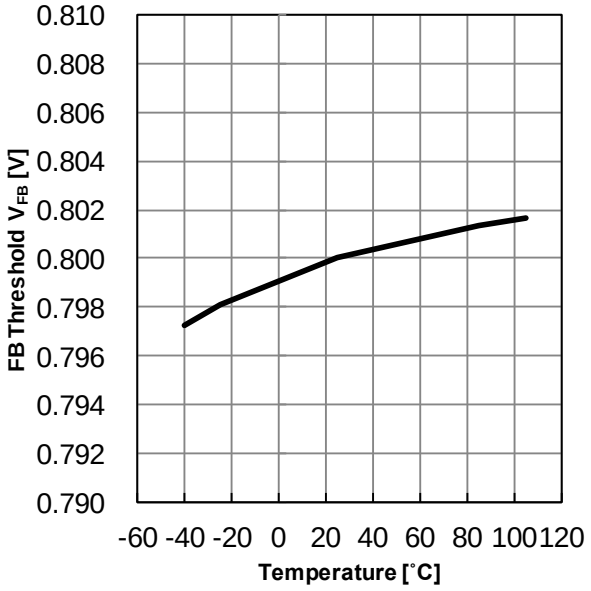


Figure 17. FB Threshold vs Temperature

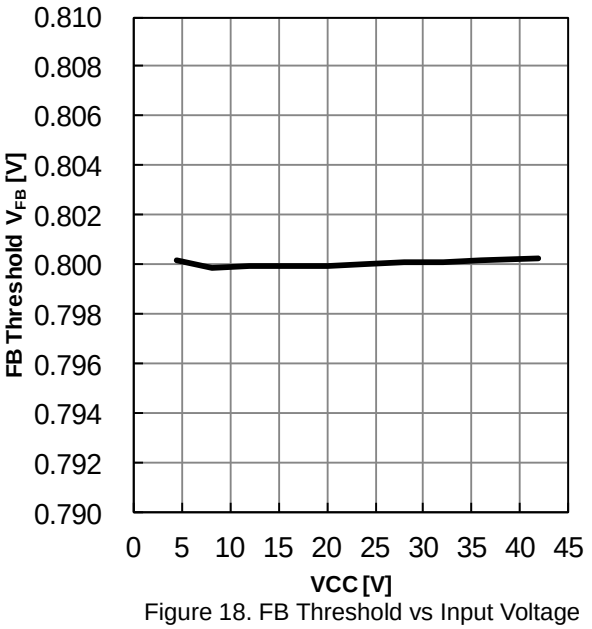


Figure 18. FB Threshold vs Input Voltage

Performance Curves (Reference data) - Continued

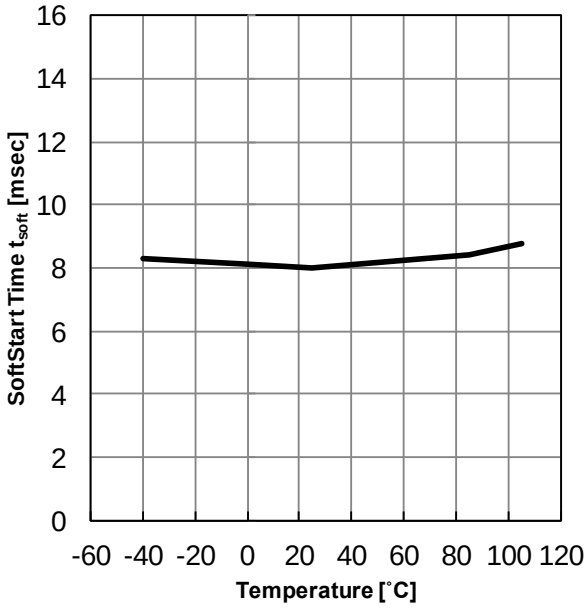


Figure 19. Soft Start Time vs Temperature

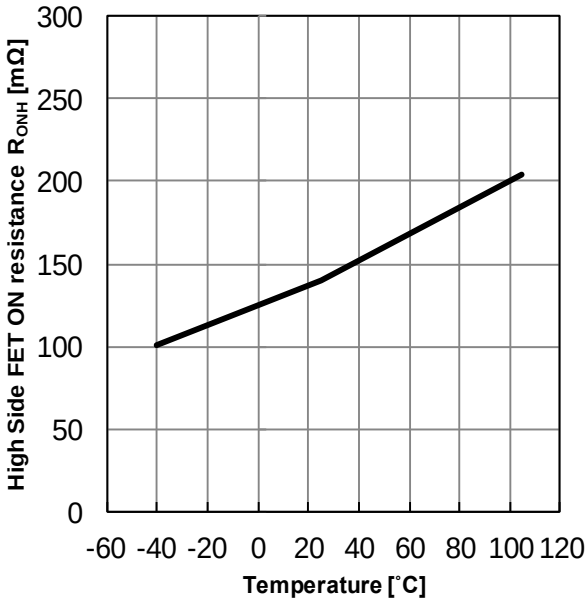


Figure 20. High Side FET R_{ON} vs Temperature

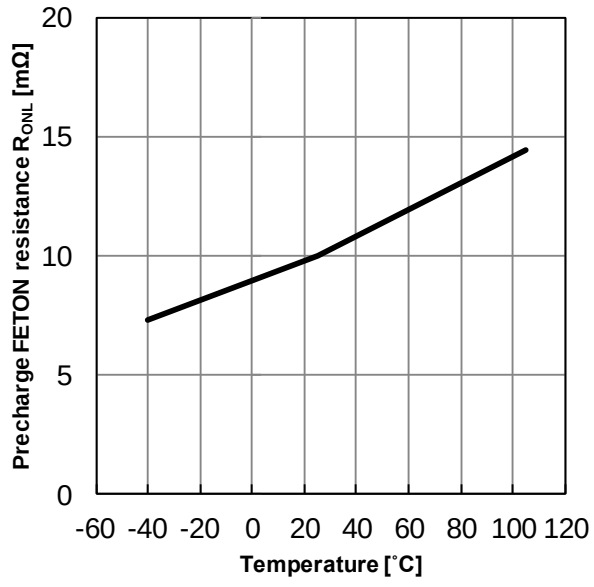


Figure 21. Precharge FET R_{ON} vs Temperature

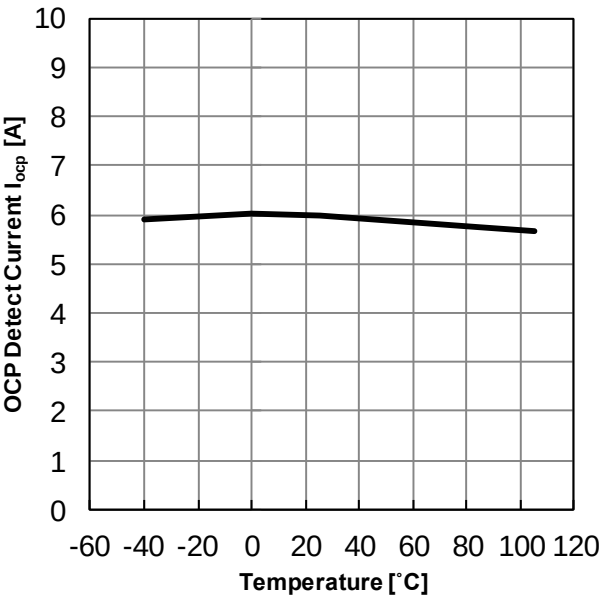


Figure 22. OCP Detect Current vs Temperature

Performance Curves(Reference data) – Continued

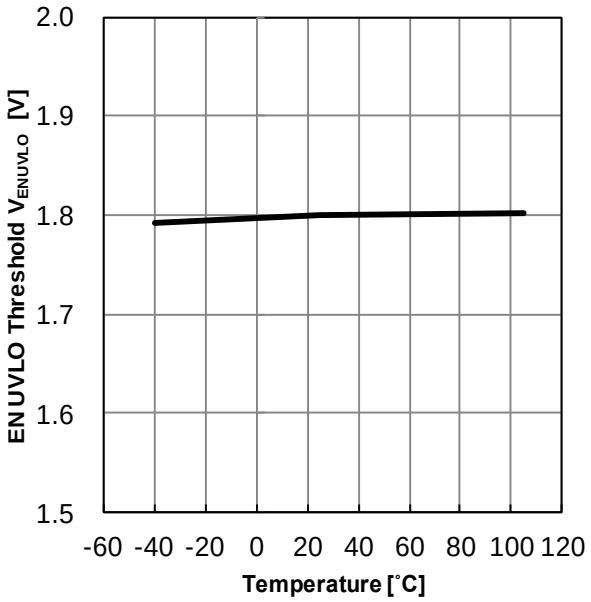


Figure 23. ENUVLO Threshold vs Temperature

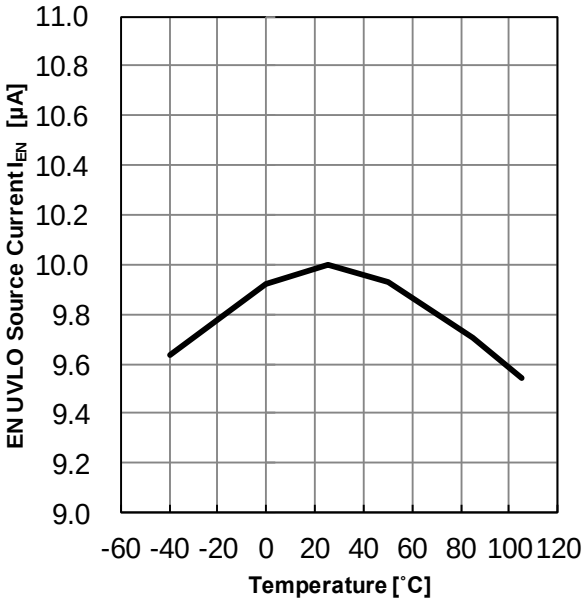


Figure 24. EN Source Current vs Temperature

Reference Characteristics of Typical Application Circuits

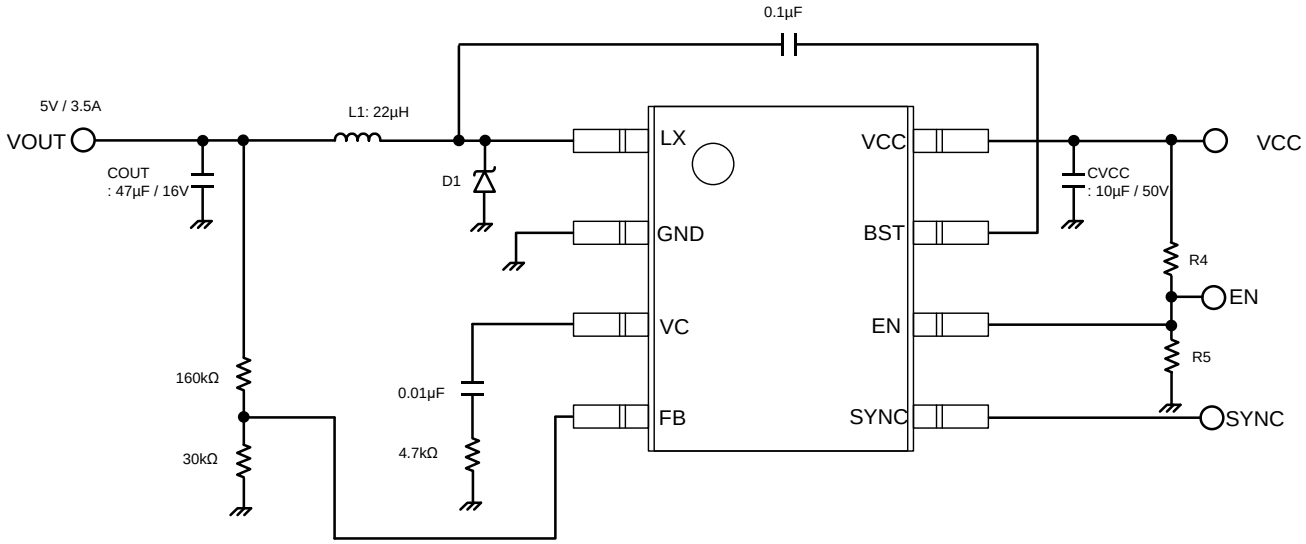


Figure 25. Typical Application Circuits

Parts :	L1	: TDK	CLF12577NIT - 220M	22µH
	CVCC	: murata	GRM32ER71H106K	10µF / 50V
	COUT	: murata	GRM32EB31C476K	47µF / 16V
	D1	: Rohm	RB050L-60	

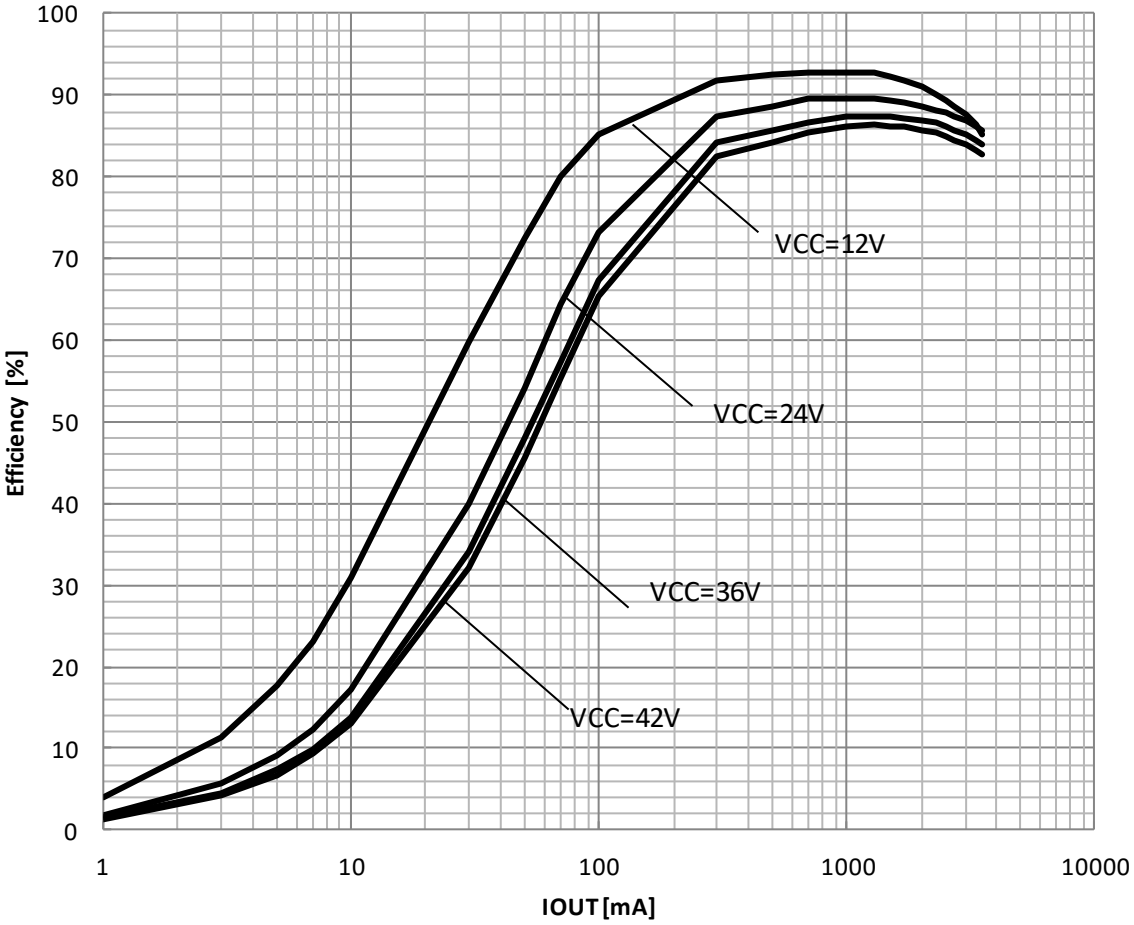


Figure 26. Efficiency vs IOUT

Reference Characteristics of Typical Application Circuits - Continued

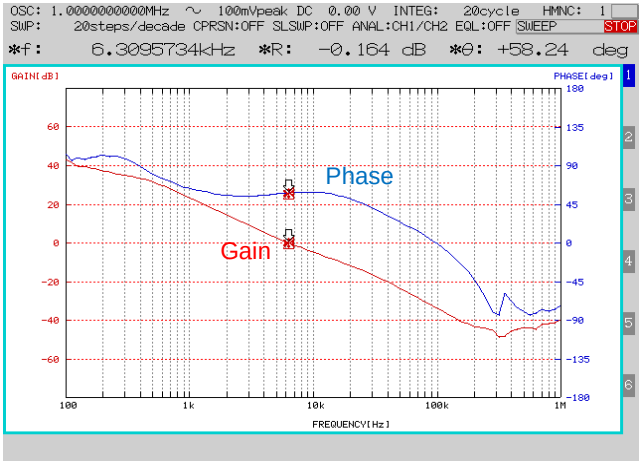


Figure 27. Frequency Characteristics (IOUT= 0.5A)

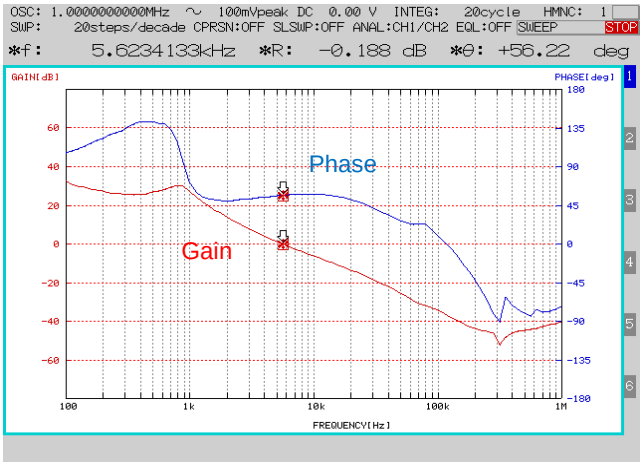


Figure 28. Frequency Characteristics (IOUT= 3.5A)

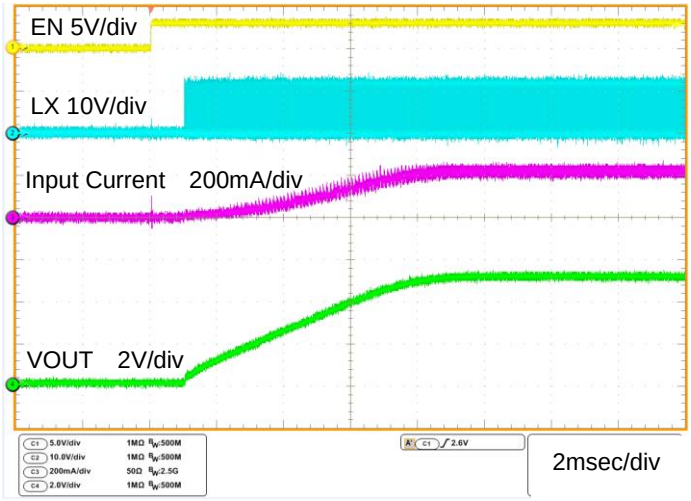


Figure 29. Startup Waveform (IOUT= 0.5A)

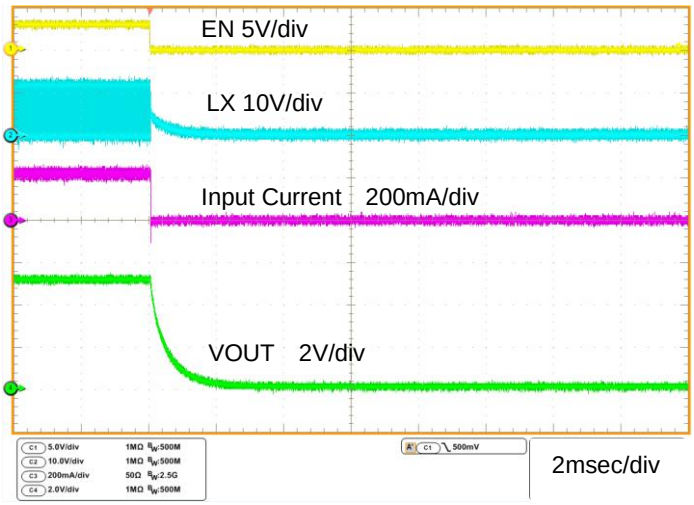


Figure 30. Shutdown Waveform (IOUT= 0.5A)

Application Components Selecting Method

(1) Inductor

Shielded type that meets the current rating (current value from the Ipeak below), with low DCR (Direct Current Resistance element) is recommended.
The value of inductor has an effect in the inductor ripple current which causes the output ripple.
In the same formula below, this ripple current can be made small with a large value L of the coil or as high as the switching frequency.

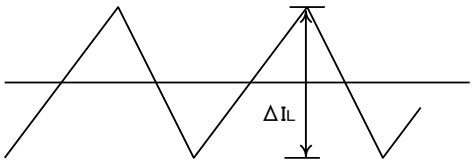


Figure 31. Inductor Current

$$Ipeak = Iout + \frac{\Delta IL}{2} \quad [A] \quad (1)$$

$$\Delta IL = \frac{Vin - Vout}{L} \times \frac{Vout}{Vin} \times \frac{1}{f} \quad [A] \quad (2)$$

Where:

ΔIL is the Inductor ripple current, f is switching frequency

For design value of inductor ripple current, please carry out design tentatively with about 20% to 50% of the maximum output current of the IC.
The minimum value of inductance is shown in the following figure. Inductor is selected over the value of the graph.

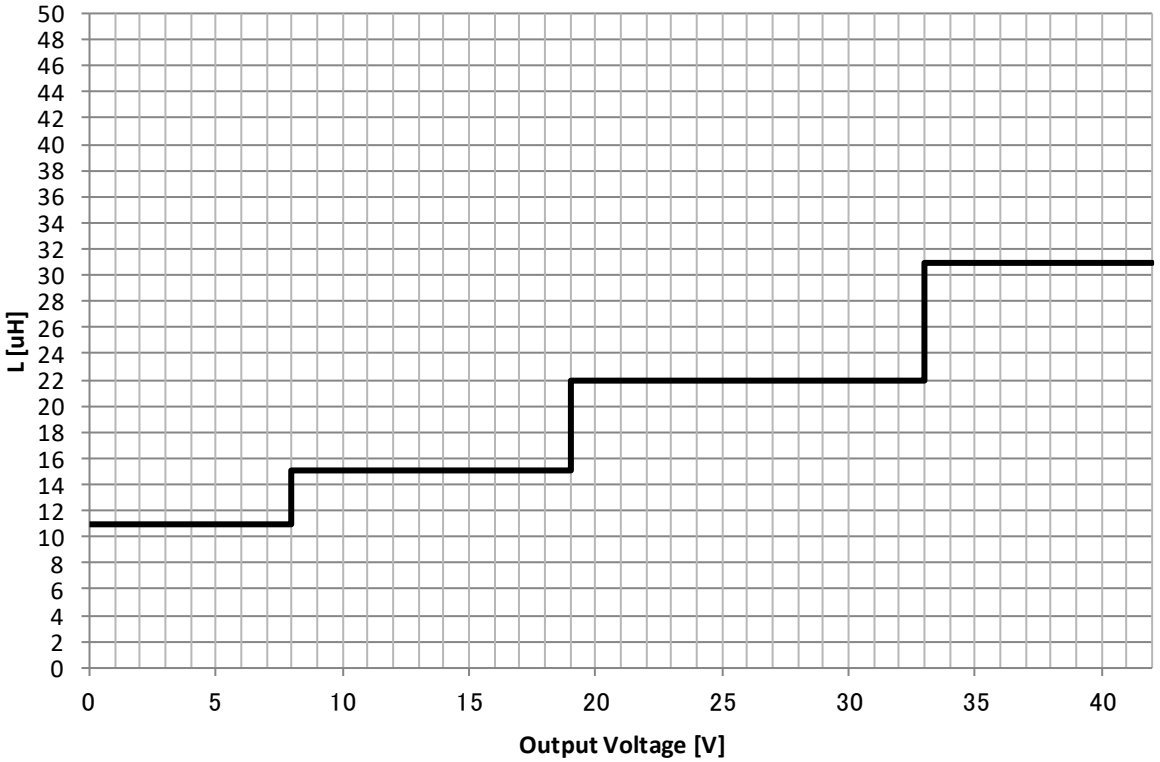


Figure 32. Output Voltage vs inductance (min)

When current that exceeds the inductor rating flows in to the inductor, the inductor causes a magnetic saturation which in turn causes a decline in efficiency and output oscillation. Please choose a inductor with a sufficient margin so that peak current does not exceed rating current of the inductor .

Application Components Selecting Method - Continued

(2) Input Capacitor

This IC needs an input decoupling capacitor. It is recommended a low ESR ceramic capacitor over 2.2μF.
The capacitance is selected considering temperature characteristics and bias voltage effect.
The input ripple voltage is determined by input capacitance (CIN). Because the IC input voltage is decreased, consider input voltage range including ripple voltage. The input ripple voltage is estimated by the following.

$$\Delta Vin = \frac{IOUT_{(max)} \times VOUT}{CIN \times f \times VCC} + (IOUT_{(max)} \times RESR_{(max)}) \quad [V_{p\text{-}p}] \quad (3)$$

Please notice that frequency is 1/8 times in maxduty mode when the difference between input voltage and output voltage is small. Please refer to Detailed Description for the condition of maxduty mode.
The input capacitance has a sufficient value that keep input voltage in the recommended range.

Please confirm the characteristic of RMS ripple current – temperature.
RMS ripple current (I_{RMS}) is following.

$$I_{RMS} \approx IOUT \times \sqrt{\frac{VOUT}{VIN} \times \left(1 - \frac{VOUT}{VIN}\right)} \quad [A_{RMS}] \quad (4)$$

I_{RMS} has a maximum value when VIN = 2 x VOUT

$$I_{RMS} \approx \frac{IOUT}{2} \quad [A_{RMS}] \quad (5)$$

Choose an input capacitor that have enough temperature margin at the I_{RMS}.

(3) Output Capacitor

In order to reduce output ripple, a ceramic capacitor of low ESR is recommended.
Also, for capacitor rating, take into consideration the DC bias characteristics. Use a capacitor with maximum rating of sufficient margin with respect to the output voltage.
Output ripple voltage is obtained through the following formula.

$$Vpp = \Delta IL \times \frac{1}{2\pi \times f \times COUT} + \Delta IL \times R_{ESR} \quad [V] \quad (6)$$

Please set the value within allowable ripple voltage.

Confirm rush current(I_{rush}) of the start up because the output capacitance has an effect of I_{rush}.
I_{rush} is estimated in the following.

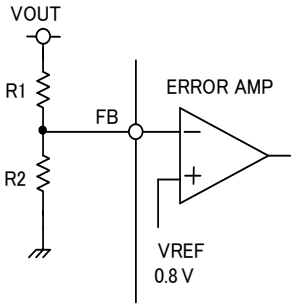
$$I_{rush} > \frac{COUT \times VOUT \times f_{osc\_ex}}{T_{softstart} \times f_{osc}} + \Delta IL + IOUT_{start} \quad [A] \quad (7)$$

Where:
$T_{softstart}$ is soft start time f_{osc} is inner frequency 300kHz
f_{osc_ex} is SYNC frequency (If the SYNC function is not used, f_{osc_ex} equals to f_{osc})
$IOUT_{start}$ is output current when IC is start up.
At least, It is required that I_{rush} is less than 4A that is minimum value of OCP threshold.
The rush current is added the current caused by ERROR AMP delay actually.
Please confirm that start up rush current is lower than 4A.

Application Components Selecting Method - Continued

(4) Output Voltage Setting

The ERROR AMP internal reference voltage is 0.8V. Output voltage is determined by next formula.



$$VOUT = \frac{(R1 + R2)}{R2} \times 0.8\ [V] \quad (8)$$

Figure 33. Voltage feed back Resistance Setting Method

(5) Bootstrap Capacitor

Please connect a 0.1µF (Ceramic Capacitor) between BST and LX terminal.
Because the rating between BST-LX becomes 7V, as for the proof pressure, 10V or more are recommended.

(6) About the adjustment of DC / DC Converter Frequency Characteristics

Role of phase compensation element C1, C2, R3

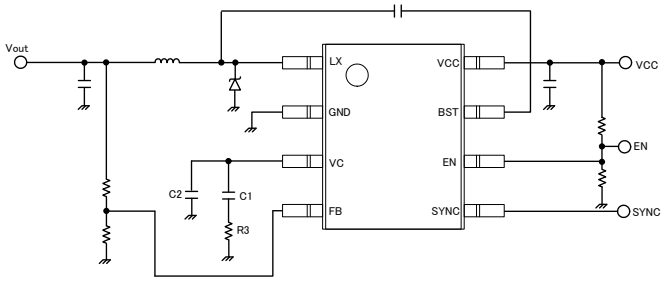


Figure 34. Phase Compensation Element

Stability and responsiveness of the loop are controlled through the VC terminal which is the output of the error amplifer. The combination of zero and pole that determines the stability and responsiveness is adjusted through the combination of resistor and capacitor connected in series to the VC terminal.

The DC Gain of the Voltage feed back Loop can be calculated using the following formula.

$$Adc = RI \times G_{CS} \times A_{EA} \times \frac{V_{FB}}{Vout}$$

Here, V_{FB} is the Feedback Voltage (0.8V). A_{EA} is the Voltage Gain of Error amplifier (Typ: 80dB),
G_{CS} is the Trans-conductance of Current Detect (Typ: 10A / V), and RI is the Output Load Resistance value.

There are 2 important poles in the control loop of this DC / DC.
The first occurs in the output resistance of phase compensation capacitor (C1) and error amplifier, the other one occurs in the output capacitor and load Resistor.
These poles appear in the frequency written below.

$$fp1 = \frac{G_{EA}}{2\pi \times C1 \times A_{EA}}$$

$$fp2 = \frac{1}{2\pi \times COUT \times RI}$$

Here, G_{EA} is the trans-conductance of Error amplifier (Typ: 220µA / V).

In this control loop, one zero becomes important. With the zero which occurs because of phase compensation capacitor C1 and phase compensation resistor R3, the frequency as shown below appears.

Application Components Selecting Method - Continued

$$fz1 = \frac{1}{2\pi \times C1 \times R3}$$

Also, if in this control loop the output capacitor is large, and that the ESR (RESR) is also large, there are cases when it has an important, separate zero (ESR zero).
This ESR zero that occurs due to ESR of output capacitor and its capacitance can be calculated as follows.

$$f_{ZESR} = \frac{1}{2\pi \times COUT \times RESR} \quad \text{(ESR zero)}$$

In this case, the 3rd pole is determined with the 2nd phase compensation capacitor (C2) and phase correction resistor (R3) is used in order to correct the ESR zero results in the loop gain.
This pole exists in the frequency shown below.

$$fp3 = \frac{1}{2\pi \times C2 \times R3} \quad \text{(Pole that corrects ESR zero)}$$

The target of phase compensation design is to acquire necessary band and phase margin.

It set that cross-over frequency (bandwidth):fc at which loop gain of the return loop becomes “0” .
When the cross-over frequency becomes low, power supply fluctuation response, load response, etc worsens.
On the other hand, when cross-over frequency becomes high, loop of phase margin becomes decrease.
In order to ensure the phase margin, cross-over frequency needs to set 1/20 or below of the switching frequency.

Selection method of Phase Compensation constant is shown below.

1. Phase compensation resistor (R3) is selected in order to set the desired cross-over frequency.
   Calculation of R3 is done using the formula below.

$$R3 = \frac{2\pi \times COUT \times fc}{G_{EA} \times G_{CS}} \times \frac{Vout}{V_{FB}}$$

2. Select phase compensation capacitor (C1).
   By matching the zero of compensation to 1/4 and below of the cross-over frequency, sufficient phase margin can be acquired. C1 can be calculated using the following formula.

$$C1 > \frac{4}{2\pi \times R3 \times fc}$$

3. Examination whether the second phase compensation capacitor C2 is necessary or not is done.
   If the ESR zero of the output capacitor is smaller than half of the switching frequency, a second phase compensation capacitor is necessary. In other words, it is the case wherein the condition below happens:

$$\frac{1}{2\pi \times COUT \times RESR} < \frac{fs}{2}$$

In this case, add a second phase compensation capacitor C2, and match the frequency of the third pole fp3 to the frequency of ESR zero.
C2 can be acquired using the following formula.

$$C2 = \frac{COUT \times RESR}{R3}$$

Power Dissipation Estimate

The following formulas show how to estimate the device power dissipation under continuous mode operations. They should not be used if the device is working in the discontinuous conduction mode.

1) Conduction loss：$Pcon = IOUT^2 \times RonH \times VOUT / VCC$
2) Switching loss：$Psw = 19 \times 10^{-9} \times VCC \times IOUT \times fsw$
3) Gate charge loss：$Pgc = 9.0 \times 10^{-9} \times fsw$
4) Quiescent current loss：$Pq = ICC \times VCC$

IOUT is the output current , RonH is the on-resistance of the high-side Nch FET, VOUT is the output voltage.
VCC is the input voltage, fsw is the switching frequency.

Power dissipation of IC is the sum of above dissipation.
$Pd = Pcon + Psw + Pgc + Pq$
For given Tj,
$Tj = Ta + \theta ja \times Pd$

Pd is the total device power dissipation, Ta is the ambient temperature.
Tj is the junction temperature, θja is the thermal resistance of the package.

PCB Layout

Layout is a critical portion of a good power supply design. Here are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supply's performance. To help eliminate these problems, the VCC terminal should be bypassed to ground with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor, VCC terminal, and anode of the catch diode. See Figure.34 for a PCB layout example. The GND terminal should be soldered directly to the thermal pad under the IC and the thermal pad.

The thermal pad should be connected to any internal PCB ground plane using multiple VIAs directly under the IC. The LX terminal should be routed to the cathode of the catch diode and to the output inductor. Since the LX connection is the switching node, the catch diode and output inductor should be located close to the LX terminal, and the area of the PCB conductor is minimized to prevent excessive capacitive coupling. For operation at full rated load, the topside ground area must provide adequate heat dissipation. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts; however, this layout has been shown to produce good results and is meant as a guideline.

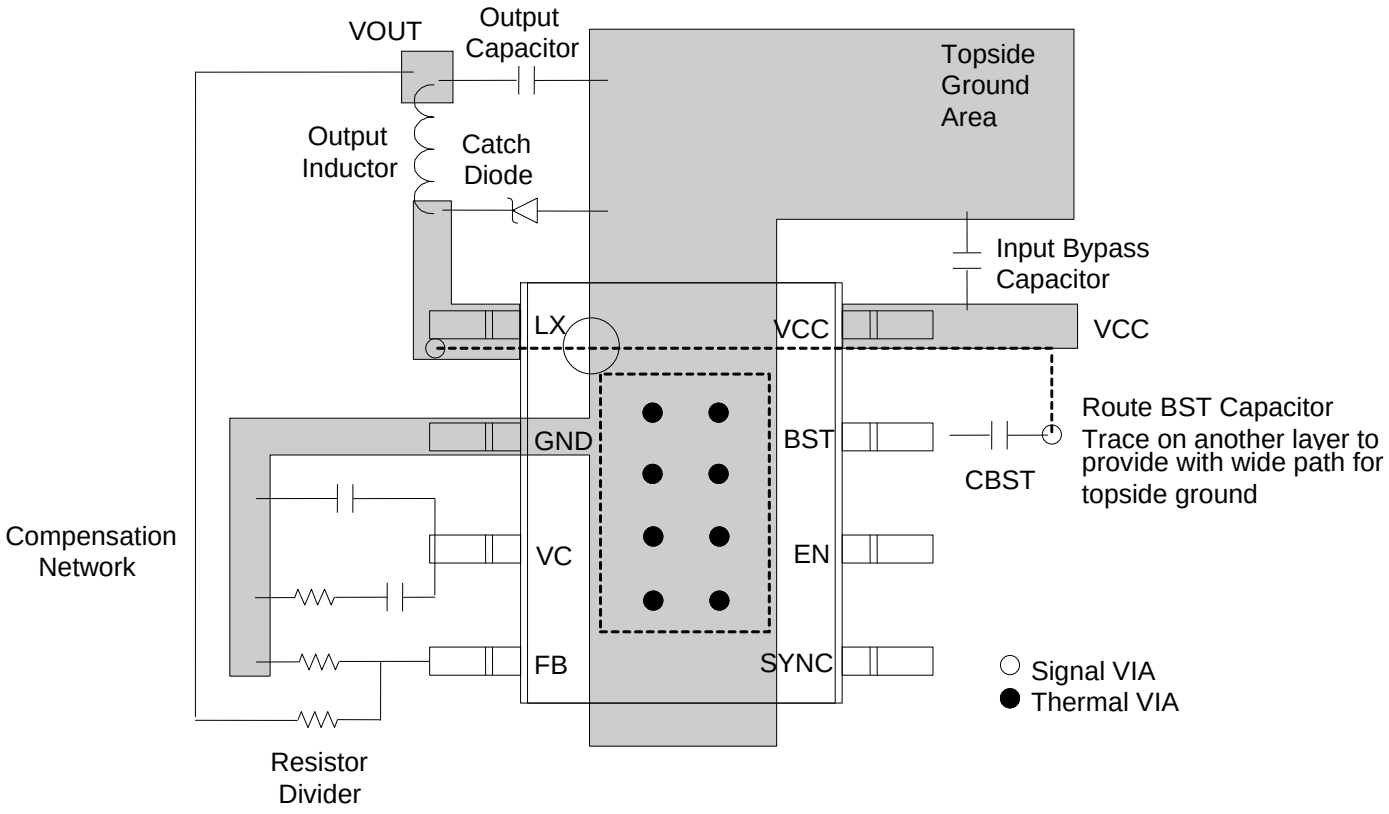
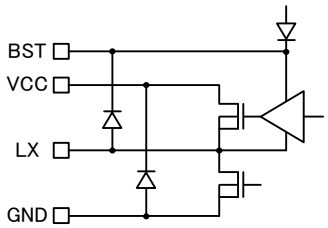
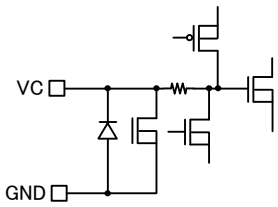
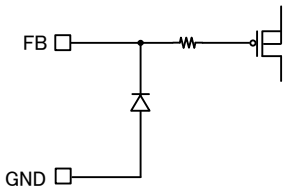
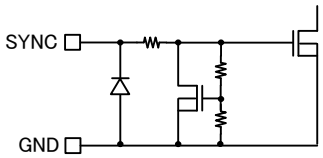
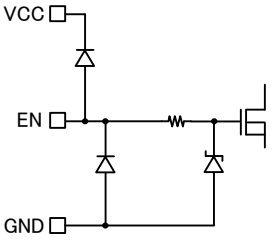


Figure 35. Reference Evaluation Board Pattern

I/O Equivalent Schematic

Pin. No	Pin. Name	Pin Equivalent Schematic
1 2 7 8	LX GND BST VCC	
3	VC	
4	FB	

Pin. No	Pin. Name	Pin Equivalent Schematic
5	SYNC	
6	EN	

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.
   In addition, including transition phenomenon, it prevents all pin except GND pin from not becoming lower than GND pin voltage.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes – Continued

10. Inter-Pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

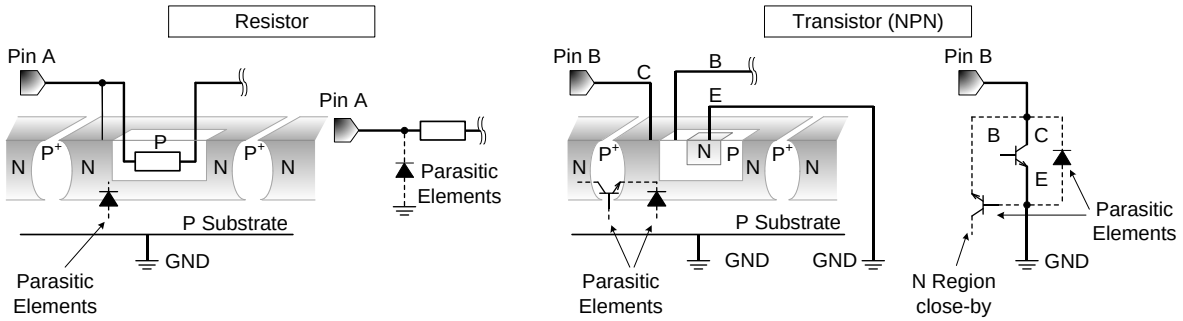


Figure 36. Example of Monolithic IC Structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

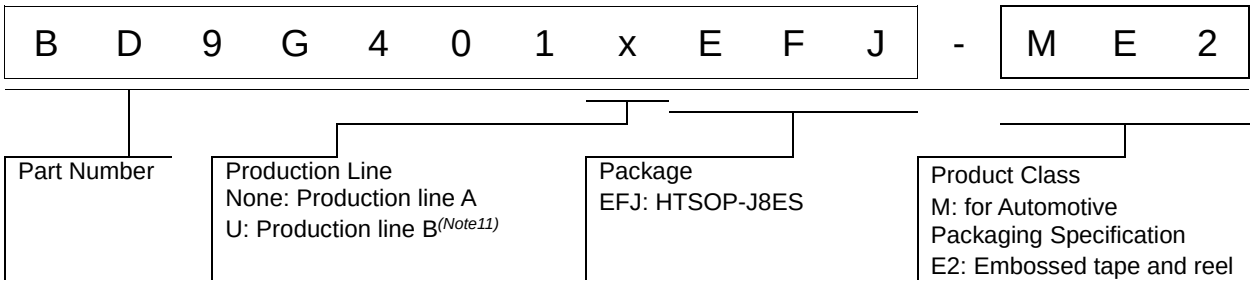
15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Part Information

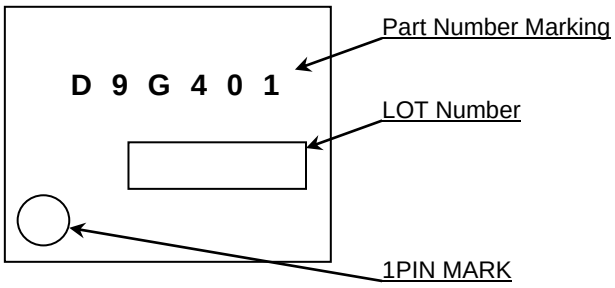


(Note11) For the purpose of improving production efficiency, this product has multi-line configuration. Electric characteristics noted in this datasheet does not differ between the 2 lines. Production line B is recommended for new product.

Marking Diagram

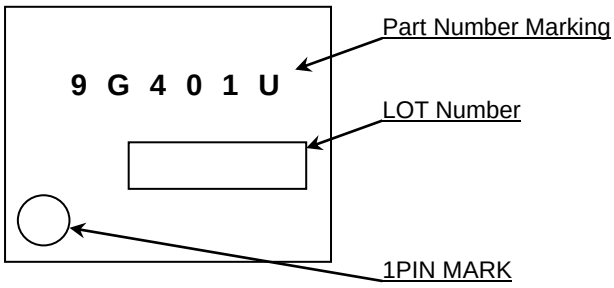
BD9G401EFJ-M

HTSOP-J8ES (TOP VIEW)



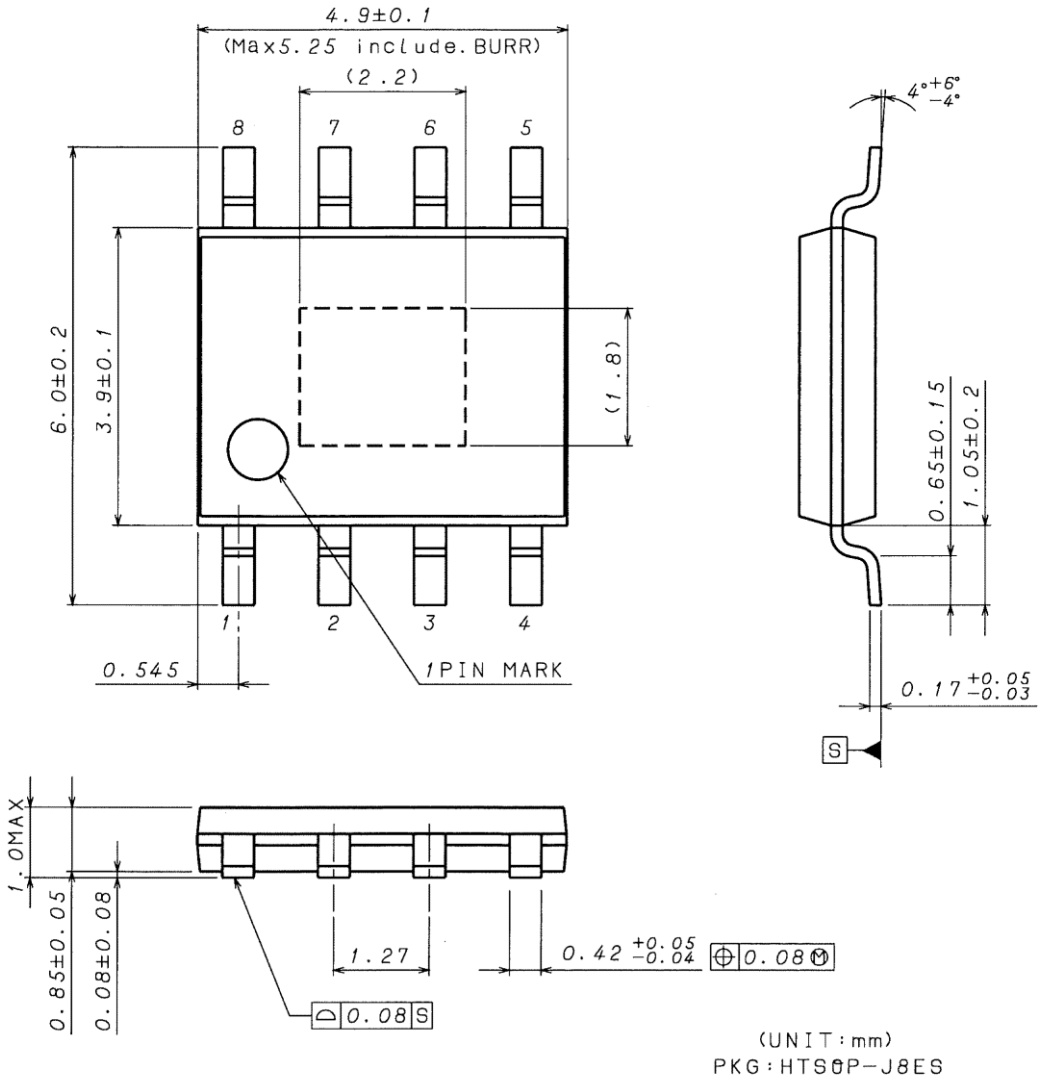
BD9G401UEFJ-M

HTSOP-J8ES (TOP VIEW)



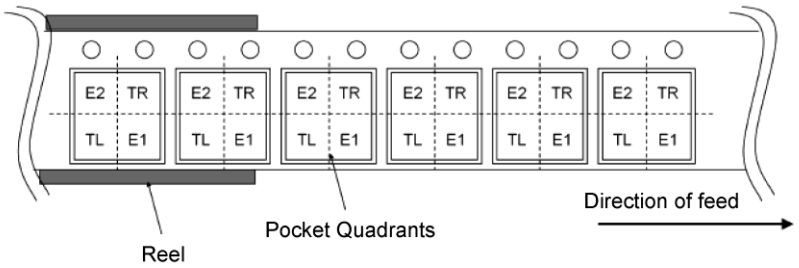
Physical Dimension, Tape and Reel Information

Package Name	HTSOP-J8ES



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
30.Nov.2016	001	Create new Rev.001
10.Mar.2017	002	P1.SYNC Terminal input frequency min 200kHz ⇒250kHz P5. Recommended Operating Ratings added SYNC Terminal Input Frequency, Input Capacitance and Inductance. P17.Inductance min value added P18.Input capacitor selection added P19.Output capacitor selection added
29.Mar.2022	003	P1-28 Added production line B part name to the header P1 Changed the package image P26 Added information of production line B to Ordering Part Information P26 Added marking diagram for production line B P27 Fixed physical dimension image P27 Updated Tape and Reel Information image

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

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General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

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