

Operational Amplifiers Series

Low Noise Operational Amplifiers

BA4510xxx



● General Description

BA4510 is dual operational amplifier with high gain. It has good performance of input referred noise voltage($6\text{ nV}/\sqrt{\text{Hz}}$) and total harmonic distortion(0.007%). These are suitable for Audio applications.

● Packages

SOP8
SSOP-B8
TSSOP-B8
MSOP8

W(Typ.) x D(Typ.) x H(Max.)
5.00mm x 6.20mm x 1.71mm
3.00mm x 6.40mm x 1.35mm
3.00mm x 6.40mm x 1.20mm
2.90mm x 4.00mm x 0.90mm

● Features

- High voltage gain
- Low input referred noise voltage
- Low distortion
- Wide operating supply voltage

● Application

- Audio application
- Consumer electronics

● Key Specification

- Wide Operating Supply Voltage (split supply) : $\pm 1.0\text{V}$ to $\pm 3.5\text{V}$
- Wide Temperature Range: -20°C to $+75^\circ\text{C}$
- High Slew Rate: $5\text{V}/\mu\text{s}(\text{Typ.})$
- Total Harmonic Distortion: 0.007% (Typ.)
- Input Referred Noise Voltage: $6\text{ nV}/\sqrt{\text{Hz}}$ (Typ.)

● Block Diagrams

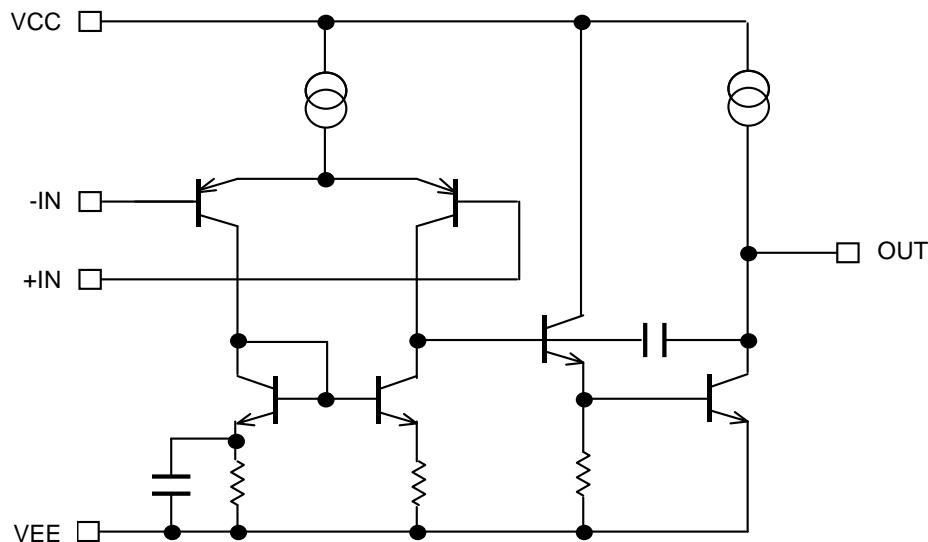
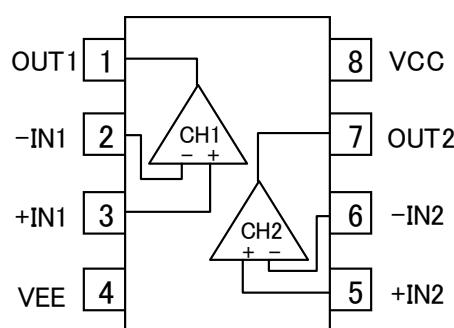


Figure 1. Simplified schematic

Product structure : Silicon monolithic integrated circuit This product is not designed protection against radioactive rays.

●Pin Configuration(TOP VIEW)

SOP8, SSOP-B8, TSSOP-B8, MSOP8



Pin No.	Symbol
1	OUT1
2	-IN1
3	+IN1
4	VEE
5	+IN2
6	-IN2
7	OUT2
8	VCC

Package			
SOP8	SSOP-B8	TSSOP-B8	MSOP8
BA4510F	BA4510FV	BA4510FVT	BA4510FVM

●Ordering Information

B	A	4	5	1	0	x	x	x	-	E2
<hr/>										
Part Number					Package			Packaging and forming specification		
BA4510xxx					F : SOP8			E2: Embossed tape and reel		
					FV : SSOP-B8			(SOP8/SSOP-B8/TSSOP-B8)		
					FVT : TSSOP-B8			TR: Embossed tape and reel		
					FVM : MSOP8			(MSOP8)		

●Line-up

Topr	Operating Supply Voltage (split supply)	Supply Current (Typ.)	Slew Rate (Typ.)	Package		Orderable Part Number
-20°C to +75°C	±1.0V to ±3.5V	5mA	5V/µs	SOP8	Reel of 2500	BA4510F-E2
				SSOP-B8	Reel of 2500	BA4510FV-E2
				TSSOP-B8	Reel of 2500	BA4510FVT-E2
				MSOP8	Reel of 3000	BA4510FVM-TR

● Absolute Maximum Ratings (Ta=25°C)

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Parameter	Symbol	Ratings	Unit
Supply Voltage	VCC-VEE	+10	V
Power dissipation	Pd	SOP8	620 ^{*1*5}
		SSOP-B8	550 ^{*2*5}
		TSSOP-B8	500 ^{*3*5}
		MSOP8	470 ^{*4*5}
Differential Input Voltage ^{*6}	Vid	VCC-VEE	V
Input Common-mode Voltage Range	Vicm	VEE to VCC	V
Operating Supply Voltage	Vopr	2 to 7(±1 to ±3.5)	V
Operating Temperature	Topr	-20 to +75	°C
Storage Temperature	Tstg	-40 to 125	°C
Maximum Junction Temperature	Tjmax	+125	°C

Note: Absolute maximum rating item indicates the condition which must not be exceeded.

Application of voltage in excess of absolute maximum rating or use out absolute maximum rated temperature environment may cause deterioration of characteristics.

^{*1} To use at temperature above Ta=25°C reduce 6.2mW/°C^{*2} To use at temperature above Ta=25°C reduce 5.5mW/°C^{*3} To use at temperature above Ta=25°C reduce 5.0mW/°C^{*4} To use at temperature above Ta=25°C reduce 4.8mW/°C^{*5} Mounted on a FR4 glass epoxy PCB(70mmx70mmx1.6mm).^{*6} The voltage difference between inverting input and non-inverting input is the differential input voltage.

Then input terminal voltage is set to more than VEE.

● Electrical Characteristics

OBA4510 (Unless otherwise specified VCC=+2.5V, VEE=-2.5V, Ta=25°C)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Input Offset Voltage ^{*7}	Vio	-	1	6	mV	RS=50Ω
Input Offset Current ^{*7}	Iio	-	2	200	nA	-
Input Bias Current ^{*8}	Ib	-	80	500	nA	-
Supply Current	ICC	2.5	5.0	7.5	mA	RL=∞, All Op-Amps
Maximum Output Voltage(High)	VOH	+2.0	+2.4	-	V	RL=10kΩ
Maximum Output Voltage(Low)	VOL	-	-2.4	-2.0	V	RL=10kΩ
Large Signal Voltage Gain	Av	60	90	-	dB	RL≥10kΩ
Input Common-mode Voltage Range	Vicm	-1.3	-	+1.5	V	-
Common-mode Rejection Ratio	CMRR	60	80	-	dB	-
Power Supply Rejection Ratio	PSRR	60	80	-	dB	RS=50Ω
Slew Rate	SR	-	5.0	-	V/μs	Av=1
Total Harmonic Distortion+ Noise	THD+N	-	0.007	-	%	Av=20dB, RL=10kΩ, VIN=0.05Vrms, f=1kHz DIN-AUDIO
Input Referred Noise Voltage	Vn	-	6	-	nV/√Hz	RS=100Ω, Vi=0V, f=1kHz
		-	0.7	-	μVrms	DIN-AUDIO
Channel Separation	CS	-		-	dB	R1=100Ω, f=1kHz

^{*7} Absolute value^{*8} Current direction: Since first input stage is composed with PNP transistor, input bias current flows out of IC.

Description of electrical characteristics

Described here are the terms of electric characteristics used in this datasheet. Items and symbols used are also shown. Note that item name and symbol and their meaning may differ from those on another manufacturer's document or general document.

1. Absolute maximum ratings

Absolute maximum rating item indicates the condition which must not be exceeded. Application of voltage in excess of absolute maximum rating or use out of absolute maximum rated temperature environment may cause deterioration of characteristics.

1.1 Power supply voltage (VCC/VEE)

Indicates the maximum voltage that can be applied between the positive power supply terminal and negative power supply terminal without deterioration or destruction of characteristics of internal circuit.

1.2 Differential input voltage (Vid)

Indicates the maximum voltage that can be applied between non-inverting terminal and inverting terminal without deterioration and destruction of characteristics of IC.

1.3 Input common-mode voltage range (Vicm)

Indicates the maximum voltage that can be applied to non-inverting terminal and inverting terminal without deterioration or destruction of characteristics. Input common-mode voltage range of the maximum ratings not assure normal operation of IC. When normal operation of IC is desired, the input common-mode voltage of characteristics item must be followed.

1.4 Power dissipation (Pd)

Indicates the power that can be consumed by specified mounted board at the ambient temperature 25°C(normal temperature). As for package product, Pd is determined by the temperature that can be permitted by IC chip in the package (maximum junction temperature) and thermal resistance of the package.

2. Electrical characteristics item**2.1 Input offset voltage (Vio)**

Indicates the voltage difference between non-inverting terminal and inverting terminal. It can be translated into the input voltage difference required for setting the output voltage at 0 V.

2.2 Input offset current (Iio)

Indicates the difference of input bias current between non-inverting terminal and inverting terminal.

2.3 Input bias current (Ib)

Indicates the current that flows into or out of the input terminal. It is defined by the average of input bias current at non-inverting terminal and input bias current at inverting terminal.

2.4 Input common-mode voltage range(Vicm)

Indicates the input voltage range where IC operates normally.

2.5 Large signal voltage gain (Av)

Indicates the amplifying rate (gain) of output voltage against the voltage difference between non-inverting terminal and Inverting terminal. It is normally the amplifying rate (gain) with reference to DC voltage.
 $Av = (\text{Output voltage fluctuation}) / (\text{Input offset fluctuation})$

2.6 Circuit current (ICC)

Indicates the IC current that flows under specified conditions and no-load steady status.

2.7 Maximum Output Voltage(High) / Maximum Output Voltage(Low) (VOH/VOL)

Indicates the voltage range that can be output by the IC under specified load condition. It is typically divided into maximum output voltage High and low. Maximum output voltage high indicates the upper limit of output voltage. Maximum output voltage low indicates the lower limit.

2.8 Common-mode rejection ratio (CMRR)

Indicates the ratio of fluctuation of input offset voltage when in-phase input voltage is changed. It is normally the fluctuation of DC.

$CMRR = (\text{Change of Input common-mode voltage}) / (\text{Input offset fluctuation})$

2.9 Power supply rejection ratio (PSRR)

Indicates the ratio of fluctuation of input offset voltage when supply voltage is changed. It is normally the fluctuation of DC.

$PSRR = (\text{Change of power supply voltage}) / (\text{Input offset fluctuation})$

2.10 Slew Rate (SR)

SR is a parameter that shows movement speed of operational amplifier. It indicates rate of variable output voltage as unit time.

2.11 Total harmonic distortion + Noise (THD+N)

Indicates the fluctuation of input offset voltage or that of output voltage with reference to the change of output voltage of driven channel.

2.12 Input referred noise voltage (V_n)

Indicates a noise voltage generated inside the operational amplifier equivalent by ideal voltage source connected in series with input terminal.

2.13 Channel separation (CS)

Indicates the fluctuation of input offset voltage or that of output voltage with reference to the change of output voltage of driven channel.

●Typical Performance Curves

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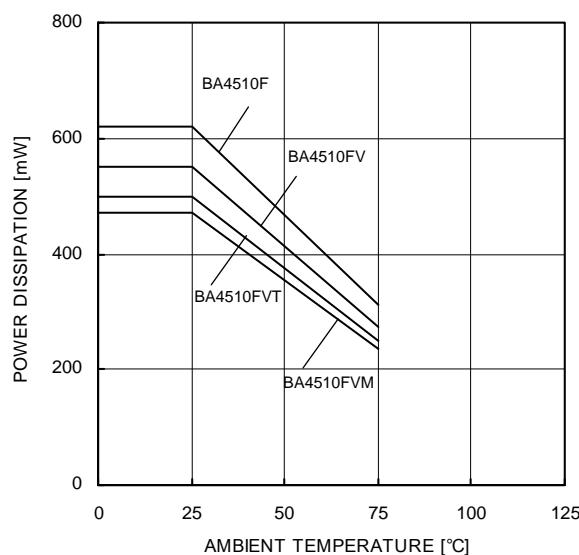


Figure 2.
Derating Curve

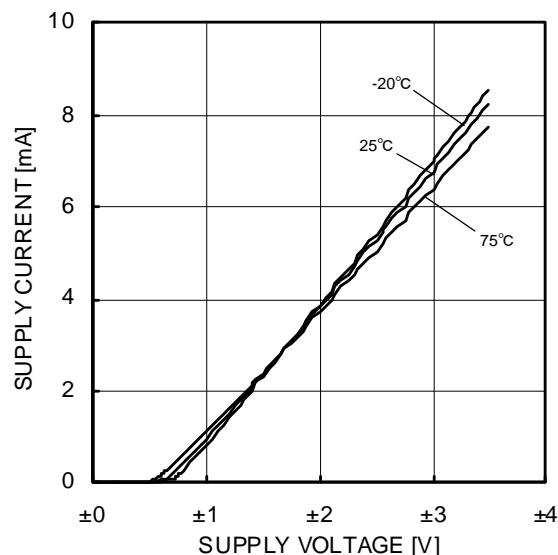


Figure 3.
Supply Current - Supply Voltage

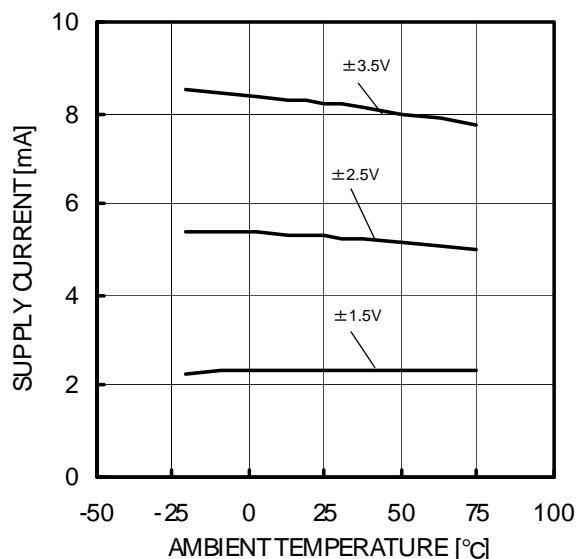


Figure 4.
Supply Current - Ambient Temperature

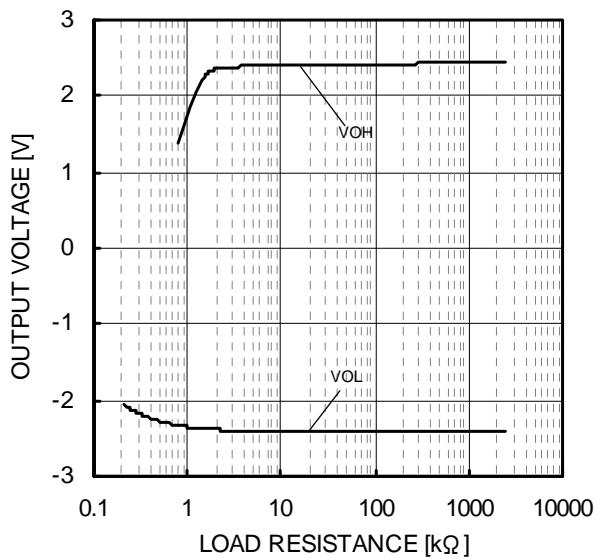


Figure 5.
Maximum Output Voltage Swing
- Load Resistance
(VCC/VEE=2.5V/-2.5V, Ta=25°C)

(*) The above data is measurement value of typical sample, it is not guaranteed.

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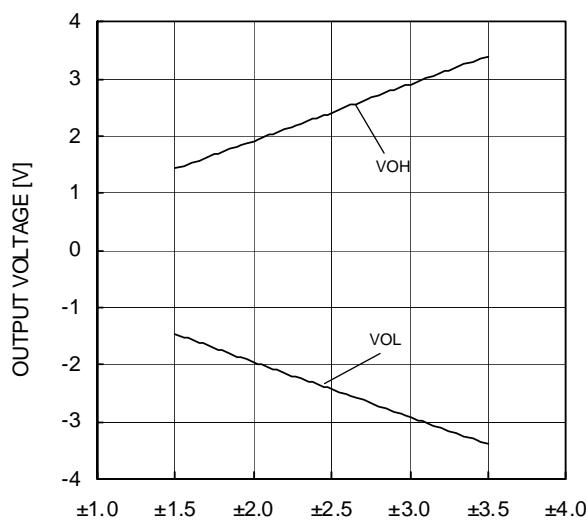


Figure 6.
Maximum Output Voltage
- Supply Voltage
($RL=10k\Omega$, $Ta=25^\circ C$)

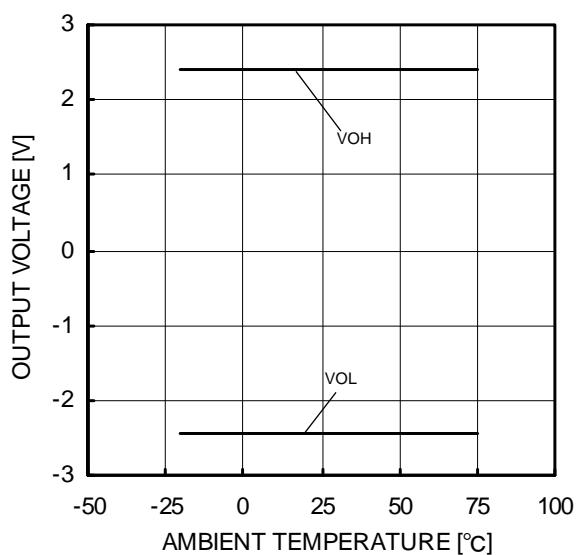


Figure 7.
Maximum Output Voltage
- Ambient Temperature
($VCC/VEE=2.5V/-2.5V$, $RL=10k\Omega$)

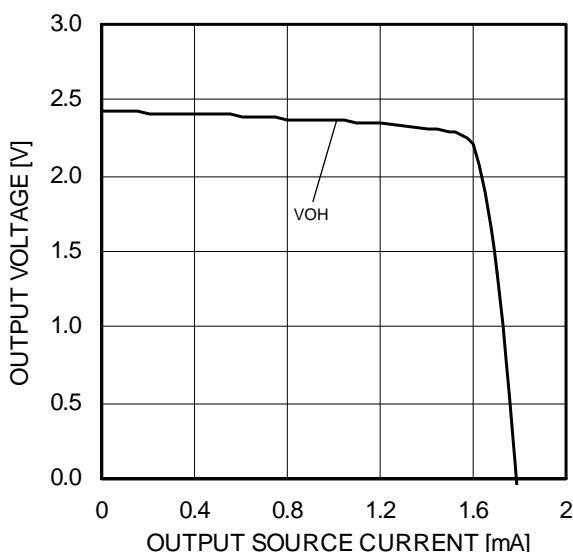


Figure 8.
Maximum Output Voltage
- Output Source Current
($VCC/VEE=2.5V/-2.5V$, $Ta=25^\circ C$)

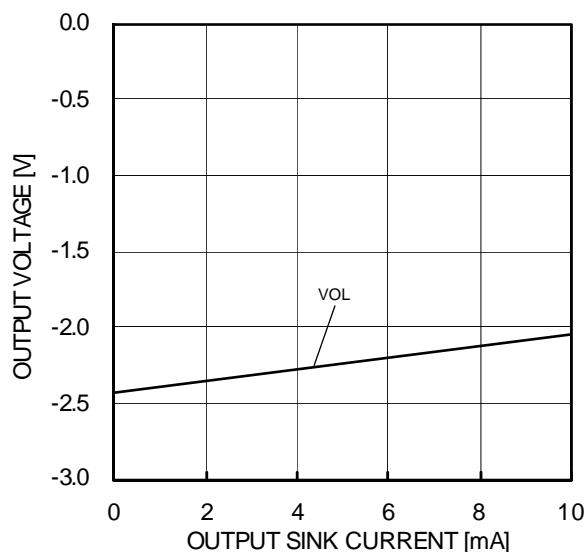


Figure 9.
Maximum Output Voltage
- Output Sink Current
($VCC/VEE=2.5V/-2.5V$, $Ta=25^\circ C$)

(*) The above data is measurement value of typical sample, it is not guaranteed.

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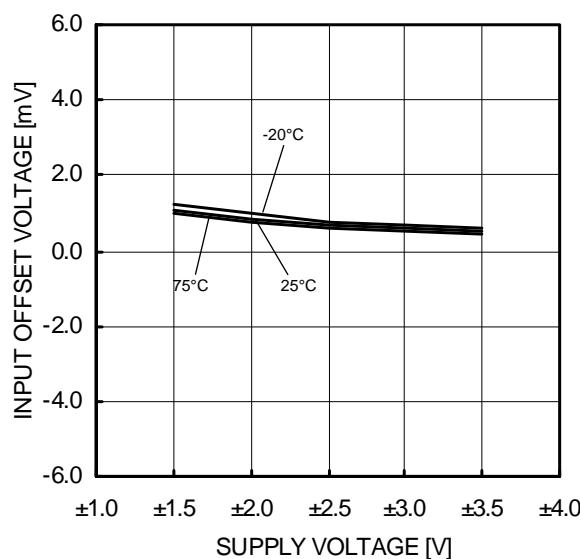


Figure 10.
Input Offset Voltage - Supply Voltage
($V_{icm}=0V$, $V_{out}=0V$)

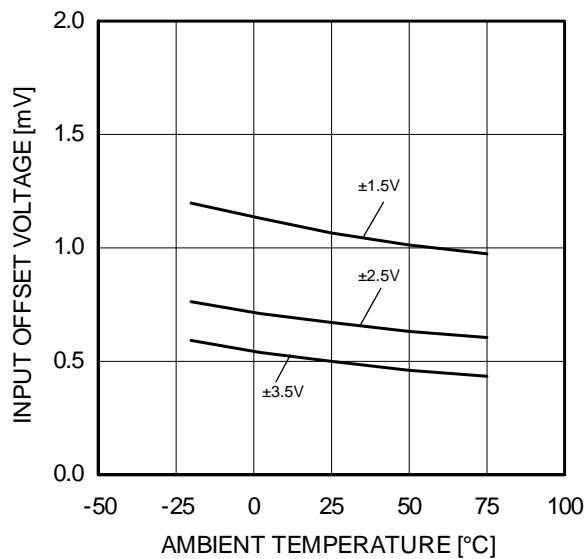


Figure 11.
Input Offset Voltage - Ambient Temperature
($V_{icm}=0V$, $V_{out}=0V$)

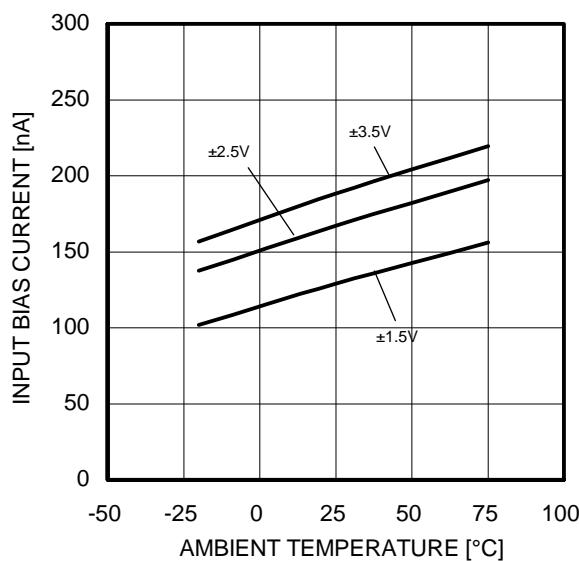


Figure 12.
Input Bias Current - Supply Voltage
($V_{icm}=0V$, $V_{out}=0V$)

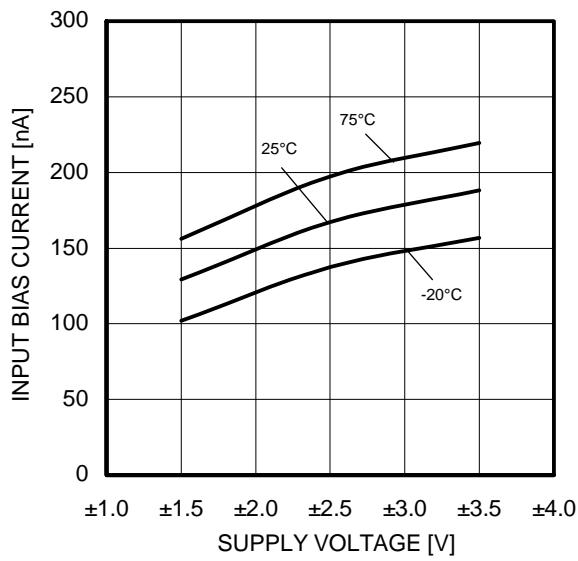


Figure 13.
Input Bias Current - Ambient Temperature
($V_{icm}=0V$, $V_{out}=0V$)

(*) The above data is measurement value of typical sample, it is not guaranteed.

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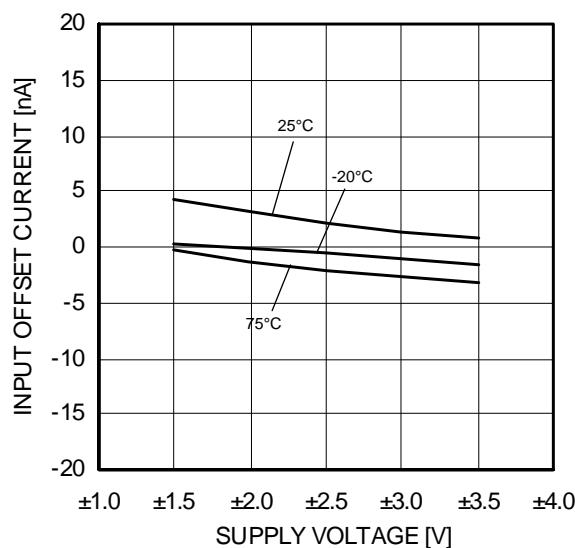


Figure 14.
Input Offset Current - Supply Voltage
($V_{ICM}=0V$, $V_{out}=0V$)

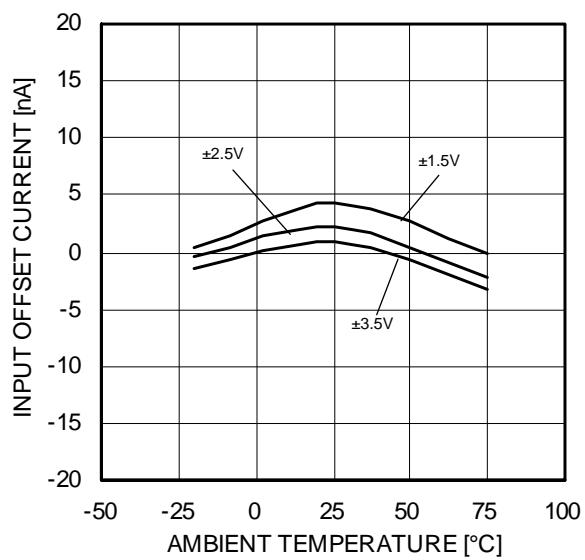


Figure 15.
Input Offset Current - Ambient Temperature
($V_{ICM}=0V$, $V_{out}=0V$)

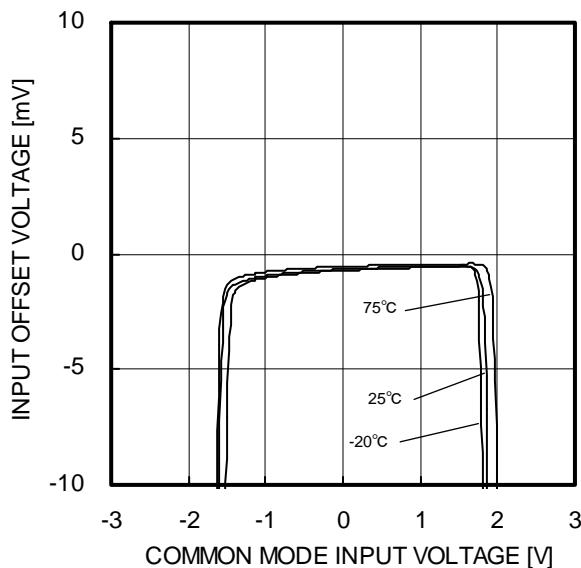


Figure 16.
Input Offset Voltage
- Common Mode Input Voltage
($V_{CC}/V_{EE}=2.5V/-2.5V$)

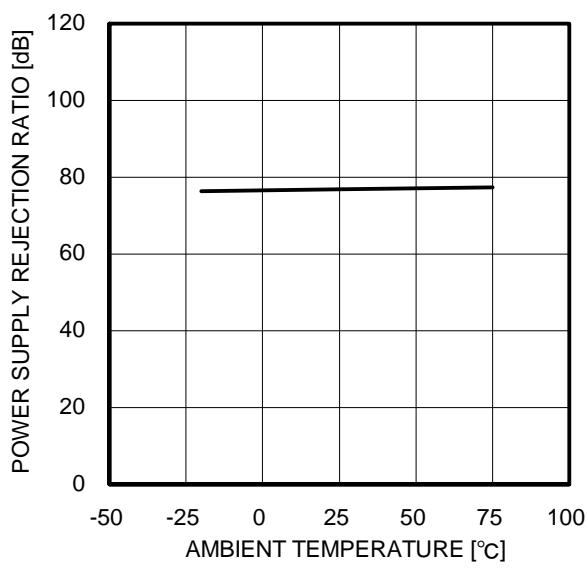


Figure 17.
Large Signal Voltage Gain
- Ambient Temperature

(*) The above data is measurement value of typical sample, it is not guaranteed.

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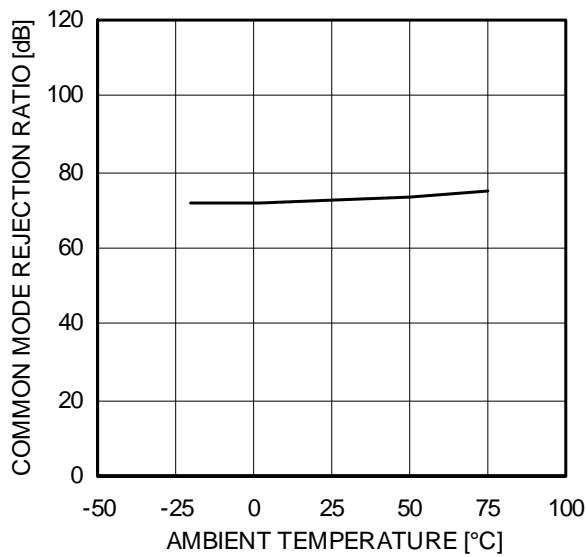


Figure 18.
Common Mode Rejection Ratio
- Ambient Temperature

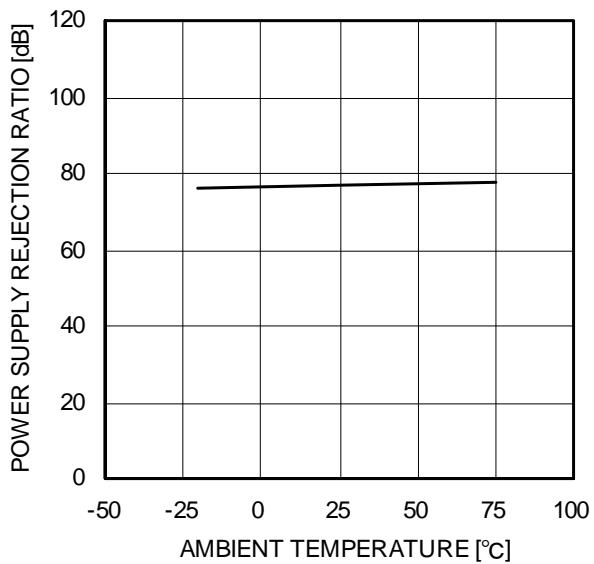


Figure 19.
Power Supply Rejection Ratio
- Ambient Temperature

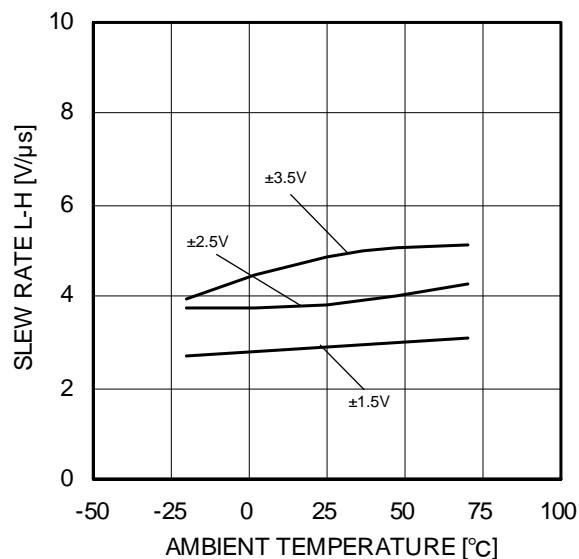


Figure 20.
Slew Rate L-H - Ambient Temperature

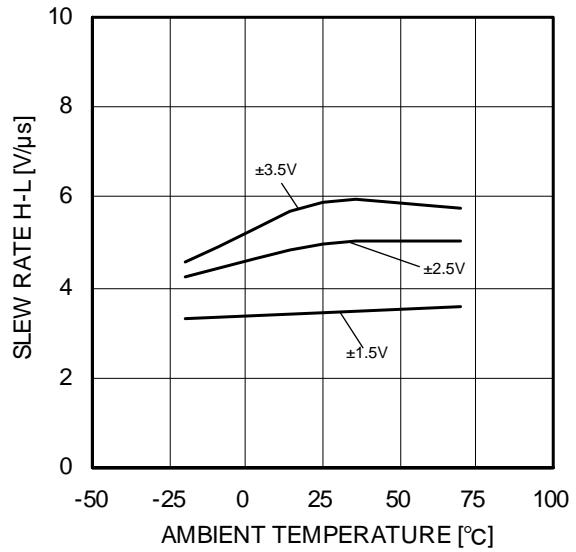


Figure 21.
Slew Rate H-L - Ambient Temperature

(*) The above data is measurement value of typical sample, it is not guaranteed.

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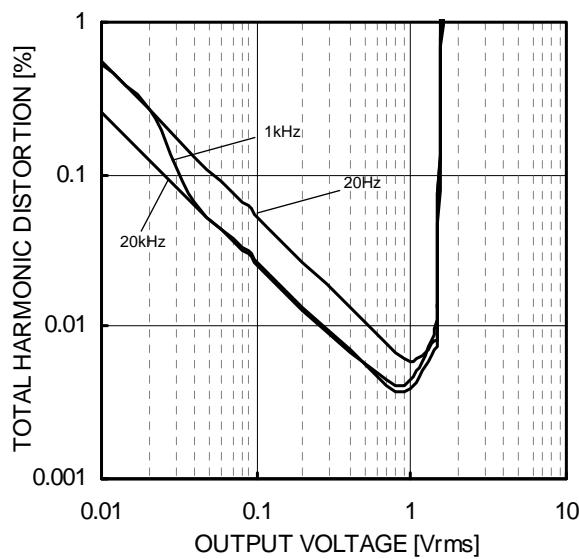


Figure 22.
Total Harmonic Distortion - Output Voltage
(VCC/VEE=2.5V/-2.5V, RL=3kΩ, 80kHz-LPF, Ta=25°C)

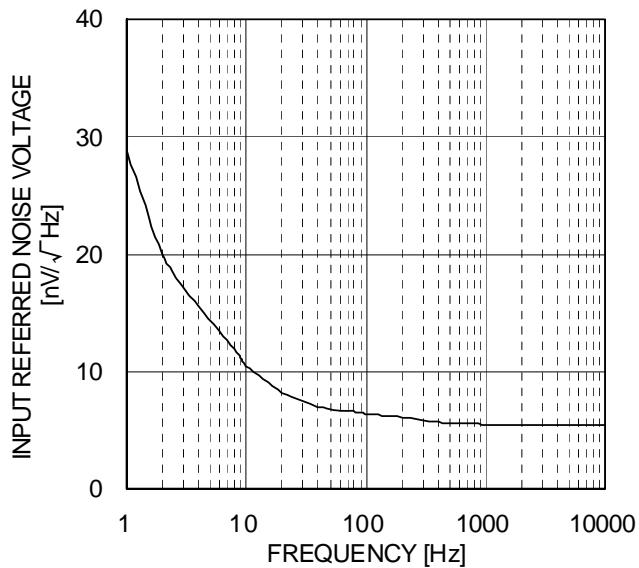


Figure 23.
Equivalent Input Noise Voltage - Frequency
(VCC/VEE=2.5V/-2.5V)

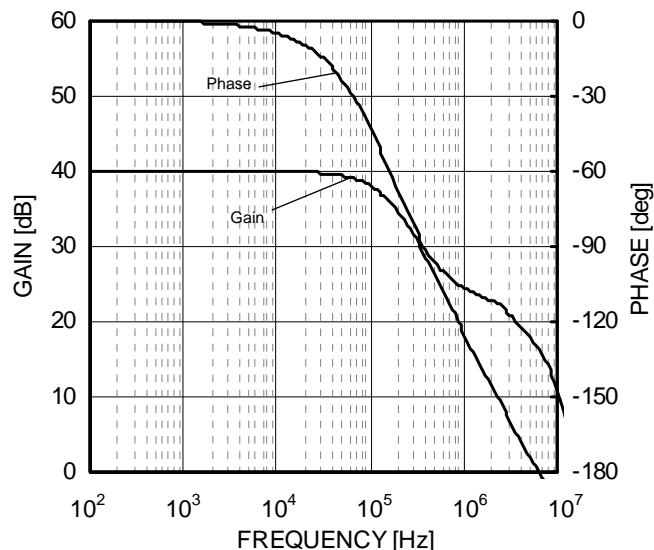


Figure 24.
Voltage Gain • Phase - Frequency
(VCC/VEE=2.5V/-2.5V, Av=40dB, RL=10kΩ)

(*) The above data is measurement value of typical sample, it is not guaranteed.

● Application Information

NULL method Condition for Test circuit1

VCC, VEE, EK, Vicm Unit: V

Parameter	VF	S1	S2	S3	VCC	VEE	EK	Vicm	calculation
Input Offset Voltage	VF1	ON	ON	OFF	2.5	-2.5	0	0	1
Input Offset Current	VF2	OFF	OFF	OFF	2.5	-2.5	0	0	2
Input Bias Current	VF3	OFF	ON	OFF	2.5	-2.5	0	0	3
	VF4	ON	OFF				0	0	
Large Signal Voltage Gain	VF5	ON	ON	ON	2.5	-2.5	0	0	4
	VF6				2.5	-2.5	0	0	
Common-mode Rejection Ratio (Input common-mode Voltage Range)	VF7	ON	ON	OFF	1	-4	0	0	5
	VF8				3.8	-1.2	0	0	
Power Supply Rejection Ratio	VF9	ON	ON	OFF	1	-1	0	0	6
	VF10				2.5	-2.5	0	0	

-Calculation-

$$1. \text{ Input Offset Voltage (Vio)} \quad V_{\text{io}} = \frac{|VF1|}{1+RF/RS} \text{ [V]}$$

$$2. \text{ Input Offset Current (lio)} \quad I_{\text{io}} = \frac{|VF2 - VF1|}{R_i \times (1+RF/RS)} \text{ [A]}$$

$$3. \text{ Input Bias Current (Ib)} \quad I_b = \frac{|VF4 - VF3|}{2 \times R_i \times (1+RF/RS)} \text{ [A]}$$

$$4. \text{ Large Signal Voltage Gain (Av)} \quad A_v = 20 \times \log \frac{\Delta EK \times (1+RF/RS)}{|VF5 - VF6|} \text{ [dB]}$$

$$5. \text{ Common-mode Rejection Ration (CMRR)} \quad CMRR = 20 \times \log \frac{\Delta Vicm \times (1+RF/RS)}{|VF8 - VF7|} \text{ [dB]}$$

$$6. \text{ Power supply rejection ratio (PSRR)} \quad PSRR = 20 \times \log \frac{\Delta Vcc \times (1+RF/RS)}{|VF10 - VF9|} \text{ [dB]}$$

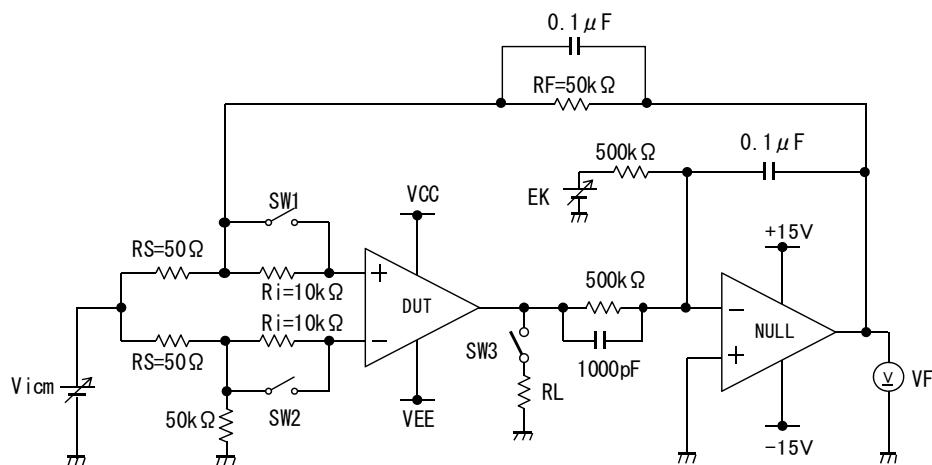


Figure 25. Test circuit1 (one channel only)

Switch Condition for Test Circuit 2

SW No.	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10	SW11	SW12	SW13	SW14
Supply Current	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Maximum Output Voltage(High)	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF
Maximum Output Voltage(Low)	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
Output Source Current	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
Output Sink Current	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
Slew Rate	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	ON	ON	OFF	OFF	OFF
Gain Bandwidth Product	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	ON	OFF	OFF	OFF
Equivalent Input Noise Voltage	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF

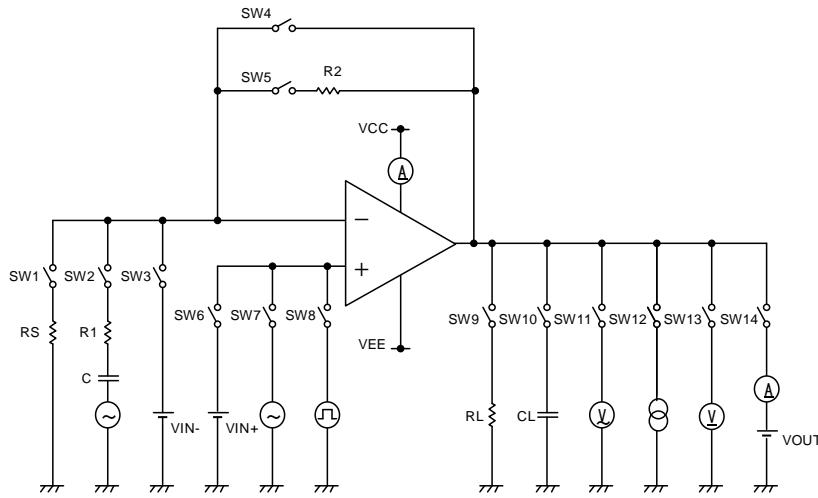


Figure 26. Test Circuit 2 (each Op-Amp)

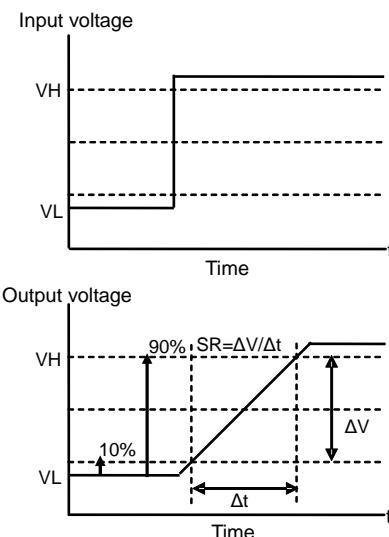
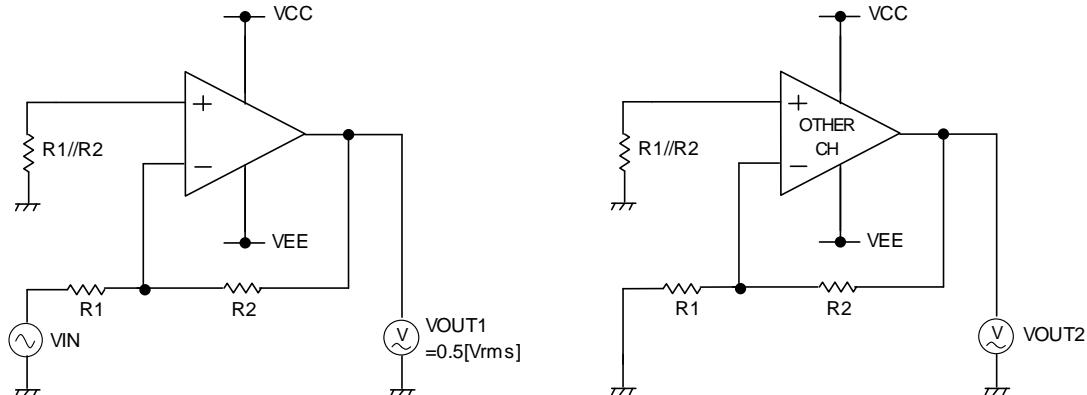


Figure 27. Slew Rate Input Waveform



$$CS = 20 \times \log \frac{100 \times VOUT1}{VOUT2}$$

Figure 28. Test Circuit 3 (Channel Separation)
(VCC=+2.5V, VEE=-2.5V, R1=100Ω, R2=10kΩ)

● Power Dissipation

Power dissipation(total loss) indicates the power that can be consumed by IC at $T_a=25^{\circ}\text{C}$ (normal temperature). IC is heated when it consumed power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip(maximum junction temperature) and thermal resistance of package(heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage temperature range. Heat generated by consumed power of IC radiates from the mold resin or lead frame of the package. The parameter which indicates this heat dissipation capability(hardness of heat release)is called thermal resistance, represented by the symbol $\theta_{ja}\text{ }^{\circ}\text{C/W}$. The temperature of IC inside the package can be estimated by this thermal resistance. Figure 29. (a) shows the model of thermal resistance of the package. Thermal resistance θ_{ja} , ambient temperature T_a , maximum junction temperature $T_{j\max}$, and power dissipation P_d can be calculated by the equation below:

$$\theta_{ja} = (T_{j\max} - T_a) / P_d \quad ^{\circ}\text{C/W} \quad \dots \dots \quad (I)$$

Derating curve in Figure 29. (b) indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance θ_{ja} . Thermal resistance θ_{ja} depends on chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Figure 30. (c) show a derating curve for an example of BA4510.

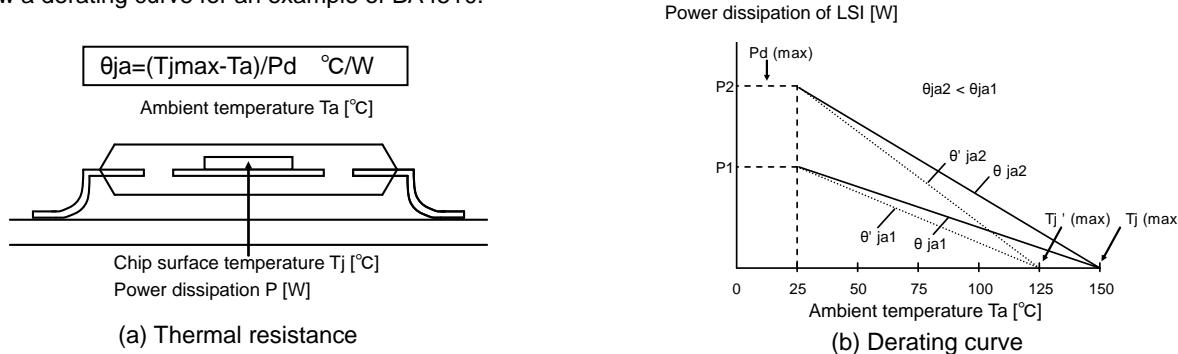
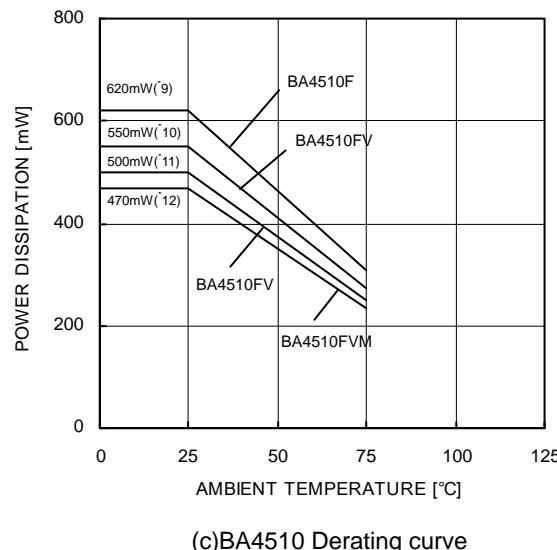


Figure 29. Thermal resistance and derating curve



(c)BA4510 Derating curve

(*9)	(*10)	(*11)	(*12)	Unit
6.2	5.5	5.0	4.8	mW/°C

When using the unit above $T_a=25^{\circ}\text{C}$, subtract the value above per degree $^{\circ}\text{C}$. Permissible dissipation is the value.

Permissible dissipation is the value when FR4 glass epoxy board 70mm \times 70mm \times 1.6mm (cooper foil area below 3%) is mounted.

Figure 30. Derating curve

Application examples

○Voltage follower

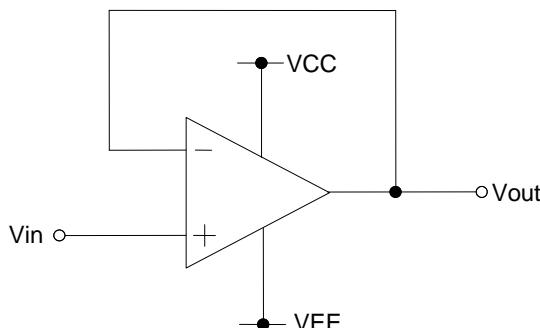


Figure 31. Voltage follower circuit

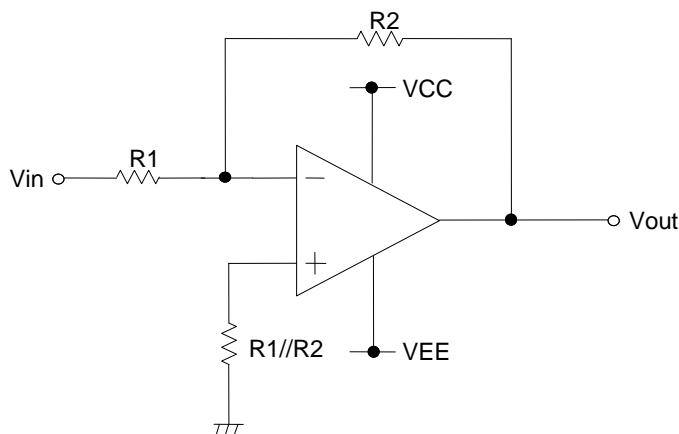
Voltage gain is 0 dB.

This circuit controls output voltage (Vout) equal input voltage (Vin), and keeps Vout with stable because of high input impedance and low output impedance.

Vout is shown next expression.

 $V_{out} = V_{in}$

○Inverting amplifier



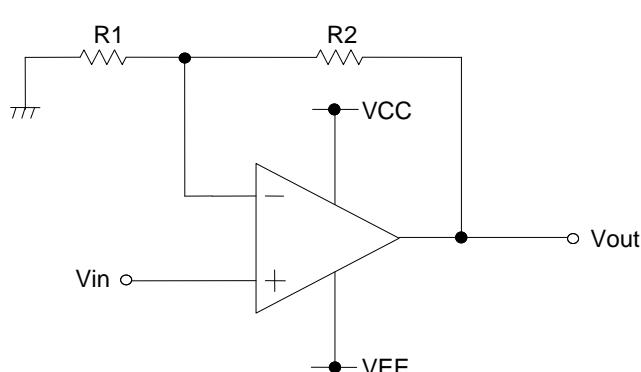
For inverting amplifier, Vin is amplified by voltage gain decided R1 and R2, and phase reversed voltage is output.

Vout is shown next expression.

 $V_{out} = -(R_2/R_1) \cdot V_{in}$

Input impedance is R1.

○Non-inverting amplifier



For non-inverting amplifier, Vin is amplified by voltage gain decided R1 and R2, and phase is same with Vin.

Vout is shown next expression.

 $V_{out} = (1 + R_2/R_1) \cdot V_{in}$

This circuit performs high input impedance because Input impedance is operational amplifier's input Impedance.

Figure 33. Non-inverting amplifier circuit

●Operational Notes

1) Processing of unused circuit

It is recommended to apply connection (see the Figure 34.) and set the non inverting input terminal at the potential within input common-mode voltage range (V_{icm}), for any unused circuit.

2) Input voltage

Please note that the circuit operates normally only when the input voltage is within the common mode input voltage range of the electric characteristics.

3) Maximum output voltage

Because the output voltage range becomes narrow as the output current increases, design the application with margin by considering changes in electrical characteristics and temperature characteristics.

4) Short-circuit of output terminal

When output terminal and VCC or VEE terminal are shorted, excessive Output current may flow under some conditions, and heating may destroy IC. It is necessary to connect a resistor as shown in Figure 35. thereby protecting against load shorting.

5) Power supply (split supply / single supply) in used

Op-amp operates when specified voltage is applied between VCC and VEE. Therefore, the single supply Op-Amp can be used for double supply Op-Amp as well.

6) Power dissipation (P_d)

Use a thermal design that allows for a sufficient margin in light of the power dissipation (P_d) in actual operating conditions.

7) Short-circuit between pins and wrong mounting

Pay attention to the assembly direction of the ICs. Wrong mounting direction or shorts between terminals, GND, or other components on the circuits, can damage the IC.

8) Use in strong electromagnetic field

Using the ICs in strong electromagnetic field can cause operation malfunction.

9) Radiation

This IC is not designed to be radiation-resistant.

10) Handing of IC

When stress is applied to IC because of deflection or bend of board, the characteristics may fluctuate due to piezo resistance effects.

11) Inspection on set board

During testing, turn on or off the power before mounting or dismounting the board from the test Jig. Do not power up the board without waiting for the output capacitors to discharge. The capacitors in the low output impedance terminal can stress the device. Pay attention to the electro static voltages during IC handling, transportation, and storage.

12) Output capacitor

When VCC terminal is shorted to VEE (GND) potential and an electric charge has accumulated on the external capacitor, connected to output terminal, accumulated charge may be discharged VCC terminal via the parasitic element within the circuit or terminal protection element. The element in the circuit may be damaged (thermal destruction). When using this IC for an application circuit where there is oscillation, output capacitor load does not occur, as when using this IC as a voltage comparator. Set the capacitor connected to output terminal below $0.1\mu F$ in order to prevent damage to IC.

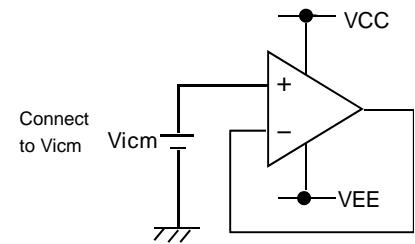


Figure 34. The example of application circuit for unused op-amp

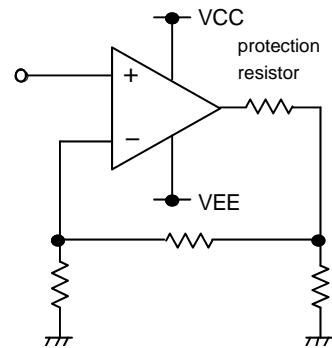


Figure 35. The example of output short protection

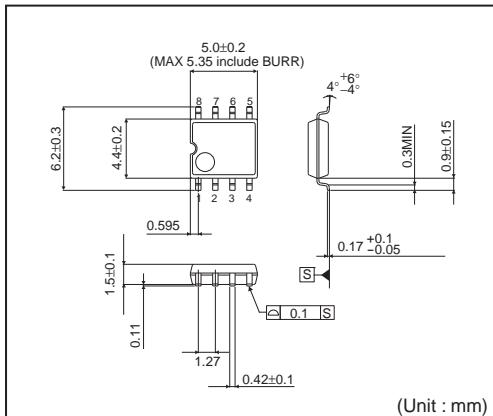
Status of this document

The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document formal version takes priority.

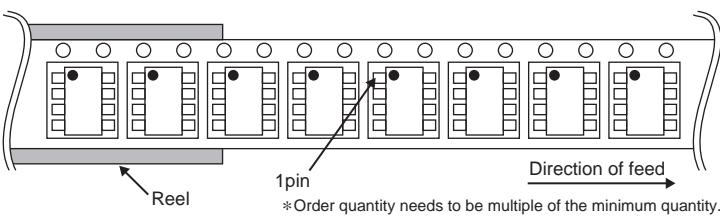
●Physical Dimensions Tape and Reel Information

SOP8

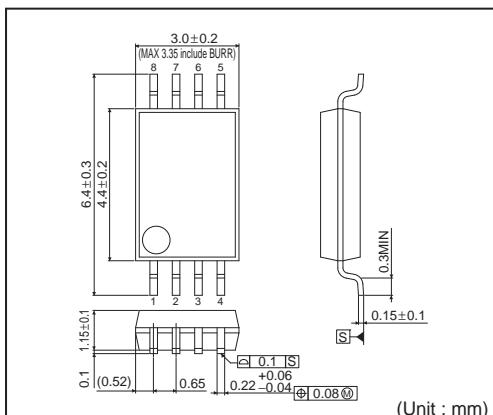


<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

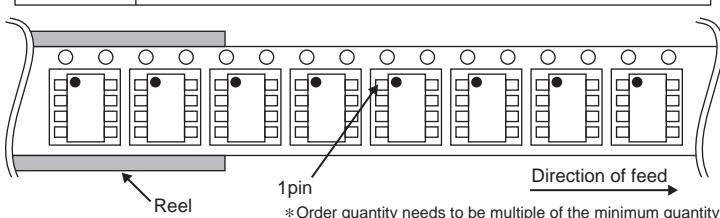


SSOP-B8

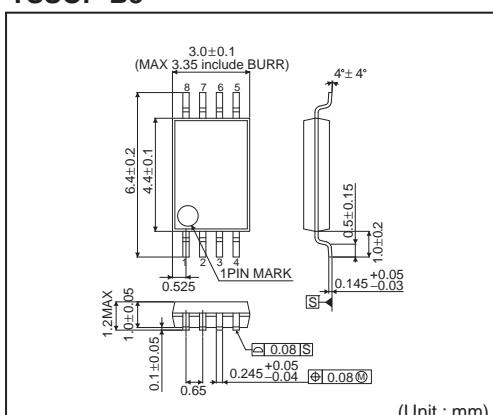


<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

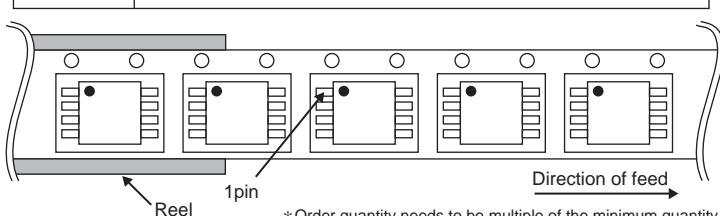


TSSOP-B8

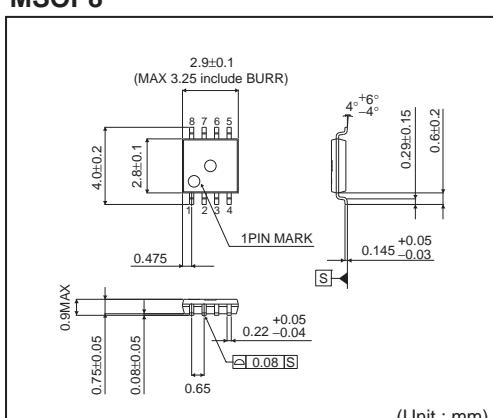


<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

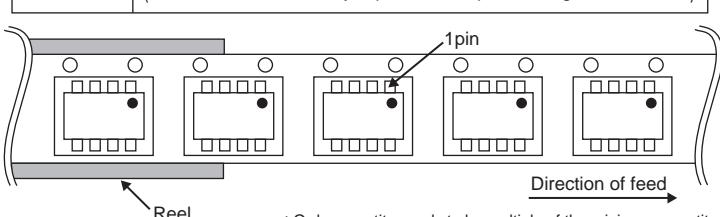


MSOP8

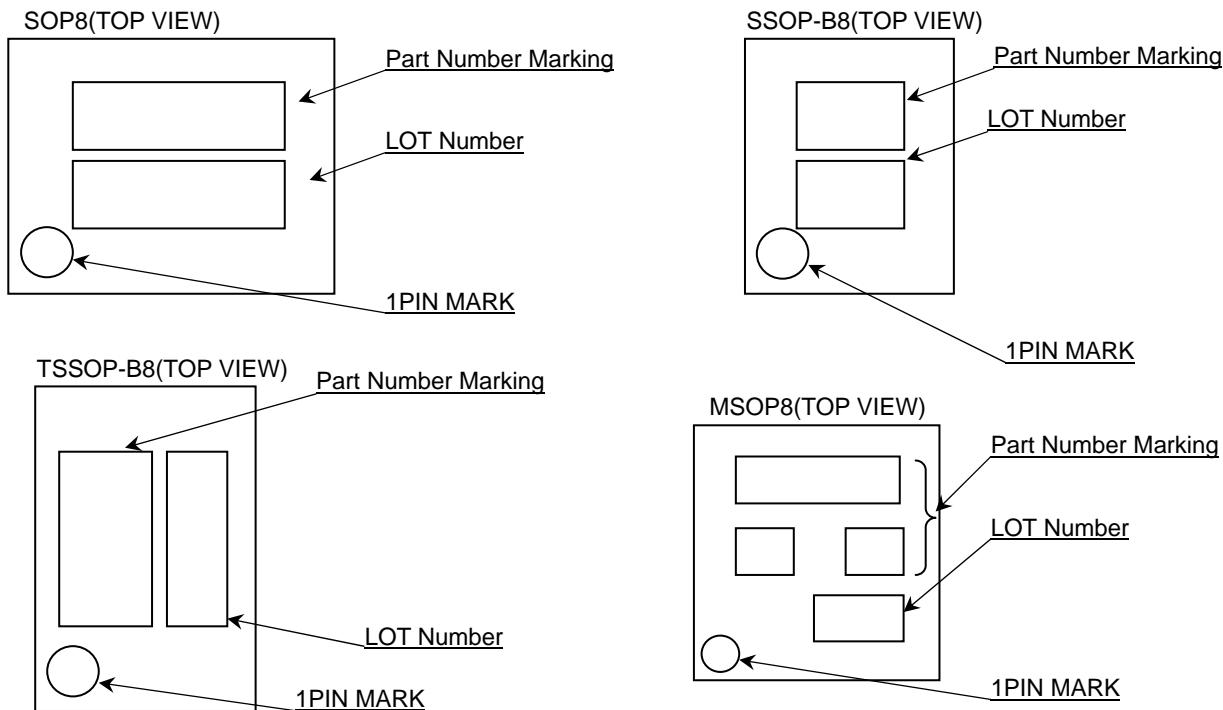


<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



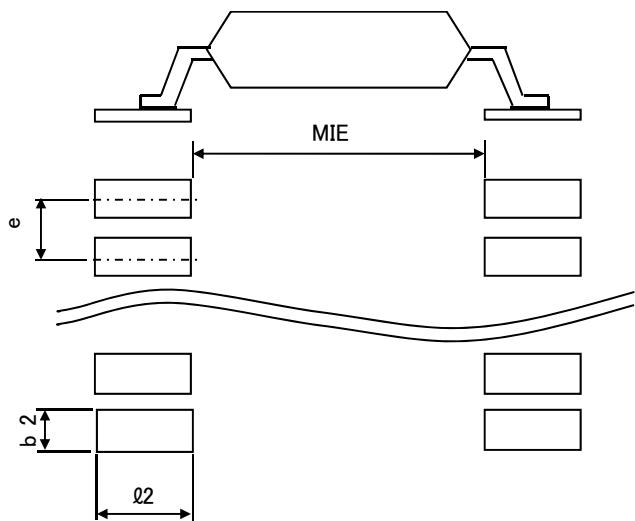
●Marking Diagrams



Product Name		Package Type	Marking
BA4510	F	SOP8	4510
	FV	SSOP-B8	
	FVT	TSSOP-B8	
	FVM	MSOP8	

●Land pattern data

PKG	Land pitch <i>e</i>	Land space MIE	all dimensions in mm	
			Land length $\geq l_2$	Land width <i>b</i> ₂
SOP8	1.27	4.60	1.10	0.76
SSOP-B8	0.65	4.60	1.20	0.35
TSSOP-B8	0.65	4.60	1.20	0.35
MSOP8	0.65	2.62	0.99	0.35



● Revision History

Date	Revision	Changes
2012.11.7	001	New Release

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - Installation of redundant circuits to reduce the impact of single or multiple circuit failure
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 - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
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- Confirm that operation temperature is within the specified range described in the product specification.
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- In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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